## **General Description**

The SAB 82258A is an advanced general-purpose four-channel DMA controller tailored for efficient high speed data transfer between peripheral devices and memories. It is either coupled tightly with a companion CPU (local mode) or working in stand alone applications using the remote mode. The SAB 82258A is unique among DMA controllers providing complete direct interfacing to the SAB 80286 as well as to SAB 80186/188/86/88 bus.

Its four superfast DMA channels transfer rate up to 10 Mbytes per second are possible. If the maximum transfer rate reaches as much as 20 Mbyte/second. In addition one of the DMA channels may be configured as multiplexer channel so that a large number of low speed peripherals can share the use of the same channel. The interrupt structure belongs to the fastest and most versatile ones available. Multiple SAB 82258A DMAs can be integrated very easily by using a simple local bus arbiter logic.

The SAB 82258A is the only DMA controller that provides source or destination-oriented data chaining (two chaining modes) as well as conditional command chaining (jumps within channel program based on several conditions).

Туре	Package	Speed	Muxed Channel
SAB 82C257-1-N	P-LCC-68-1 (SMD)	10 MHz	no
SAB 82C258A-12-N	P-LCC-68-1 (SMD)	12 MHz	yes
SAB 82C258A-20-N	P-LCC-68-1 (SMD)	20 MHz	yes

## **Features**

- 16-bit DMA controller for 16-bit family processors
  - SAB 80286
  - SAB 80186 188
  - SAB 8086/88
- 4 independent high-speed DMA channels
- 16 Mbyte addressing range
- 16 Mbyte maximum block length
- · Memory based communication with CPU
- "On-the fly" compare, translate and verify operations
- Transfer rates up to 10 Mbyte/s
- 32-bit-fly-by transfers with up to 20 Mbyte/s (10-MHz system)
- Single cycle and two cycle transfer
- · Automatic chaining of command blocks
- · Variable chaining of data blocks
- Multiplexer mode operation with up to 32 subchannels
- · Local and remote (standalone) mode
- Support of 16-bit and 8-bit data buses
- Multiple programmable control of channel priorities
- Direct and fast CPU/channel communication

