AT91SAM ARM-based Embedded MPU

SAMA5D3 Series

PRELIMINARY SUMMARY DATASHEET

Description

The Atmel SAMA5D3 series is a high-performance, power-efficient embedded MPU based on the ARM® Cortex™-A5 processor, achieving 536 MHz with power consumption levels below 0.5 mW in low-power mode. The device features a floating point unit for high-precision computing and accelerated data processing, and a high data bandwidth architecture. It integrates advanced user interface and connectivity peripherals and security features.

The SAMA5D3 series features an internal multi-layer bus architecture associated with 39 DMA channels to sustain the high bandwidth required by the processor and the high-speed peripherals. The device offers support for DDR2/LPDDR/LPDDR2 and MLC NAND Flash memory with 24-bit ECC.

The comprehensive peripheral set includes an LCD controller with overlays for hardware-accelerated image composition, a touchscreen interface and a CMOS sensor interface. Connectivity peripherals include Gigabit EMAC with IEEE1588, 10/100 EMAC, multiple CAN, UART, SPI and I2C. With its secure boot mechanism, hardware accelerated engines for encryption (AES, TDES) and hash function (SHA), the SAMA5D3 ensures anti-cloning, code protection and secure external data transfers.

The SAMA5D3 series is optimized for control panel/HMI applications and applications that require high levels of connectivity in the industrial and consumer markets. Its low-power consumption levels make the SAMA5D3 particularly suited for battery-powered devices.

There are four SAMA5D3 devices in this series. The following table shows the differences in the embedded features. All other features are available on all derivatives; this includes the three USB ports as well as the encryption engine and secure boot features.

This is a summary document. The complete document is available on the Atmel website at www.atmel.com.

1. Features

- Core
  - ARM® Cortex™-A5 Processor with ARM v7-A Thumb2® Instruction Set
    - CPU Frequency up to 536 MHz
  - 32 Kbyte Data Cache, 32 Kbyte Instruction Cache, Virtual Memory System Architecture (VMSA)
  - Fully Integrated MMU and Floating Point Unit (VFPv4)
- Memories
  - One 160 Kbyte Internal ROM Single-cycle Access at System Speed, Embedded Boot Loader: Boot on NAND Flash, SDCard, eMMC, serial DataFlash®, selectable Order
  - One 128 Kbyte Internal SRAM, Single-cycle Access at System Speed
  - High Bandwidth 32-bit Multi-port Dynamic Ram Controller supporting 512 Mbyte 8 bank DDR2/LPDDR/LPDDR2
  - Independent Static Memory Controller with SLC/MLC NAND Support with up to 24-bit Error Correcting Code (PMECC)
- System running up to 166 MHz
  - Power-on Reset Cells, Reset Controller, Shut Down Controller, Periodic Interval Timer, Watchdog Timer and Real Time Clock
  - Boot Mode Select Option, Remap Command
  - Internal Low-power 32 kHz RC Oscillator and Fast 12 MHz RC Oscillators
  - Selectable 32768 Hz Low-power Oscillator and 12 MHz Oscillator
  - One 400 to 1000 MHz PLL for the System and one PLL at 480 MHz optimized for USB High Speed
  - 39 DMA Channels including two 8-channel 64-bit Central DMA Controllers
  - 64-bit Advanced Interrupt Controller
  - Three Programmable External Clock Signals
  - Programmable Fuse Box with 256 fuse bits, 192 of them available for Customer
- Low Power Management
  - Shut Down Controller
  - Battery Backup Registers
  - Clock Generator and Power Management Controller
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
- Peripherals
  - LCD TFT Controller with Overlay, Alpha-blending, Rotation, Scaling and Color Space Conversion
  - ITU-R BT. 601/656 Image Sensor Interface
  - Three HS/FS/LS USB Ports with On-Chip Transceivers
    - One Device Controller
    - One Host Controller with Integrated Root Hub (3 Downstream Ports)
  - One 10/100/1000 Mbps Gigabit Ethernet Mac Controller (GMAC) with IEEE1588 support
  - One 10/100 Mbps Ethernet Mac Controller (EMAC)
  - Two CAN Controllers with 8 Mailboxes, fully Compliant with CAN 2.0 Part A and 2.0 Part B
  - Softmodem Interface
  - Three High Speed Memory Card Hosts (eMMC 4.3 and SD 2.0)
  - Two Master/Slave Serial Peripheral Interface
  - Two Synchronous Serial Controllers
  - Three Two-wire Interface up to 400 Kbits supporting I2C Protocol and SMBUS
  - Four USARTs, two UARTs, one DBGU
  - Two Three-channel 32-bit Timer/Counters

- One Four-channel 16-bit PWM Controller
- One 12-channel 12-bit Analog-to-Digital Converter with Resistive Touch-Screen function
- Write Protected Registers

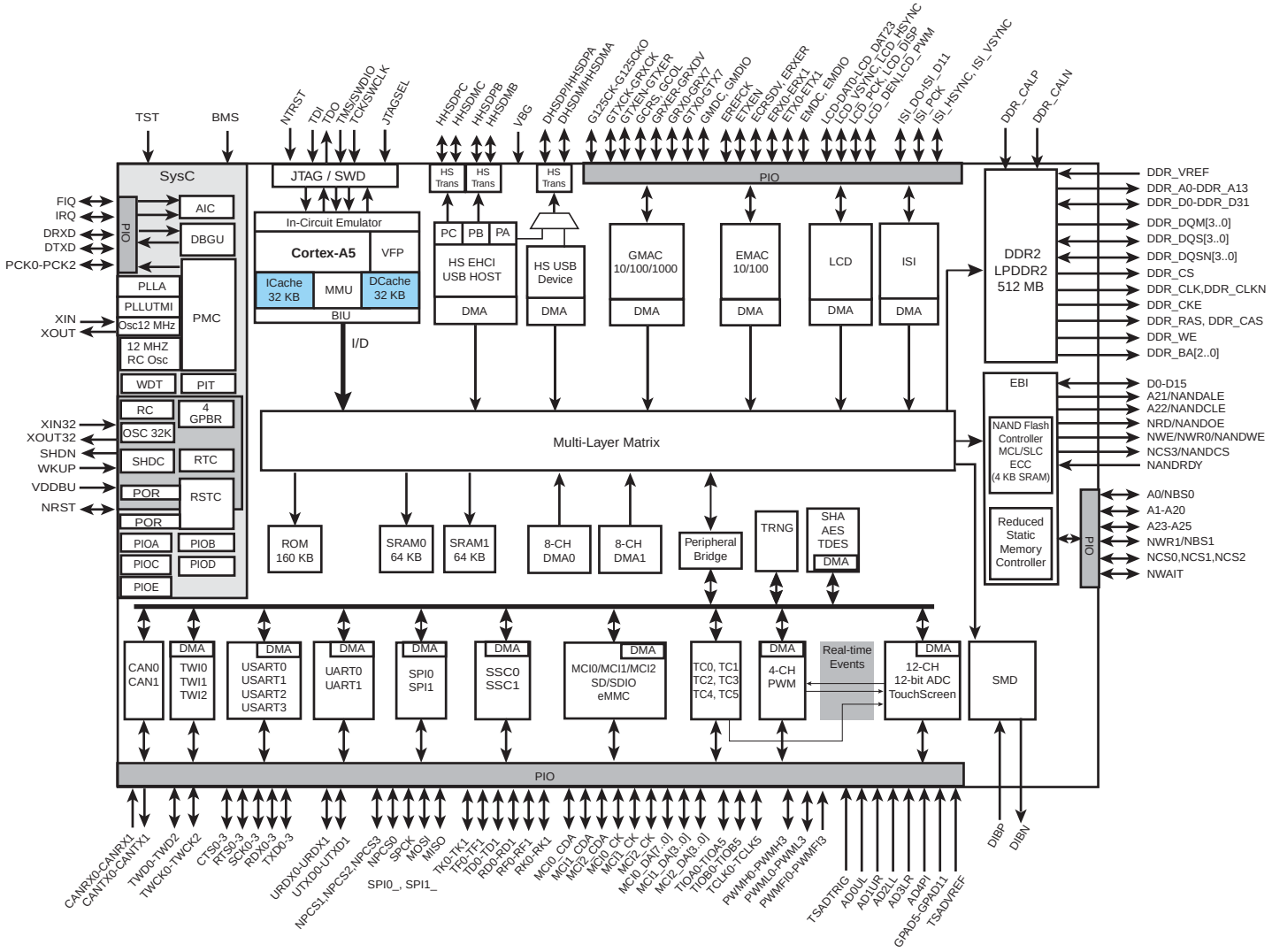
- Security
  - TRNG: True Random Number Generator
  - Encryption Engine
    - AES: 256-bit, 192-bit, 128-bit Key Algorithm, Compliant with FIPS PUB 197 Specifications
    - TDES: Two-key or Three-key Algorithms, Compliant with FIPS PUB 46-3 Specifications
    - SHA: Supports Secure Hash Algorithm (SHA1, SHA224, SHA256, SHA384, SHA512)
  - Atmel® Secure Boot Solution
- I/O
  - Five 32-bit Parallel Input/Output Controllers
  - 160 I/Os
  - Input Change Interrupt Capability on Each I/O Line, Selectable Schmitt Trigger Input
  - Individually Programmable Open-drain, Pull-up and Pull-down Resistor, Synchronous Output, Filtering
  - Slew Rate Control on High Speed I/Os
  - Impedance Control on DDR I/Os
- Package
  - 324-ball LFBGA, pitch 0.8 mm

Table 1-1. SAMA5D3 Devices

	SAMA5D31	SAMA5D33	SAMA5D34	SAMA5D35
LCDC	X	X	X	
GMAC		X	X	X
EMAC	X			X
CAN0, CAN1			X	X
HSMCI2	X		X	X
UART0	X			X
UART1	X			X
TC1				X

2. Block Diagram

Figure 2-1. SAMA5D3 Block Diagram



3. Signal Description

Table 3-1 gives details on the signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Frequency (MHz)	Comments
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input			
XOUT	Main Oscillator Output	Output			
XIN32	Slow Clock Oscillator Input	Input			
XOUT32	Slow Clock Oscillator Output	Output			
VBG	Bias Voltage Reference for USB	Analog			
PCK0 - PCK2	Programmable Clock Output	Output			
Shutdown, Wakeup Logic					
SHDN	Shut-Down Control	Output			
WKUP	Wake-Up Input	Input			
ICE and JTAG					
TCK/SWCLK	Test Clock/Serial Wire Clock	Input			
TDI	Test Data In	Input			
TDO	Test Data Out	Output			
TMS/SWDIO	Test Mode Select/Serial Wire Input/Output	I/O			
JTAGSEL	JTAG Selection	Input			
Reset/Test					
NRST	Microcontroller Reset	I/O	Low		
TST	Test Mode Select	Input			
NTRST	Test Reset Signal	Input			
BMS	Boot Mode Select	**Input**			
Debug Unit - DBGU					
DRXD	Debug Receive Data	Input			
DTXD	Debug Transmit Data	Output			
Advanced Interrupt Controller - AIC					
IRQ	External Interrupt Input	Input			
FIQ	Fast Interrupt Input	Input			
PIO Controller - PIOA - PIOB - PIOC - PIOD - PIOE					
PA0 - PAxx	Parallel IO Controller A	I/O			
PB0 - PBxx	Parallel IO Controller B	I/O			
PC0 - PCxx	Parallel IO Controller C	I/O			
PD0 - PDxx	Parallel IO Controller D	I/O			
PE0 - PExx	Parallel IO Controller E	I/O			

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Frequency (MHz)	Comments
External Bus Interface - EBI					
D0 - D15	Data Bus	I/O			
A0 - A25	Address Bus	Output			
NWAIT	External Wait Signal	Input	Low		
Static Memory Controller - HSMC					
NCS0 - NCS3	Chip Select Lines	Output	Low		
NWR0 - NWR1	Write Signal	Output	Low		
NRD	Read Signal	Output	Low		
NWE	Write Enable	Output	Low		
NBS0 - NBS1	Byte Mask Signal	Output	Low		
NANDOE	NAND Flash Output Enable	Output	Low		
NANDWE	NAND Flash Write Enable	Output	Low		
DDR2/LPDDR Controller					
DDR_VREF	Reference Voltage	Input			
DDR_CALP	Positive Calibration Reference	Input			
DDR_CALN	Negative Calibration Reference	Input			
DDR_CK, DDR_CKN	DDR2 differential clock	Output			
DDR_CKE	DDR2 Clock Enable	Output	High		
DDR_CS	DDR2 Controller Chip Select	Output	Low		
DDR_BA[2..0]	Bank Select	Output	Low		
DDR_WE	DDR2 Write Enable	Output	Low		
DDR_RAS, DDR_CAS	Row and Column Signal	Output	Low		
DDR_A[13..0]	DDR2 Address Bus	Output			
DDR_D[31..0]	DDR2 Data Bus	I/O/-PD			
DQS[3..0]	Differential Data Strobe	I/O- PD			
DQSN[3..0]	DQSN must be connected to DDR_VREF for DDR2 memories	I/O- PD			
DQM[3..0]	Write Data Mask	Output			
High Speed Multimedia Card Interface - HSMCI0-2					
MCI0_CK, MCI1_CK, MCI2_CK	Multimedia Card Clock	I/O			
MCI0_CDA,MCI1_CDA, MCI2_CDA	Multimedia Card Command	I/O			
MCI0_DA[7..0]	Multimedia Card 0 Data	I/O			
MCI1_DA[3..0]	Multimedia Card 1 Data	I/O			
MCI2_DA[3..0)	Multimedia Card 2 Data	I/O			

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Frequency (MHz)	Comments
Universal Synchronous Asynchronous Receiver Transmitter- USART0-3					
SCKx	USARTx Serial Clock	I/O			
TXDx	USARTx Transmit Data	Output			
RXDx	USARTx Receive Data	Input			
RTSx	USARTx Request To Send	Output			
CTSx	USARTx Clear To Send	Input			
Universal Asynchronous Receiver Transmitter - UARTx [1..0]					
UTXDx	UARTx Transmit Data	Output			
URXDx	UARTx Receive Data	Input			
Synchronous Serial Controller - SSCx [1..0]					
TDx	SSC Transmit Data	Output			
RDx	SSC Receive Data	Input			
TKx	SSC Transmit Clock	I/O			
RKx	SSC Receive Clock	I/O			
TFx	SSC Transmit Frame Sync	I/O			
RFx	SSC Receive Frame Sync	I/O			
Timer/Counter - TCx [5..0]					
TCLKx	TC Channel x External Clock Input	Input			
TIOAx	TC Channel x I/O Line A	I/O			
TIOBx	TC Channel x I/O Line B	I/O			
Serial Peripheral Interface - SPIx [1..0]					
SPIx_MISO	Master In Slave Out	I/O			
SPIx_MOSI	Master Out Slave In	I/O			
SPIx_SPCK	SPI Serial Clock	I/O			
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low		
SPIx_NPCS[3..1]	SPI Peripheral Chip Select	Output	Low		
Two-Wire Interface -TWIx [2..0]					
TWDx	Two-wire Serial Data	I/O			
TWCKx	Two-wire Serial Clock	I/O			
CAN controller - CANx					
CANRXx	CAN input	Input			
CANTXx	CAN output	Output			
Soft Modem - SMD					
DIBN	Soft Modem Signal	I/O			
DIBP	Soft Modem Signal	I/O			

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Frequency (MHz)	Comments
Pulse Width Modulation Controller- PWMC					
PWMH[3..0]	PWM Waveform Output High	Output			
PWML[3..0]	PWM Waveform Output LOW	Output			
PWMFIx	PWM Fault Input	Input			
USB Host High Speed Port - UHPHS					
HHSDPA	USB Host Port A High Speed Data +	Analog			
HHSDMA	USB Host Port A High Speed Data -	Analog			
HHSDPB	USB Host Port B High Speed Data +	Analog			
HHSDMB	USB Host Port B High Speed Data -	Analog			
HHSDPC	USB Host Port C High Speed Data +	Analog			
HHSDMC	USB Host Port C High Speed Data -	Analog			
USB Device High Speed Port - UDPHS					
DHSDP	USB Device High Speed Data +	Analog			
DHSDM	USB Device High Speed Data -	Analog			
GIgabit Ethernet 10/100/1000 - GMAC					
GTXCK	Transmit Clock or Reference Clock	Input			
G125CK	125 MHz input Clock	Input			
G125CKO	125 MHz output Clock	Output			
GTXEN	Transmit Enable	Output			
GTX[7..0]	Transmit Data	Output			
GTXER	Transmit Coding Error	Output			
GRXCK	Receive Clock	Input			
GRXDV	Receive Data Valid	Input			
GRX[7..0]	Receive Data	Input			
GRXER	Receive Error	Input			
GCRS	Carrier Sense and Data Valid	Input			
GCOL	Collision Detect	Input			
GMDC	Management Data Clock	Output			
GMDIO	Management Data Input/Output	I/O			
RMII Ethernet 10/100 - EMAC					
EREFCK	Transmit Clock or Reference Clock	Input			
ETXEN	Transmit Enable	Output			
ETX[1..0]	Transmit Data	Output			
ECRSDV	Carrier Sense/Data Valid	Input			
ERX[1..0]	Receive Data	Input			
ERXER	Receive Error	Input			

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Frequency (MHz)	Comments
EMDC	Management Data Clock	Output			
EMDIO	Management Data Input/Output	I/O			
LCD Controller - LCDC					
LCDDAT[23..0]	LCD Data Bus	Output			
LCDVSYNC	LCD Vertical Synchronization	Output			
LCDHSYNC	LCD Horizontal Synchronization	Output			
LCDPCK	LCD pixel Clock	Output			
LCDDEN	LCD Data Enable	Output			
LCDPWM	LCDPWM for Contrast Control	Output			
LCDDISP	LCD Display ON/OFF	Output			
Image Sensor Interface - ISI					
ISI_D[11..0]	Image Sensor Data	Input			
ISI_HSYNC	Image Sensor Horizontal Synchro	input			
ISI_VSYNC	Image Sensor Vertical Synchro	input			
ISI_PCK	Image Sensor Data clock	input			
Touch Screen Analog-to-Digital Converter - ADC					
$AD0_{UL}$	Upper Left Touch Panel	Analog			
$AD1_{UR}$	Upper Right Touch Panel	Analog			
$AD2_{LL}$	Lower Left Touch Panel	Analog			
$AD3_{LR}$	Lower Right Touch Panel	Analog			
$AD4_{PI}$	Panel Input	Analog			
AD5-AD11	7 Analog Inputs	Analog			
ADTRG	ADC Trigger	Input			
ADVREF	ADC Reference	Analog			

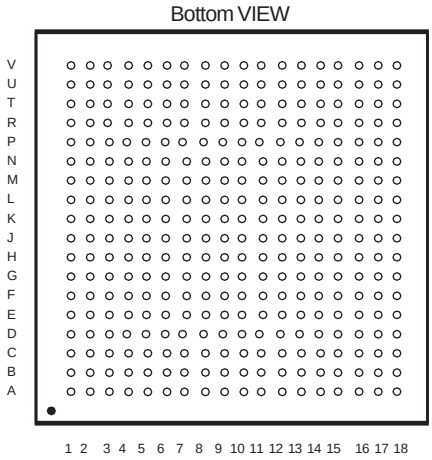
4. Package and Pinout

The SAMA5D3 product is available in a 324-ball LFBGA package.

4.1 Mechanical Overview of the 324-ball LFBGA Package

Figure 4-1 shows the orientation of the 324-ball BGA Package.

Figure 4-1. Orientation of the 324-ball LFBGA Package



4.2 324-ball LFBGA Package Pinout

Table 4-1. SAMA5D3 Pinout for 324-ball LFBGA Package

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Pin	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
E3	VDDIOP0	GPIO	PA0	I/O			LCDDAT0	O					PIO, I, PU, ST
F5	VDDIOP0	GPIO	PA1	I/O			LCDDAT1	O					PIO, I, PU, ST
D2	VDDIOP0	GPIO	PA2	I/O			LCDDAT2	O					PIO, I, PU, ST
F4	VDDIOP0	GPIO	PA3	I/O			LCDDAT3	O					PIO, I, PU, ST
D1	VDDIOP0	GPIO	PA4	I/O			LCDDAT4	O					PIO, I, PU, ST
J10	VDDIOP0	GPIO	PA5	I/O			LCDDAT5	O					PIO, I, PU, ST
G4	VDDIOP0	GPIO	PA6	I/O			LCDDAT6	O					PIO, I, PU, ST
J9	VDDIOP0	GPIO	PA7	I/O			LCDDAT7	O					PIO, I, PU, ST
F3	VDDIOP0	GPIO	PA8	I/O			LCDDAT8	O					PIO, I, PU, ST
J8	VDDIOP0	GPIO	PA9	I/O			LCDDAT9	O					PIO, I, PU, ST
E2	VDDIOP0	GPIO	PA10	I/O			LCDDAT10	O					PIO, I, PU, ST
K8	VDDIOP0	GPIO	PA11	I/O			LCDDAT11	O					PIO, I, PU, ST
F2	VDDIOP0	GPIO	PA12	I/O			LCDDAT12	O					PIO, I, PU, ST
G6	VDDIOP0	GPIO	PA13	I/O			LCDDAT13	O					PIO, I, PU, ST
E1	VDDIOP0	GPIO	PA14	I/O			LCDDAT14	O					PIO, I, PU, ST
H5	VDDIOP0	GPIO	PA15	I/O			LCDDAT15	O					PIO, I, PU, ST
H3	VDDIOP0	GPIO	PA16	I/O			LCDDAT16	O			ISI_D0	I	PIO, I, PU, ST
H6	VDDIOP0	GPIO	PA17	I/O			LCDDAT17	O			ISI_D1	I	PIO, I, PU, ST
H4	VDDIOP0	GPIO	PA18	I/O			LCDDAT18	O	TWD2	I/O	ISI_D2	I	PIO, I, PU, ST
H7	VDDIOP0	GPIO	PA19	I/O			LCDDAT19	O	TWCK2	O	ISI_D3	I	PIO, I, PU, ST
H2	VDDIOP0	GPIO	PA20	I/O			LCDDAT20	O	PWMH0	O	ISI_D4	I	PIO, I, PU, ST
J6	VDDIOP0	GPIO	PA21	I/O			LCDDAT21	O	PWML0	O	ISI_D5	I	PIO, I, PU, ST
G2	VDDIOP0	GPIO	PA22	I/O			LCDDAT22	O	PWMH1	O	ISI_D6	I	PIO, I, PU, ST
J5	VDDIOP0	GPIO	PA23	I/O			LCDDAT23	O	PWML1	O	ISI_D7	I	PIO, I, PU, ST
F1	VDDIOP0	GPIO	PA24	I/O			LCDPWM	O					PIO, I, PU, ST
J4	VDDIOP0	GPIO	PA25	I/O			LCDDISP	O					PIO, I, PU, ST
G3	VDDIOP0	GPIO	PA26	I/O			LCDVSYNC	O					PIO, I, PU, ST
J3	VDDIOP0	GPIO	PA27	I/O			LCDHSYNC	O					PIO, I, PU, ST
G1	VDDIOP0	GPIO_CLK2	PA28	I/O			LCDPCK	O					PIO, I, PU, ST
K4	VDDIOP0	GPIO	PA29	I/O			LCDDEN	O					PIO, I, PU, ST
H1	VDDIOP0	GPIO	PA30	I/O			TWD0	I/O	URXD1	I	ISI_VSYNC	I	PIO, I, PU, ST
K3	VDDIOP0	GPIO	PA31	I/O			TWCK0	O	UTXD1	O	ISI_HSYNC	I	PIO, I, PU, ST
T2	VDDIOP1	GMAC	PB0	I/O			GTX0	O	PWMH0	O			PIO, I, PU, ST
N7	VDDIOP1	GMAC	PB1	I/O			GTX1	O	PWML0	O			PIO, I, PU, ST
T3	VDDIOP1	GMAC	PB2	I/O			GTX2	O	TK1	I/O			PIO, I, PU, ST
N6	VDDIOP1	GMAC	PB3	I/O			GTX3	O	TF1	I/O			PIO, I, PU, ST
P5	VDDIOP1	GMAC	PB4	I/O			GRX0	I	PWMH1	O			PIO, I, PU, ST
T4	VDDIOP1	GMAC	PB5	I/O			GRX1	I	PWML1	O			PIO, I, PU, ST
R4	VDDIOP1	GMAC	PB6	I/O			GRX2	I	TD1	O			PIO, I, PU, ST
U1	VDDIOP1	GMAC	PB7	I/O			GRX3	I	RK1	I			PIO, I, PU, ST
R5	VDDIOP1	GMAC	PB8	I/O			GTXCK	I	PWMH2	O			PIO, I, PU, ST
P3	VDDIOP1	GMAC	PB9	I/O			GTXEN	O	PWML2	O			PIO, I, PU, ST

Table 4-1. SAMA5D3 Pinout for 324-ball LFBGA Package (Continued)

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Pin	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
R6	VDDIOP1	GMAC	PB10	I/O			GTXER	O	RF1	I/O			PIO, I, PU, ST
V3	VDDIOP1	GMAC	PB11	I/O			GRXCK	I	RD1	I			PIO, I, PU, ST
P6	VDDIOP1	GMAC	PB12	I/O			GRXDV	I	PWMH3	O			PIO, I, PU, ST
V1	VDDIOP1	GMAC	PB13	I/O			GRXER	I	PWML3	O			PIO, I, PU, ST
R7	VDDIOP1	GMAC	PB14	I/O			GCRS	I	CANRX1	I			PIO, I, PU, ST
U3	VDDIOP1	GMAC	PB15	I/O			GCOL	I	CANTX1	O			PIO, I, PU, ST
P7	VDDIOP1	GMAC	PB16	I/O			GMDC	O					PIO, I, PU, ST
V2	VDDIOP1	GMAC	PB17	I/O			GMDIO	I/O					PIO, I, PU, ST
V5	VDDIOP1	GMAC	PB18	I/O			G125CK	I					PIO, I, PU, ST
T6	VDDIOP1	GMAC	PB19	I/O			MCI1_CDA	I/O	GTX4	O			PIO, I, PU, ST
N8	VDDIOP1	GMAC	PB20	I/O			MCI1_DA0	I/O	GTX5	O			PIO, I, PU, ST
U4	VDDIOP1	GMAC	PB21	I/O			MCI1_DA1	I/O	GTX6	O			PIO, I, PU, ST
M7	VDDIOP1	GMAC	PB22	I/O			MCI1_DA2	I/O	GTX7	O			PIO, I, PU, ST
U5	VDDIOP1	GMAC	PB23	I/O			MCI1_DA3	I/O	GRX4	I			PIO, I, PU, ST
M8	VDDIOP1	GMAC	PB24	I/O			MCI1_CK	I/O	GRX5	I			PIO, I, PU, ST
T5	VDDIOP1	GMAC	PB25	I/O			SCK1	I/O	GRX6	I			PIO, I, PU, ST
N9	VDDIOP1	GMAC	PB26	I/O			CTS1	I	GRX7	I			PIO, I, PU, ST
V4	VDDIOP1	GPIO	PB27	I/O			RTS1	O	G125CKO	O			PIO, I, PU, ST
M9	VDDIOP1	GPIO	PB28	I/O			RXD1	I					PIO, I, PU, ST
P8	VDDIOP1	GPIO	PB29	I/O			TXD1	O					PIO, I, PU, ST
M10	VDDIOP0	GPIO	PB30	I/O			DRXD	I					PIO, I, PU, ST
R9	VDDIOP0	GPIO	PB31	I/O			DTXD	O					PIO, I, PU, ST
D8	VDDIOP0	GPIO	PC0	I/O			ETX0	O	TIOA3	I/O			PIO, I, PU, ST
A4	VDDIOP0	GPIO	PC1	I/O			ETX1	O	TIOB3	I/O			PIO, I, PU, ST
E8	VDDIOP0	GPIO	PC2	I/O			ERX0	I	TCLK3	I			PIO, I, PU, ST
A3	VDDIOP0	GPIO	PC3	I/O			ERX1	I	TIOA4	I/O			PIO, I, PU, ST
A2	VDDIOP0	GPIO	PC4	I/O			ETXEN	O	TIOB4	I/O			PIO, I, PU, ST
F8	VDDIOP0	GPIO	PC5	I/O			ECRSDV	I	TCLK4	I			PIO, I, PU, ST
B3	VDDIOP0	GPIO	PC6	I/O			ERXER	I	TIOA5	I/O			PIO, I, PU, ST
G8	VDDIOP0	GPIO	PC7	I/O			EREFCK	I	TIOB5	I/O			PIO, I, PU, ST
B4	VDDIOP0	GPIO	PC8	I/O			EMDC	O	TCLK5	I			PIO, I, PU, ST
F7	VDDIOP0	GPIO	PC9	I/O			EMDIO	I/O					PIO, I, PU, ST
A1	VDDIOP0	GPIO	PC10	I/O			MCI2_CDA	I/O			LCDDAT20	O	PIO, I, PU, ST
D7	VDDIOP0	GPIO	PC11	I/O			MCI2_DA0	I/O			LCDDAT19	O	PIO, I, PU, ST
C6	VDDIOP0	GPIO	PC12	I/O			MCI2_DA1	I/O	TIOA1	I/O	LCDDAT18	O	PIO, I, PU, ST
E7	VDDIOP0	GPIO	PC13	I/O			MCI2_DA2	I/O	TIOB1	I/O	LCDDAT17	O	PIO, I, PU, ST
B2	VDDIOP0	GPIO	PC14	I/O			MCI2_DA3	I/O	TCLK1	I	LCDDAT16	O	PIO, I, PU, ST
F6	VDDIOP0	MCI_CLK	PC15	I/O			MCI2_CK	I/O	PCK2	O	LCDDAT21	O	PIO, I, PU, ST
B1	VDDIOP0	GPIO	PC16	I/O			TK0	I/O					PIO, I, PU, ST
E6	VDDIOP0	GPIO	PC17	I/O			TF0	I/O					PIO, I, PU, ST
C3	VDDIOP0	GPIO	PC18	I/O			TD0	O					PIO, I, PU, ST
D6	VDDIOP0	GPIO	PC19	I/O			RK0	I/O					PIO, I, PU, ST
C4	VDDIOP0	GPIO	PC20	I/O			RF0	I/O					PIO, I, PU, ST
D5	VDDIOP0	GPIO	PC21	I/O			RD0	I					PIO, I, PU, ST

Table 4-1. SAMA5D3 Pinout for 324-ball LFBGA Package (Continued)

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Pin	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
C2	VDDIOP0	GPIO	PC22	I/O			SPI1_MISO	I/O					PIO, I, PU, ST
G9	VDDIOP0	GPIO	PC23	I/O			SPI1_MOSI	I/O					PIO, I, PU, ST
C1	VDDIOP0	GPIO_CLK	PC24	I/O			SPI1_SPCK	I/O					PIO, I, PU, ST
H10	VDDIOP0	GPIO	PC25	I/O			SPI1_NPCS0	I/O					PIO, I, PU, ST
H9	VDDIOP0	GPIO	PC26	I/O			SPI1_NPCS1	O	TWD1	I/O	ISI_D11	I	PIO, I, PU, ST
D4	VDDIOP0	GPIO	PC27	I/O			SPI1_NPCS2	O	TWCK1	O	ISI_D10	I	PIO, I, PU, ST
H8	VDDIOP0	GPIO	PC28	I/O			SPI1_NPCS3	O	PWMFI0	I	ISI_D9	I	PIO, I, PU, ST
G5	VDDIOP0	GPIO	PC29	I/O			URXD0	I	PWMFI2	I	ISI_D8	I	PIO, I, PU, ST
D3	VDDIOP0	GPIO	PC30	I/O			UTXD0	O			ISI_PCK	O	PIO, I, PU, ST
E4	VDDIOP0	GPIO	PC31	I/O			FIQ	I	PWMFI1	I			PIO, I, PU, ST
K5	VDDIOP1	GPIO	PD0	I/O			MCI0_CDA	I/O					PIO, I, PU, ST
P1	VDDIOP1	GPIO	PD1	I/O			MCI0_DA0	I/O					PIO, I, PU, ST
K6	VDDIOP1	GPIO	PD2	I/O			MCI0_DA1	I/O					PIO, I, PU, ST
R1	VDDIOP1	GPIO	PD3	I/O			MCI0_DA2	I/O					PIO, I, PU, ST
L7	VDDIOP1	GPIO	PD4	I/O			MCI0_DA3	I/O					PIO, I, PU, ST
P2	VDDIOP1	GPIO	PD5	I/O			MCI0_DA4	I/O	TIOA0	I/O	PWMH2	O	PIO, I, PU, ST
L8	VDDIOP1	GPIO	PD6	I/O			MCI0_DA5	I/O	TIOB0	I/O	PWML2	O	PIO, I, PU, ST
R2	VDDIOP1	GPIO	PD7	I/O			MCI0_DA6	I/O	TCLK0	I	PWMH3	O	PIO, I, PU, ST
K7	VDDIOP1	GPIO	PD8	I/O			MCI0_DA7	I/O			PWML3	O	PIO, I, PU, ST
U2	VDDIOP1	MCI_CLK	PD9	I/O			MCI0_CK	I/O					PIO, I, PU, ST
K9	VDDIOP1	GPIO	PD10	I/O			SPI0_MISO	I/O					PIO, I, PU, ST
M5	VDDIOP1	GPIO	PD11	I/O			SPI0_MOSI	I/O					PIO, I, PU, ST
K10	VDDIOP1	GPIO_CLK	PD12	I/O			SPI0_SPCK	I/O					PIO, I, PU, ST
N4	VDDIOP1	GPIO	PD13	I/O			SPI0_NPCS0	I/O					PIO, I, PU, ST
L9	VDDIOP1	GPIO	PD14	I/O			SCK0	I/O	SPI0_NPCS1	O	CANRX0	I	PIO, I, PU, ST
N3	VDDIOP1	GPIO	PD15	I/O			CTS0	I	SPI0_NPCS2	O	CANTX0	O	PIO, I, PU, ST
L10	VDDIOP1	GPIO	PD16	I/O			RTS0	O	SPI0_NPCS3	O	PWMFI3	I	PIO, I, PU, ST
N5	VDDIOP1	GPIO	PD17	I/O			RXD0	I					PIO, I, PU, ST
M6	VDDIOP1	GPIO	PD18	I/O			TXD0	O					PIO, I, PU, ST
T1	VDDIOP1	GPIO	PD19	I/O			ADTRG	I					PIO, I, PU, ST
N2	VDDANA	GPIO_ANA	PD20	I/O			AD0	I					PIO, I, PU, ST
M3	VDDANA	GPIO_ANA	PD21	I/O			AD1	I					PIO, I, PU, ST
M2	VDDANA	GPIO_ANA	PD22	I/O			AD2	I					PIO, I, PU, ST
L3	VDDANA	GPIO_ANA	PD23	I/O			AD3	I					PIO, I, PU, ST
M1	VDDANA	GPIO_ANA	PD24	I/O			AD4	I					PIO, I, PU, ST
N1	VDDANA	GPIO_ANA	PD25	I/O			AD5	I					PIO, I, PU, ST
L1	VDDANA	GPIO_ANA	PD26	I/O			AD6	I					PIO, I, PU, ST
L2	VDDANA	GPIO_ANA	PD27	I/O			AD7	I					PIO, I, PU, ST
K1	VDDANA	GPIO_ANA	PD28	I/O			AD8	I					PIO, I, PU, ST
K2	VDDANA	GPIO_ANA	PD29	I/O			AD9	I					PIO, I, PU, ST
J1	VDDANA	GPIO_ANA	PD30	I/O			AD10	I	PCK0	O			PIO, I, PU, ST
J2	VDDANA	GPIO_ANA	PD31	I/O			AD11	I	PCK1	O			PIO, I, PU, ST
P13	VDDIOM	EBI	PE0	I/O			A0/NBS0	O					A,I, PD, ST
R14	VDDIOM	EBI	PE1	I/O			A1	O					A,I, PD, ST

Table 4-1. SAMA5D3 Pinout for 324-ball LFBGA Package (Continued)

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Pin	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
R13	VDDIOM	EBI	PE2	I/O			A2	O					A,I, PD, ST
V18	VDDIOM	EBI	PE3	I/O			A3	O					A,I, PD, ST
P14	VDDIOM	EBI	PE4	I/O			A4	O					A,I, PD, ST
U18	VDDIOM	EBI	PE5	I/O			A5	O					A,I, PD, ST
T18	VDDIOM	EBI	PE6	I/O			A6	O					A,I, PD, ST
R15	VDDIOM	EBI	PE7	I/O			A7	O					A,I, PD, ST
P17	VDDIOM	EBI	PE8	I/O			A8	O					A,I, PD, ST
P15	VDDIOM	EBI	PE9	I/O			A9	O					A,I, PD, ST
P18	VDDIOM	EBI	PE10	I/O			A10	O					A,I, PD, ST
R16	VDDIOM	EBI	PE11	I/O			A11	O					A,I, PD, ST
N16	VDDIOM	EBI	PE12	I/O			A12	O					A,I, PD, ST
R17	VDDIOM	EBI	PE13	I/O			A13	O					A,I, PD, ST
N17	VDDIOM	EBI	PE14	I/O			A14	O					A,I, PD, ST
R18	VDDIOM	EBI	PE15	I/O			A15	O	SCK3	I/O			A,I, PD, ST
N18	VDDIOM	EBI	PE16	I/O			A16	O	CTS3	I			A,I, PD, ST
P16	VDDIOM	EBI	PE17	I/O			A17	O	RTS3	O			A,I, PD, ST
M18	VDDIOM	EBI	PE18	I/O			A18	O	RXD3	I			A,I, PD, ST
N15	VDDIOM	EBI	PE19	I/O			A19	O	TXD3	O			A,I, PD, ST
M15	VDDIOM	EBI	PE20	I/O			A20	O	SCK2	I/O			A,I, PD, ST
N14	VDDIOM	EBI	PE21	I/O			A21/NANDALE	O					A,I, PD, ST
M17	VDDIOM	EBI	PE22	I/O			A22/NANDCLE	O					A,I, PD, ST
M13	VDDIOM	EBI	PE23	I/O			A23	O	CTS2	I			A,I, PD, ST
M16	VDDIOM	EBI	PE24	I/O			A24	O	RTS2	O			A,I, PD, ST
N12	VDDIOM	EBI	PE25	I/O			A25	O	RXD2	I			A,I, PD, ST
M14	VDDIOM	EBI	PE26	I/O			NCS0	O	TXD2	O			A,I, PD, ST
M12	VDDIOM	EBI	PE27	I/O			NCS1	O	TIOA2	I/O	LCDDAT22	O	PIO,I, PD, ST
L13	VDDIOM	EBI	PE28	I/O			NCS2	O	TIOB2	I/O	LCDDAT23	O	PIO, I, PD, ST
L15	VDDIOM	EBI	PE29	I/O			NWR1/NBS1	O	TCLK2	I			PIO, I, PD, ST
L14	VDDIOM	EBI	PE30	I/O			NWAIT	I					PIO, I, PD, ST
L16	VDDIOM	EBI	PE31	I/O			IRQ	I	PWML1	O			PIO,I, PD, ST
U15	VDDBU	SYSC	TST	I									I, PD,
U9	VDDIOP0	SYSC	BMS	I									I
U8	VDDIOP0	CLOCK	XIN	I									I
V8	VDDIOP0	CLOCK	XOUT	O									O
U16	VDDBU	CLOCK	XIN32	I									I
V16	VDDBU	CLOCK	XOUT32	O									O
T12	VDDBU	SYSC	SHDN	O									O, PU
T10	VDDBU	SYSC	WKUP	I									I, ST
V9	VDDIOP0	RSTJTAG	NRST	I/O									I, PU, ST
P11	VDDIOP0	RSTJTAG	NTRST	I									I, PU, ST
R8	VDDIOP0	RSTJTAG	TDI	I									I, ST
M11	VDDIOP0	RSTJTAG	TDO	O									O
N10	VDDIOP0	RSTJTAG	TMS	I	SWDIO	I/O							I, ST
P9	VDDIOP0	RSTJTAG	TCK	I	SWCLK	I							I, ST

Table 4-1. SAMA5D3 Pinout for 324-ball LFBGA Package (Continued)

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Pin	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
T9	VDDBU	SYSC	JTAGSEL	I									I, PD
V6	VDDIOP0	DIB	DIBP	O									O, PU
U6	VDDIOP0	DIB	DIBN	O									O, PU
K12	VDDIOM	EBI	D0	I/O									I, PD
K15	VDDIOM	EBI	D1	I/O									I, PD
K14	VDDIOM	EBI	D2	I/O									I, PD
K16	VDDIOM	EBI	D3	I/O									I, PD
K13	VDDIOM	EBI	D4	I/O									I, PD
K17	VDDIOM	EBI	D5	I/O									I, PD
J12	VDDIOM	EBI	D6	I/O									I, PD
K18	VDDIOM	EBI	D7	I/O									I, PD
J14	VDDIOM	EBI	D8	I/O									I, PD
J16	VDDIOM	EBI	D9	I/O									I, PD
J13	VDDIOM	EBI	D10	I/O									I, PD
J17	VDDIOM	EBI	D11	I/O									I, PD
J15	VDDIOM	EBI	D12	I/O									I, PD
J18	VDDIOM	EBI	D13	I/O									I, PD
H16	VDDIOM	EBI	D14	I/O									I, PD
H18	VDDIOM	EBI	D15	I/O									I, PD
L12	VDDIOM	EBI	NCS3/NANDCS	O									O, PU
L18	VDDIOM	EBI	NANDRDY	I									I, PU
L17	VDDIOM	EBI	NRD/NANDOE	O									O, PU
K11	VDDIOM	EBI	NWE/NANDWE	O									O, PU
C13	VDDIODDR		DDR_VREF	I									I
B10	VDDIODDR	DDR_IO	DDR_A0	O									O
C11	VDDIODDR	DDR_IO	DDR_A1	O									O
A9	VDDIODDR	DDR_IO	DDR_A2	O									O
D11	VDDIODDR	DDR_IO	DDR_A3	O									O
B9	VDDIODDR	DDR_IO	DDR_A4	O									O
E10	VDDIODDR	DDR_IO	DDR_A5	O									O
D10	VDDIODDR	DDR_IO	DDR_A6	O									O
A8	VDDIODDR	DDR_IO	DDR_A7	O									O
C10	VDDIODDR	DDR_IO	DDR_A8	O									O
B8	VDDIODDR	DDR_IO	DDR_A9	O									O
F11	VDDIODDR	DDR_IO	DDR_A10	O									O
A7	VDDIODDR	DDR_IO	DDR_A11	O									O
D9	VDDIODDR	DDR_IO	DDR_A12	O									O
A6	VDDIODDR	DDR_IO	DDR_A13	O									O
H12	VDDIODDR	DDR_IO	DDR_D0	I/O									HiZ
H17	VDDIODDR	DDR_IO	DDR_D1	I/O									HiZ
H13	VDDIODDR	DDR_IO	DDR_D2	I/O									HiZ
G17	VDDIODDR	DDR_IO	DDR_D3	I/O									HiZ
G16	VDDIODDR	DDR_IO	DDR_D4	I/O									HiZ
H15	VDDIODDR	DDR_IO	DDR_D5	I/O									HiZ

Table 4-1. SAMA5D3 Pinout for 324-ball LFBGA Package (Continued)

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Pin	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
F17	VDDIODDR	DDR_IO	DDR_D6	I/O									HiZ
G15	VDDIODDR	DDR_IO	DDR_D7	I/O									HiZ
F16	VDDIODDR	DDR_IO	DDR_D8	I/O									HiZ
E17	VDDIODDR	DDR_IO	DDR_D9	I/O									HiZ
G14	VDDIODDR	DDR_IO	DDR_D10	I/O									HiZ
E16	VDDIODDR	DDR_IO	DDR_D11	I/O									HiZ
D17	VDDIODDR	DDR_IO	DDR_D12	I/O									HiZ
C18	VDDIODDR	DDR_IO	DDR_D13	I/O									HiZ
D16	VDDIODDR	DDR_IO	DDR_D14	I/O									HiZ
C17	VDDIODDR	DDR_IO	DDR_D15	I/O									HiZ
B16	VDDIODDR	DDR_IO	DDR_D16	I/O									HiZ
B18	VDDIODDR	DDR_IO	DDR_D17	I/O									HiZ
C15	VDDIODDR	DDR_IO	DDR_D18	I/O									HiZ
A18	VDDIODDR	DDR_IO	DDR_D19	I/O									HiZ
C16	VDDIODDR	DDR_IO	DDR_D20	I/O									HiZ
C14	VDDIODDR	DDR_IO	DDR_D21	I/O									HiZ
D15	VDDIODDR	DDR_IO	DDR_D22	I/O									HiZ
B14	VDDIODDR	DDR_IO	DDR_D23	I/O									HiZ
A15	VDDIODDR	DDR_IO	DDR_D24	I/O									HiZ
A14	VDDIODDR	DDR_IO	DDR_D25	I/O									HiZ
E12	VDDIODDR	DDR_IO	DDR_D26	I/O									HiZ
A11	VDDIODDR	DDR_IO	DDR_D27	I/O									HiZ
B11	VDDIODDR	DDR_IO	DDR_D28	I/O									HiZ
F12	VDDIODDR	DDR_IO	DDR_D29	I/O									HiZ
A10	VDDIODDR	DDR_IO	DDR_D30	I/O									HiZ
E11	VDDIODDR	DDR_IO	DDR_D31	I/O									HiZ
G12	VDDIODDR	DDR_IO	DDR_DQM0	O									O
E15	VDDIODDR	DDR_IO	DDR_DQM1	O									O
B15	VDDIODDR	DDR_IO	DDR_DQM2	O									O
D12	VDDIODDR	DDR_IO	DDR_DQM3	O									O
E18	VDDIODDR	DDR_IO	DDR_DQS0	I/O									I, PD
G18	VDDIODDR	DDR_IO	DDR_DQS1	I/O									I, PD
B17	VDDIODDR	DDR_IO	DDR_DQS2	I/O									I, PD
B13	VDDIODDR	DDR_IO	DDR_DQS3	I/O									I, PD
D18	VDDIODDR	DDR_IO	DDR_DQSN0	I/O									I, PU
F18	VDDIODDR	DDR_IO	DDR_DQSN1	I/O									I, PU
A17	VDDIODDR	DDR_IO	DDR_DQSN2	I/O									I, PU
A13	VDDIODDR	DDR_IO	DDR_DQSN3	I/O									I, PU
C8	VDDIODDR	DDR_IO	DDR_CS	O									O
B12	VDDIODDR	DDR_IO	DDR_CLK	O									O
A12	VDDIODDR	DDR_IO	DDR_CLKN	O									O
B7	VDDIODDR	DDR_IO	DDR_CKE	O									O
C12	VDDIODDR	DDR_IO	DDR_CALN	I									O
E13	VDDIODDR	DDR_IO	DDR_CALP	I									O

Table 4-1. SAMA5D3 Pinout for 324-ball LFBGA Package (Continued)

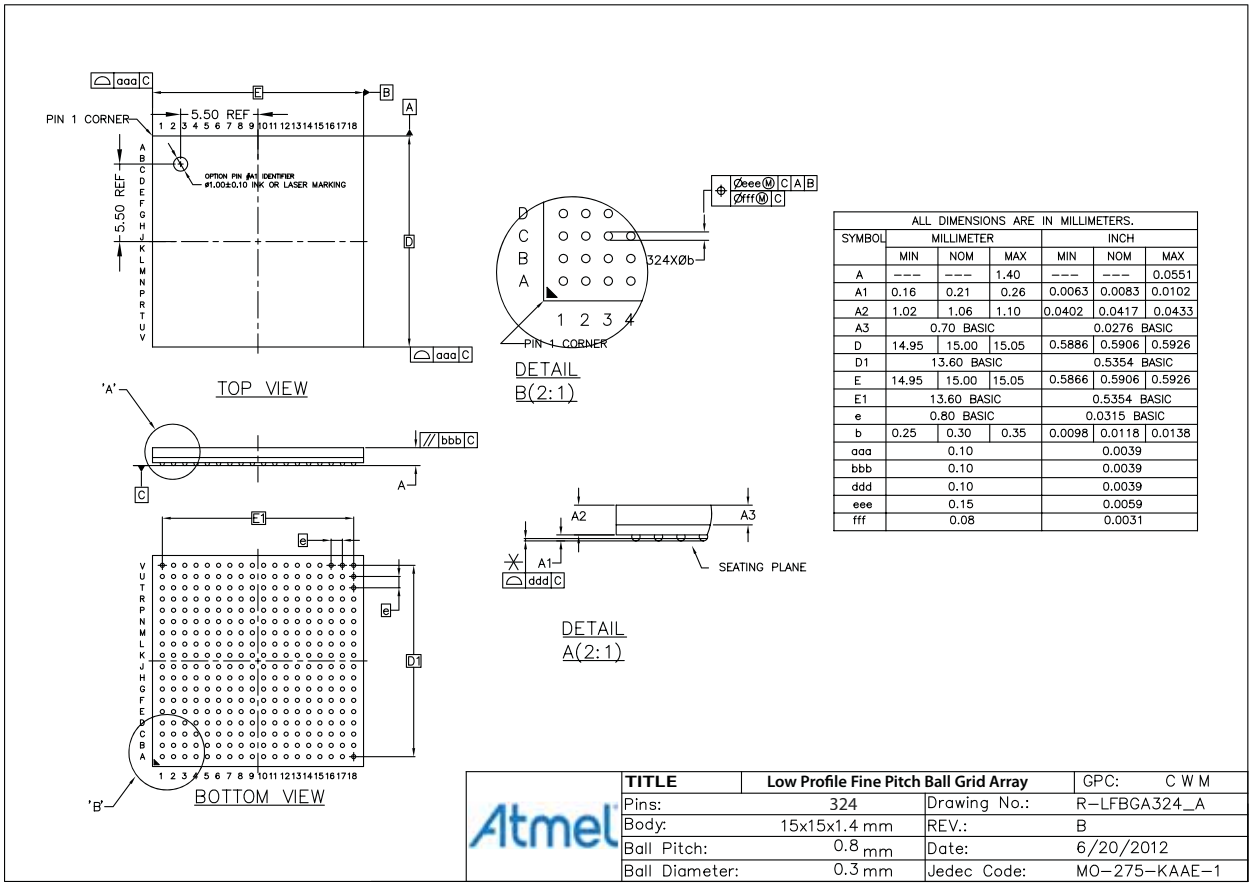
			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Pin	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
G11	VDDIODDR	DDR_IO	DDR_RAS	O									O
A5	VDDIODDR	DDR_IO	DDR_CAS	O									O
B5	VDDIODDR	DDR_IO	DDR_WE	O									O
E9	VDDIODDR	DDR_IO	DDR_BA0	O									O
B6	VDDIODDR	DDR_IO	DDR_BA1	O									O
F9	VDDIODDR	DDR_IO	DDR_BA2	O									O
R11	VBG	VBG	VBG	I									I
U14	VDDUTMII	USBHS	HHSDPC	I/O									O, PD
V14	VDDUTMII	USBHS	HHSDMC	I/O									O, PD
U12	VDDUTMII	USBHS	HHSDPB	I/O									O, PD
V12	VDDUTMII	USBHS	HHSDMB	I/O									O, PD
U10	VDDUTMII	USBHS	HHSDPA	I/O	DHSDP								O, PD
V10	VDDUTMII	USBHS	HHSDMA	I/O	DHSDM								O, PD
V15	VDDBU	power supply	VDDBU	I									I
T13	GNDBU	ground	GNDBU	I									I
C5, C7, D14, T15, T7, U17, V7	VDDCORE	power supply	VDDCORE	I									I
A16, C9, N13, T14, T8, V17	GNDCORE	ground	GNDCORE	I									I
D13, F14, G10, G13, H11	VDDIODDR	power supply	VDDIODDR	I									I
E14, F10, F13, F15, H14	GNDIODDR	ground	GNDIODDR	I									I
P12, T16	VDDIOM	power supply	VDDIOM	I									I
J11, T17	GNDIOM	ground	GNDIOM	I									I
G7, V11	VDDIOP0	power supply	VDDIOP0	I									I
L11, M4	VDDIOP1	power supply	VDDIOP1	I									I
E5, J7, N11, U7	GNDIOP	ground	GNDIOP	I									I
V13	VDDUTMIC	power supply	VDDUTMIC	I									I
U13	VDDUTMII	power supply	VDDUTMII	I									I
R12	GNDUTMI	ground	GNDUTMI	I									I
R10	VDDPLLA	power supply	VDDPLLA	I									I
P10	GNDPLL	ground	GNDPLL	I									I
U11	VDDOSC	power supply	VDDOSC	I									I
T11	GNDOSC	ground	GNDOSC	I									I

Table 4-1. SAMA5D3 Pinout for 324-ball LFBGA Package (Continued)

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Pin	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
L6	VDDANA	power supply	VDDANA	I									I
L4	GNDANA	ground	GNDANA	I									I
L5	VDDANA	power supply	ADVREF	I									I
R3	VDDFUSE	power supply	VDDFUSE	I									I
P4	GNDFUSE	ground	GNDFUSE	I									I

5. Mechanical Characteristics

Figure 5-1. 324-ball LFBGA Package Drawing



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.0551
A1	0.16	0.21	0.26	0.0063	0.0083	0.0102
A2	1.02	1.06	1.10	0.0402	0.0417	0.0433
A3	0.70 BASIC			0.0276 BASIC		
D	14.95	15.00	15.05	0.5886	0.5906	0.5926
D1	13.60 BASIC			0.5354 BASIC		
E	14.95	15.00	15.05	0.5866	0.5906	0.5926
E1	13.60 BASIC			0.5354 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.25	0.30	0.35	0.0098	0.0118	0.0138
aaa	0.10			0.0039		
bbb	0.10			0.0039		
ddd	0.10			0.0039		
eee	0.15			0.0059		
fff	0.08			0.0031		

Table 5-1. 324-ball LFBGA Package Characteristics

Moisture Sensitivity Level	3

Table 5-2. Device and 324-ball LFBGA Package Maximum Weight

400	mg

Table 5-3. Package Reference

JEDEC Drawing Reference	MO-275-KAAE-1
JESD97 Classification	e8

Table 5-4. Package Information

Ball Land	0.350 mm ± 0.05
Solder Mask Opening	0.275 mm ± 0.05
Solder Mask Definition	SMD

6. SAMA5D3 Ordering Information

Table 6-1. SAMA5D3 Ordering Information

Ordering Code	Package	Package Type	Temperature Operating Range
ATSAMA5D31A-CU	BGA324	Green	Industrial -40°C to 85°C
ATSAMA5D33A-CU	BGA324	Green	Industrial -40°C to 85°C
ATSAMA5D34A-CU	BGA324	Green	Industrial -40°C to 85°C
ATSAMA5D35A-CU	BGA324	Green	Industrial -40°C to 85°C

Revision History

In the table that follows, the most recent version of the document appears first.

“rfo” indicates changes requested during the document review and approval loop.

Table 6-2.

Doc. Rev	Comments	Change Request Ref.
11121AS	First issue	

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