

Schottky Power Rectifier, Switch-Mode, 10 A, 45 V

MBRB1045G, MBRD1045G, SBRB1045G, SBRD81045T4G

This series of Power Rectifiers employs the Schottky Barrier principle in a large metal-to-silicon power diode. State-of-the-art geometry features epitaxial construction with oxide passivation and metal overlay contact. Ideally suited for use in low voltage, high frequency switching power supplies, free wheeling diodes, and polarity protection diodes.

Features

- Guardring for Stress Protection
- Low Forward Voltage
- 175°C Operating Junction Temperature
- Epoxy Meets UL 94 V-0 @ 0.125 in
- Short Heat Sink Tab Manufactured – Not Sheared!
- SBRB and SBRD8 Prefixes for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Mechanical Characteristics:

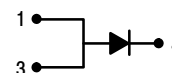
- Case: Epoxy, Molded, Epoxy Meets UL 94 V-0
- Weight: 1.7 grams for D²PAK (approximately)
0.4 grams for DPAK (approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead and Mounting Surface Temperature for Soldering Purposes: 260°C Max. for 10 Seconds
- Device Meets MSL1 Requirements
- ESD Ratings:
 - ◆ Machine Model = C (> 400 V)
 - ◆ Human Body Model = 3B (> 8000 V)



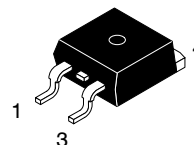
ON Semiconductor®

www.onsemi.com

SCHOTTKY BARRIER RECTIFIER 10 AMPERES, 45 VOLTS



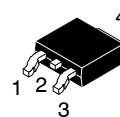
MARKING DIAGRAM



D²PAK-3
CASE 418B

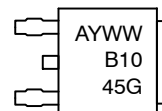


A = Assembly Location
Y = Year
WW = Work Week
MBRB1045 = Device Code
G = Pb-Free Package
AKA = Diode Polarity



DPAK
CASE 369C

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
B1045 = Device Code
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MBRB1045G, MBRD1045G, SBRB1045G, SBRD81045T4G

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	45	V
Average Rectified Forward Current, $T_C = 135^\circ\text{C}$	$I_{F(AV)}$	10	A
Peak Repetitive Forward Current (Square Wave, Duty = 0.5) $T_C = 135^\circ\text{C}$	I_{FRM}	20	A
Nonrepetitive Peak Surge Current (Surge applied at rated load conditions halfwave, single phase, 60 Hz)	I_{FSM}	150 (MBRB/SBRB) 70 (MBRD/SBRD)	A
Operating Junction and Storage Temperature Range (Note 1)	T_J, T_{stg}	-65 to +175	$^\circ\text{C}$
Voltage Rate of Change (Rated V_R)	dv/dt	10000	$\text{V}/\mu\text{s}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The heat generated must be less than the thermal conductivity from Junction-to-Ambient: $dP_D/dT_J < 1/R_{\theta JA}$.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, (MBRB1045G) Junction-to-Case (Note 2) Junction-to-Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$	1.0 50	$^\circ\text{C}/\text{W}$
(MBRD1045G) Junction-to-Case (Note 2) Junction-to-Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$	2.43 68	

2. When mounted using minimum recommended pad size on FR-4 board.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Maximum Instantaneous Forward Voltage (Note 3) ($I_F = 10$ Amps, $T_J = 125^\circ\text{C}$) ($I_F = 20$ Amps, $T_J = 125^\circ\text{C}$) ($I_F = 20$ Amps, $T_J = 25^\circ\text{C}$)	V_F	0.57 0.72 0.84	V
Maximum Instantaneous Reverse Current (Note 3) (Rated dc Voltage, $T_J = 125^\circ\text{C}$) (Rated dc Voltage, $T_J = 25^\circ\text{C}$)	I_R	15 0.1	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2.0\%$

ORDERING INFORMATION

Device	Package	Shipping†
MBRB1045G	D ² PAK-3 (Pb-Free)	50 Units / Rail
SBRB1045G		50 Units / Rail
MBRB1045T4G		800 Units / Tape & Reel
SBRB1045T4G		800 Units / Tape & Reel
MBRD1045G	DPAK (Pb-Free)	50 Units / Rail
MBRD1045T4G		2,500 Units / Tape & Reel
SBRD81045T4G		2,500 Units / Tape & Reel
SSBRD81045T4G		2,500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MBRB1045G, MBRD1045G, SBRB1045G, SBRD81045T4G

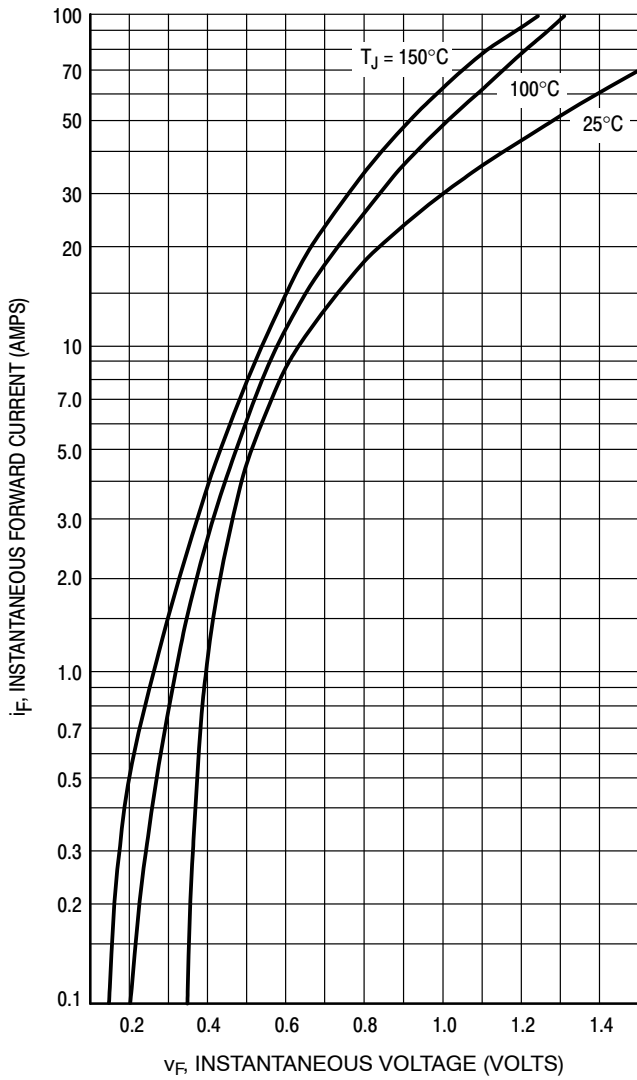


Figure 1. Maximum Forward Voltage

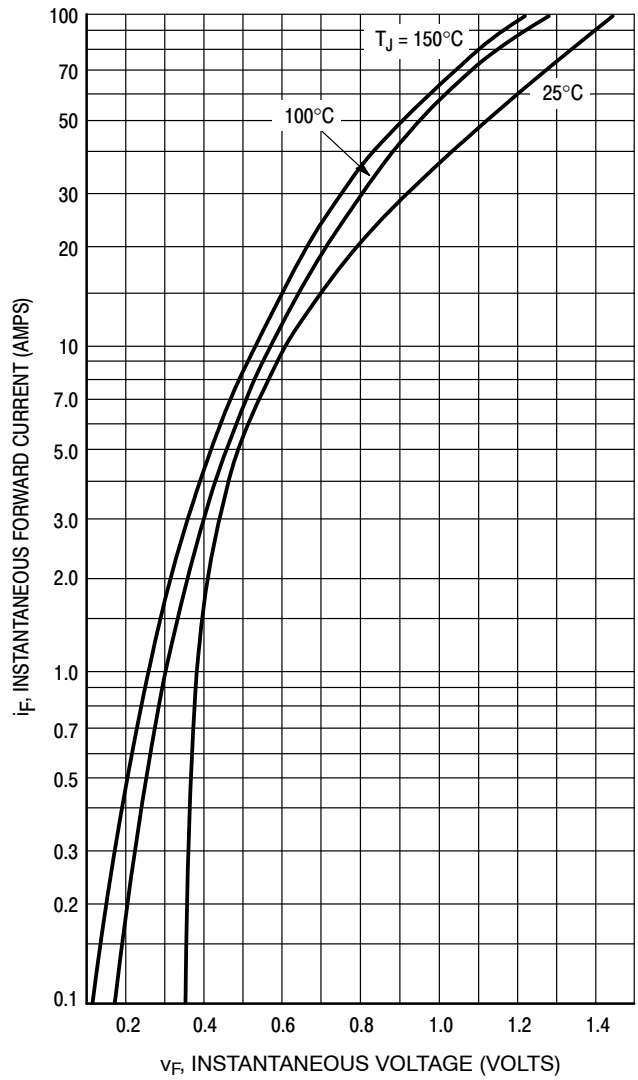


Figure 2. Typical Forward Voltage

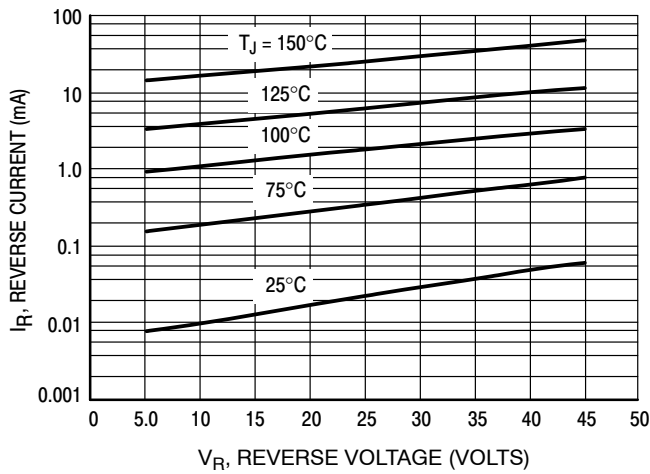


Figure 3. Maximum Reverse Current

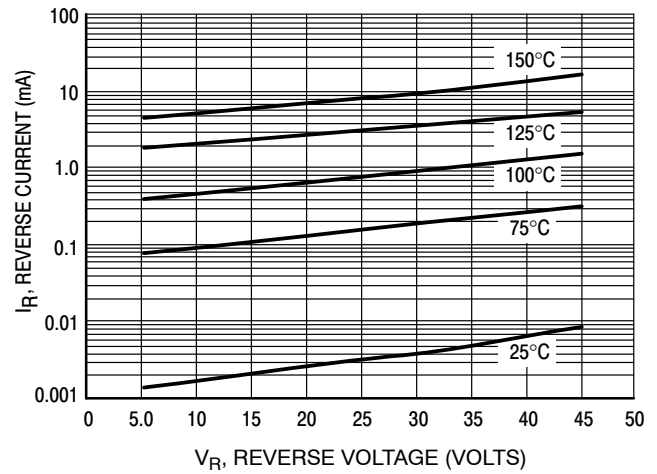


Figure 4. Typical Reverse Current

MBRB1045G, MBRD1045G, SBRB1045G, SBRD81045T4G

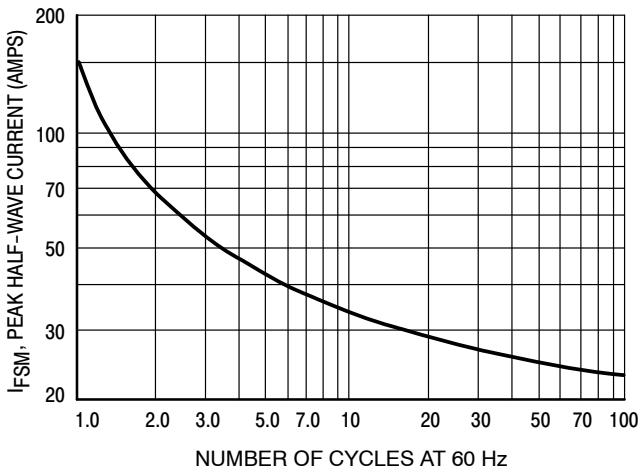


Figure 8. Maximum Surge Capability

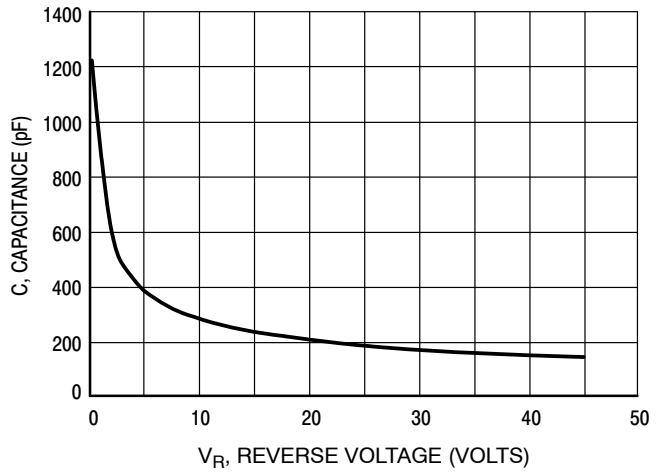
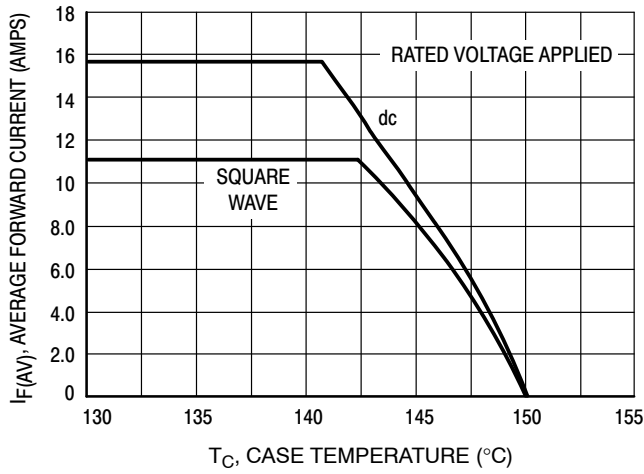


Figure 5. Typical Capacitance



**Figure 6. Current Derating, Case,
 $R_{\theta JC} = 1.0 \text{ } ^\circ\text{C/W}$**

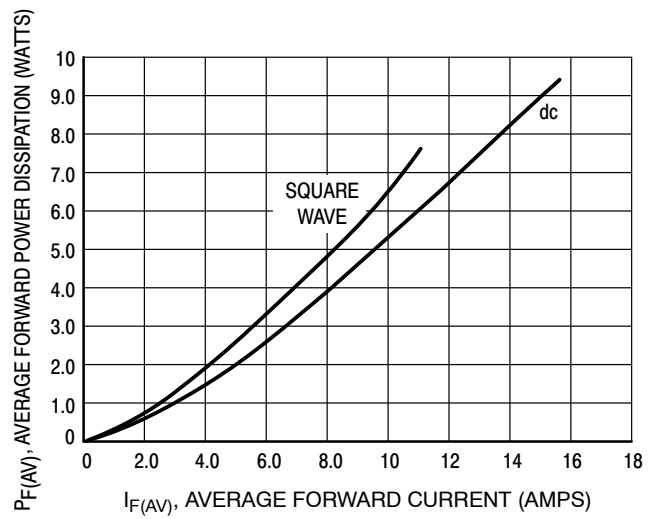
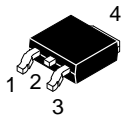


Figure 7. Forward Power Dissipation

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



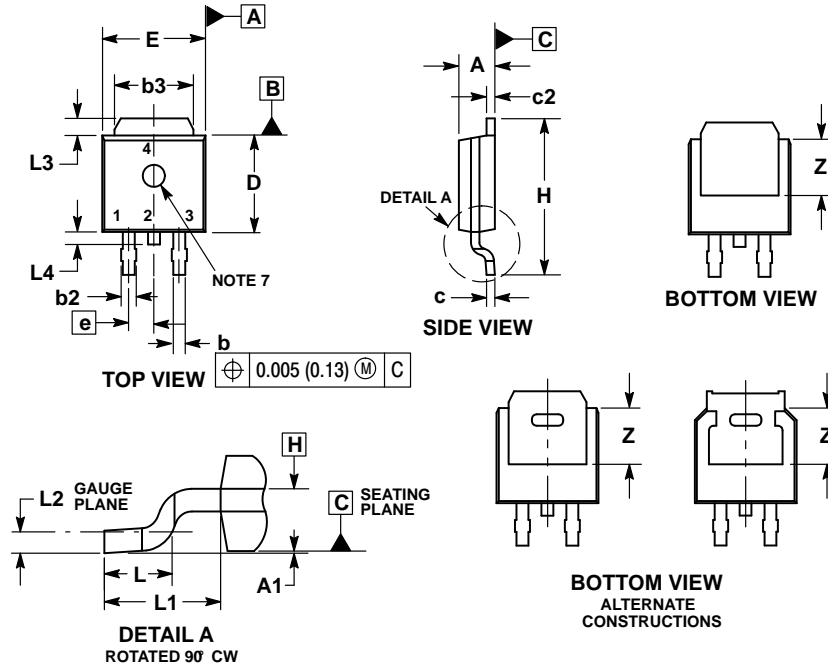
SCALE 1:1

DPAK (SINGLE GAUGE)

CASE 369C

ISSUE F

DATE 21 JUL 2015

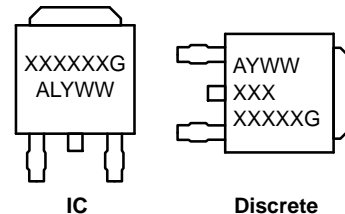


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

GENERIC MARKING DIAGRAM*

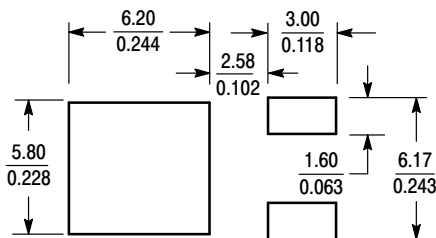


- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

- | | | | | |
|--|--|---|---|--|
| <p>STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN</p> | <p>STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE</p> | <p>STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE</p> |
| <p>STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2</p> | <p>STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE</p> | <p>STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE</p> |

SOLDERING FOOTPRINT*




SCALE 3:1 (mm / inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:	REF TO JEDEC TO-252	
DESCRIPTION:	DPAK SINGLE GAUGE SURFACE MOUNT	PAGE 1 OF 2



ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY L. GAN	24 SEP 2001
A	ADDED STYLE 8. REQ. BY S. ALLEN.	06 AUG 2008
B	ADDED STYLE 9. REQ. BY D. WARNER.	16 JAN 2009
C	ADDED STYLE 10. REQ. BY S. ALLEN.	09 JUN 2009
D	RELABELED DRAWING TO JEDEC STANDARDS. ADDED SIDE VIEW DETAIL A. CORRECTED MARKING INFORMATION. REQ. BY D. TRUHITE.	29 JUN 2010
E	ADDED ALTERNATE CONSTRUCTION BOTTOM VIEW. MODIFIED DIMENSIONS b2 AND L1. CORRECTED MARKING DIAGRAM FOR DISCRETE. REQ. BY I. CAMBALIZA.	06 FEB 2014
F	ADDED SECOND ALTERNATE CONSTRUCTION BOTTOM VIEW. REQ. BY K. MUSTAFA.	21 JUL 2015

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

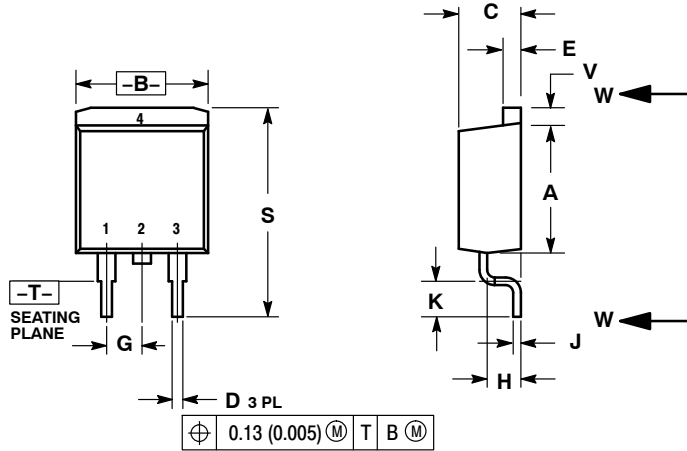
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D²PAK 3
CASE 418B-04
ISSUE L

DATE 17 FEB 2015

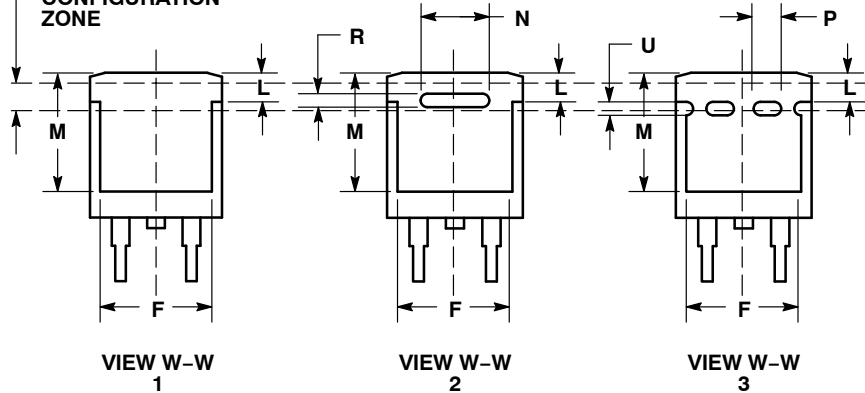
SCALE 1:1



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: INCH.
 - 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

VARIABLE CONFIGURATION ZONE



- | | | | | | |
|---|--|--|---|--|---|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE | STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE | STYLE 6:
PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE |
|---|--|--|---|--|---|

MARKING INFORMATION AND FOOTPRINT ON PAGE 2

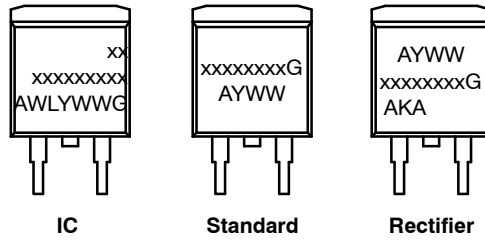
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D²PAK 3
CASE 418B-04
ISSUE L

DATE 17 FEB 2015

**GENERIC
MARKING DIAGRAM***



- xx = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package
- AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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