

PRELIMINARY - January 17, 2000

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

DESCRIPTION

The SC1545 was designed for instantly available motherboard applications. As part of the Semtech family of SmartLDO's it provides additional control functions not available in a standard LDO.

The device provides the capability to control three separate supplies. There is an on-board 500mA, 2.5V LDO with current limit protection, and drive pins for an N-channel MOSFET and a P-channel MOSFET. Internal logic circuitry ensures that the system starts up in a controlled manner, and that the correct outputs are enabled during specific sequences of BF_CUT and SLP.

The LDO draws its power from the 5V standby supply, and the N-channel MOSFET drive is derived from the 12V supply.

The SC1545 is available in the surface mount SO-8 package.

FEATURES

- 500mA LDO with Over Current Protection (OCP)
- $\pm 2.5\%$ LDO regulation over line, load and temperature
- Power sequencing for three supplies

APPLICATIONS

- Instantly available motherboards
- Embedded systems
- Desktop computers

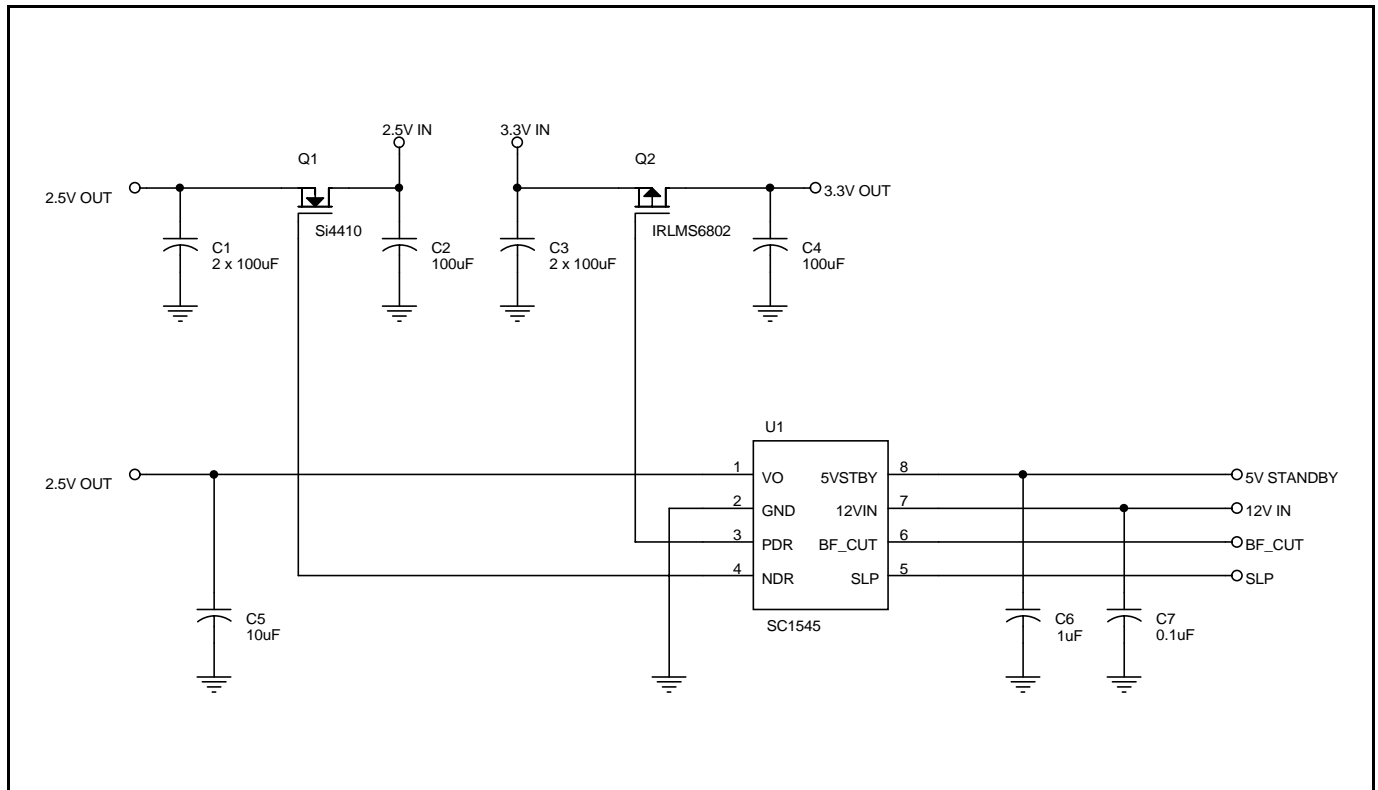
ORDERING INFORMATION

Part Number ⁽¹⁾	Package
SC1545CS	SO-8

Note:

(1) Add suffix 'TR' for tape and reel packaging.

TYPICAL APPLICATION CIRCUIT



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Maximum	Units
12V Input Voltage Range	12VIN	-0.3 to +15	V
5V Input Voltage Range	5VSTBY	-0.3 to +7	V
P-channel MOSFET Gate Drive	PDR	-0.3 to 5VSTBY	V
N-channel MOSFET Gate Drive	NDR	-0.3 to 12VIN	V
Input Pins		-0.3 to +7	V
Operating Ambient Temperature Range	T _A	0 to +70	°C
Operating Junction Temperature Range	T _J	0 to +125	°C
Storage Temperature Range	T _{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec	T _{LEAD}	300	°C
Thermal Impedance Junction to Case	θ _{JC}	47	°C/W
Thermal Impedance Junction to Ambient ⁽¹⁾	θ _{JA}	65	°C/W
ESD Rating	ESD	2	kV

Note:

(1) 2 inch square of 1/16" FR-4, double sided, 1 oz. minimum copper weight.

ELECTRICAL CHARACTERISTICS

 Unless specified, 12VIN = 12V, 5VSTBY = 5V, C_O = 100µF min., T_A = 25°C. Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
12VIN						
Supply Voltage	12VIN		11.28	12.00	12.72	V
Quiescent Current	I _{Q12}			800	1000	µA
					1200	
5VSTBY						
Supply Voltage	5VSTBY		4.7	5.0	5.3	V
Quiescent Current	I _{Q5}	LDO ON		9.5	11	mA
		LDO OFF		3.0	4.0	
					5.0	
Undervoltage Lockout (5V)						
UVLO Threshold	UVLO	5VSTBY rising	4.1	4.3	4.5	V
		5VSTBY falling	3.9	4.1	4.3	V
Hysteresis	HYST			200		mV
Logic Reset Threshold	RST		1.5	2.0	2.5	V

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ELECTRICAL CHARACTERISTICS (Cont.)

 Unless specified, 12VIN = 12V, 5VSTBY = 5V, C_O = 100μF min., T_A = 25°C. Values in **bold** apply over full operating temperature range.

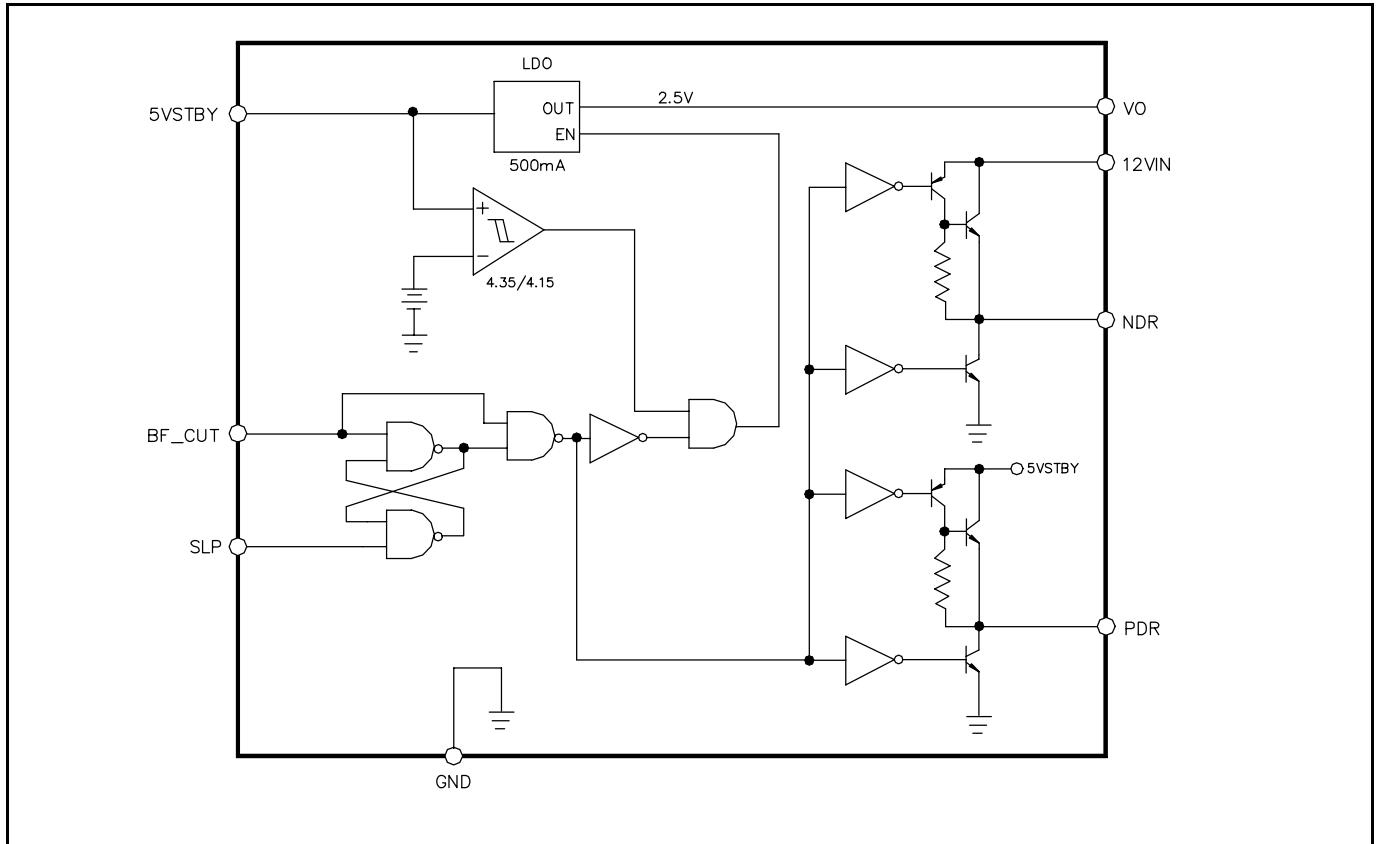
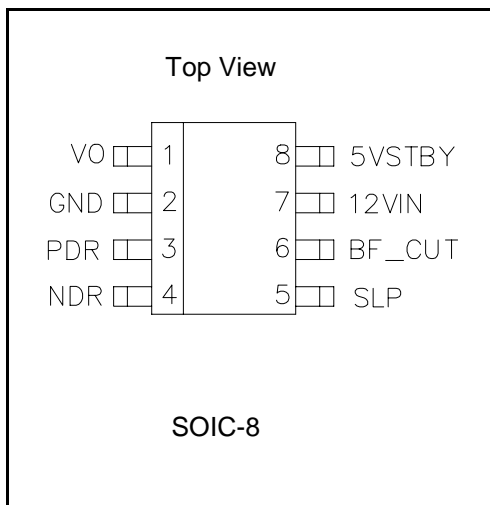
Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
VO						
LDO Output Voltage	V _O	4.7V ≤ 5VSTBY ≤ 5.3V, 1mA ≤ I _O ≤ 500mA	-1.5%	2.525	+1.5%	V
			-2.5%		+2.5%	
LDO Output Voltage During Load Transients ⁽¹⁾	V _{O(T)}	Load step between 0mA and 500mA at 8A/μs max.	-3.0%	2.525	+3.0%	V
Time To Regulation ⁽²⁾	t _{REG}				5	μs
Inputs (BF_CUT & SLP)						
Input Resistance	R _{IN}	BF_CUT = SLP = 5V	1.0	10.0		MΩ
High Level Input Voltage	V _{IH}		2.0			V
Low Level Input Voltage	V _{IL}				0.8	V
NDR						
Peak Drive Current	I _{NDR(PK)}	Sinking: NDR = 0.5V Sourcing: NDR = 10V	30			mA
Output Voltage	V _{NDR}	Full ON, I _{NDR} = 100μA	10	12		V
Drive Low Delay	t _{DL(N)}	Measured from BF_CUT threshold to 90% of NDR			150	ns
Fall Time	t _{f(N)}	Measured from 90% to 10%			1.0	μs
Drive High Delay	t _{DH(N)}	Measured from BF_CUT/SLP threshold to 10% of NDR			300	ns
Rise Time	t _{r(N)}	Measured from 10% to 90%			1.0	μs
PDR						
Peak Drive Current	I _{PDR(PK)}	Sinking: PDR = 0.5V Sourcing: PDR = 3.5V	30			mA
Output Voltage	V _{PDR}	Full ON, I _{PDR} = 100μA	3.5	5		V
Drive Low Delay	t _{DL(P)}	Measured from BF_CUT threshold to 90% of PDR			150	ns
Fall Time	t _{f(P)}	Measured from 90% to 10%			1.0	μs
Drive High Delay	t _{DH(P)}	Measured from BF_CUT/SLP threshold to 10% of PDR			300	ns
Rise Time	t _{r(P)}	Measured from 10% to 90%			1.0	μs
Overcurrent Protection						
Current Limit Threshold	I _{CL}	V _O = 0V	550			mA

NOTES:

 (1) The LDO will bring the output back to within the regular V_O limits in less than 10μs.

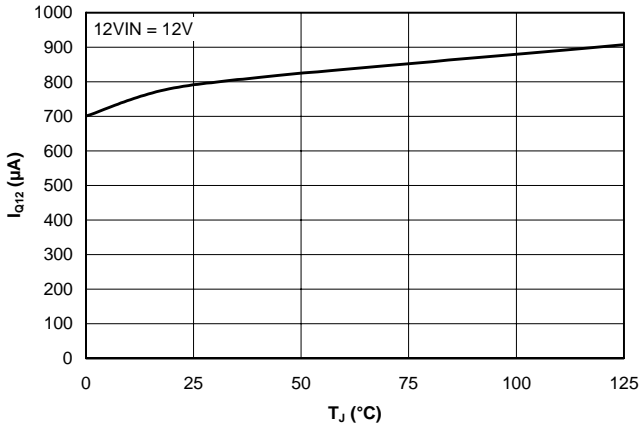
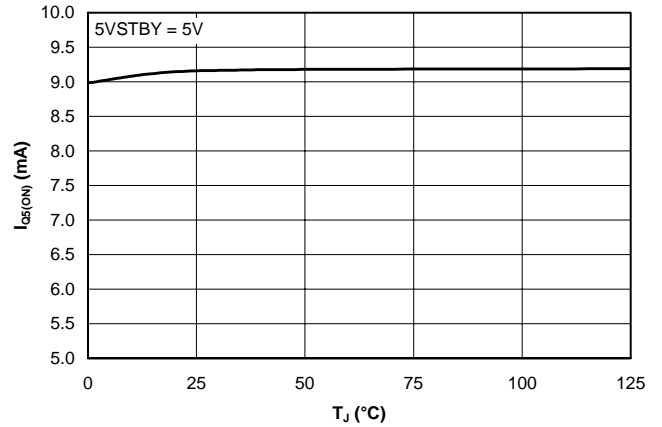
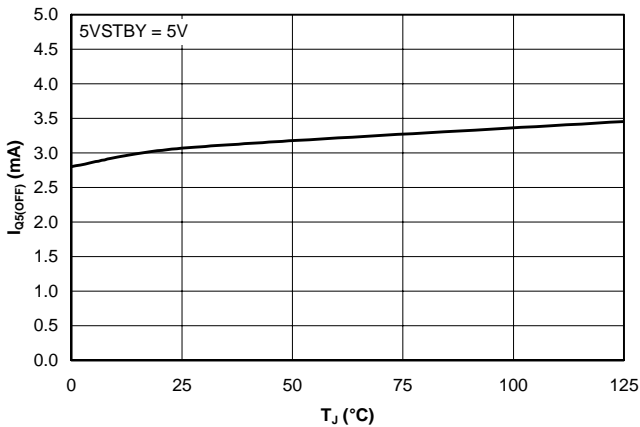
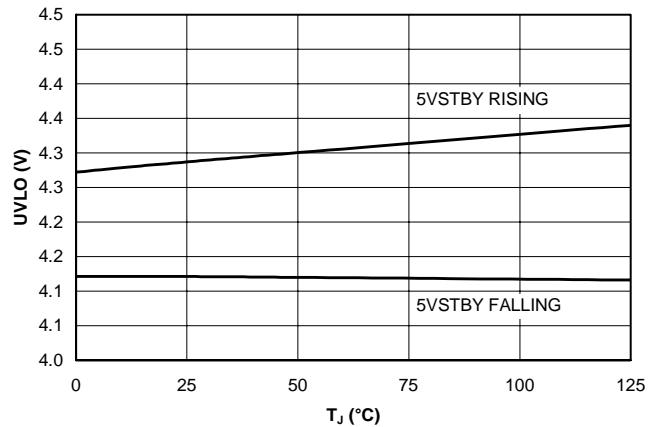
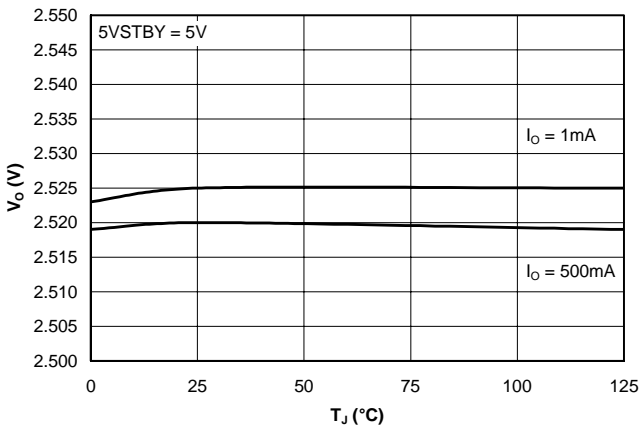
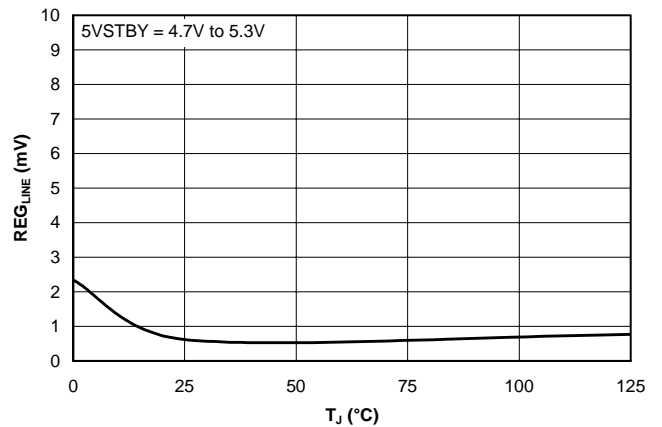
 (2) External 2.5V ± 2.5% applied at output, turning off when NDR goes low. C_O = 100μF to 400μF, I_O = 50mA to 200mA.

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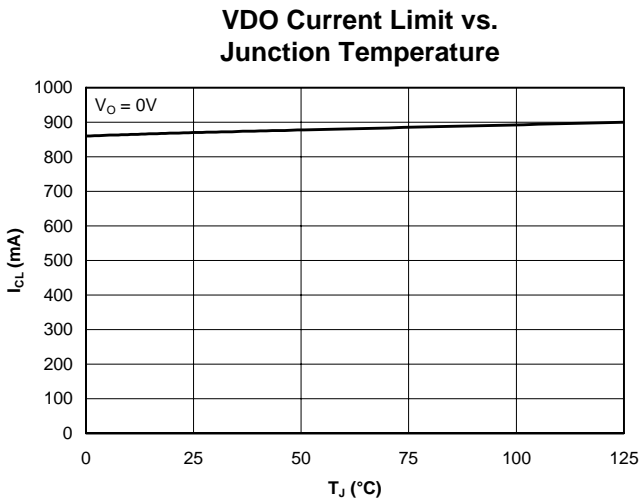
BLOCK DIAGRAM

PIN CONFIGURATION

PIN DESCRIPTION

Pin	Pin Name	Pin Function
1	VO	LDO 2.5V output.
2	GND	Logic and power ground.
3	PDR	Gate drive signal for P-channel MOSFETs.
4	NDR	Gate drive signal for N-channel MOSFETs.
5	SLP	Control input #1.
6	BF_CUT	Control input #2.
7	12VIN	+12V input supply. Used for generating NDR only.
8	5VSTBY	+5V input supply.

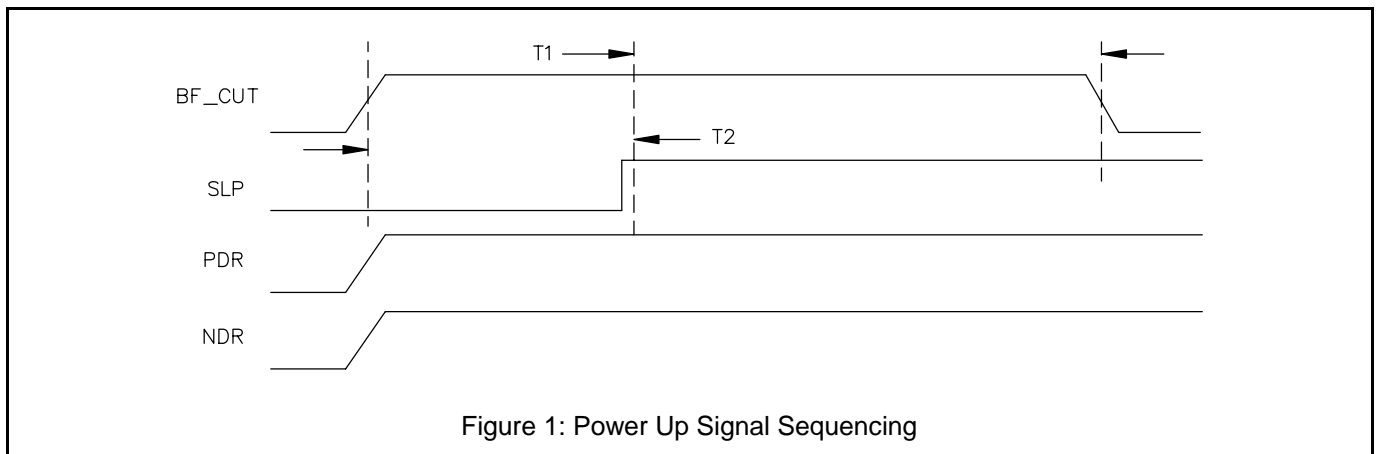
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TYPICAL CHARACTERISTICS
**12VIN Quiescent Current vs.
Junction Temperature**

**5VSTBY Quiescent Current (ON) vs.
Junction Temperature**

**5VSTBY Quiescent Current (OFF) vs.
Junction Temperature**

**5VSTBY Under Voltage Lockout vs.
Junction Temperature**

**LDO Output Voltage vs.
Junction Temperature**

**LDO Line Regulation vs.
Junction Temperature**


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TYPICAL CHARACTERISTICS (Cont.)

TIMING DIAGRAMS

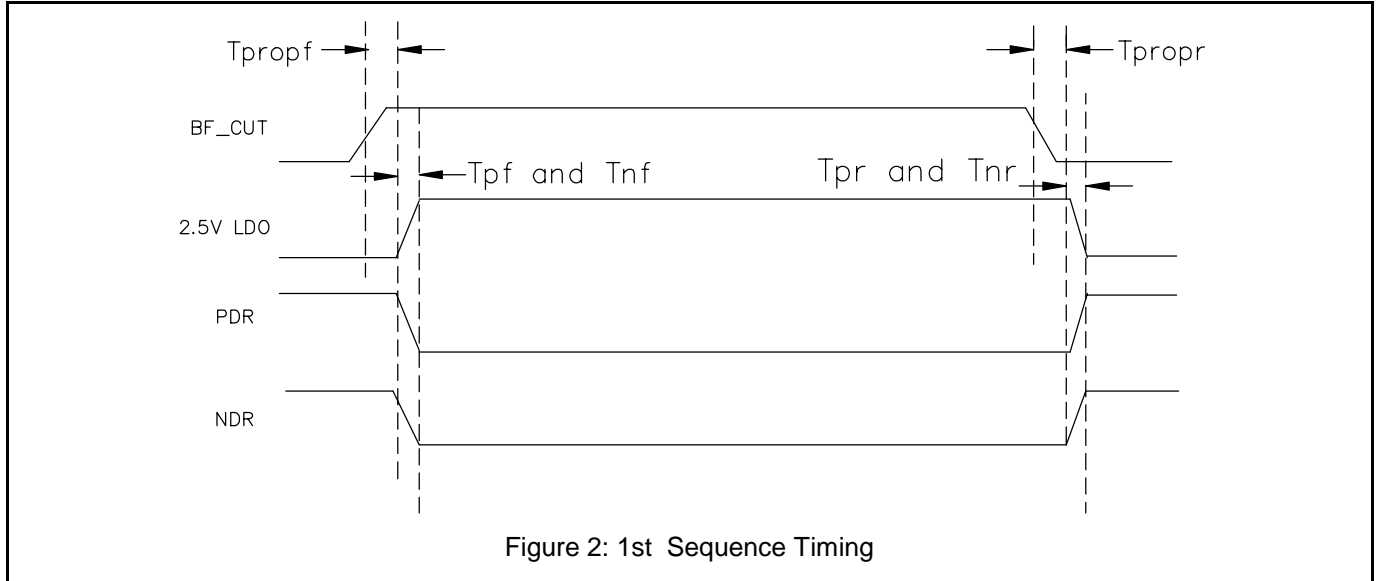
Power up signal sequencing is shown in Figure 1. BF_CUT, PDR and NDR follow the power rails up to their final values. SLP goes to its high value when the power rails have stabilized, ~25msec after power on. BF_CUT is pulled low a period T1 after SLP goes high. T1 can be as short as 1msec. Typical measured values are ~200msec. The 2.5V LDO output stays OFF through this sequence.



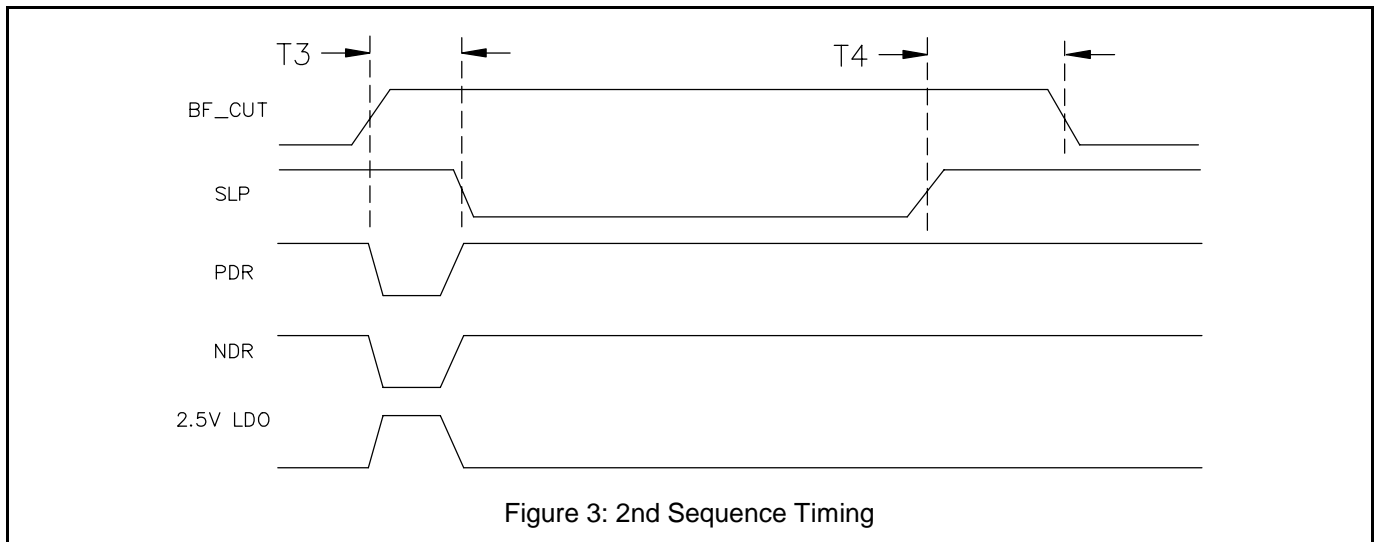
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TIMING DIAGRAMS (Cont.)

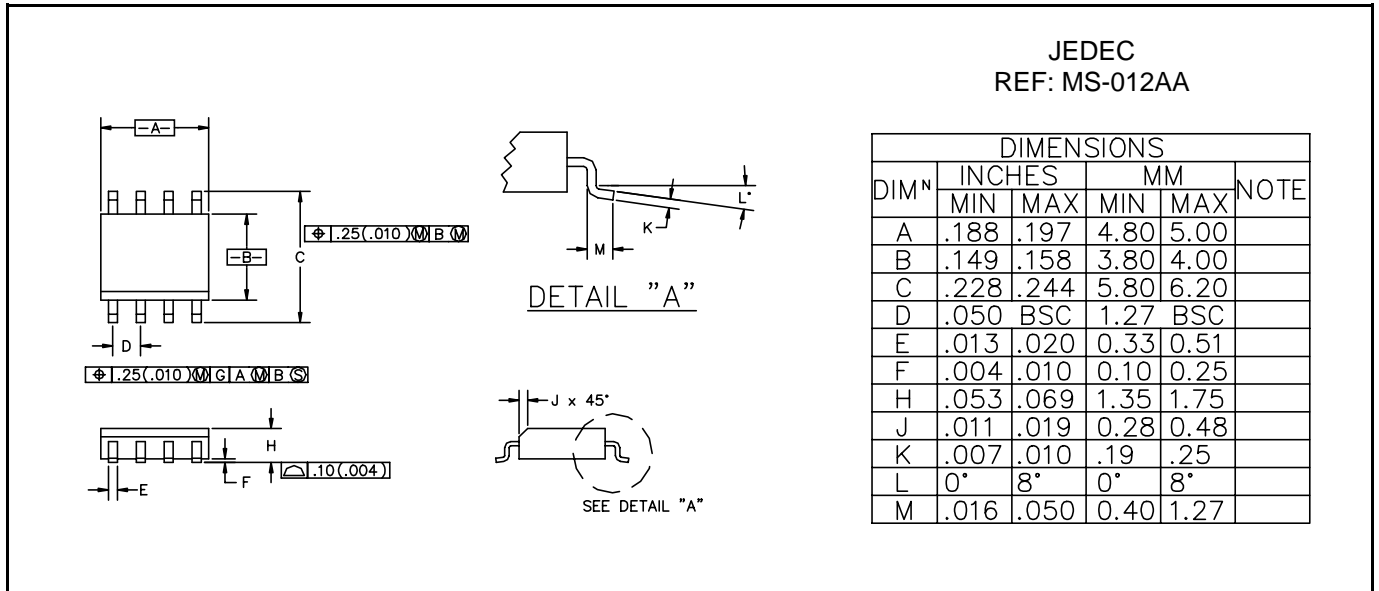
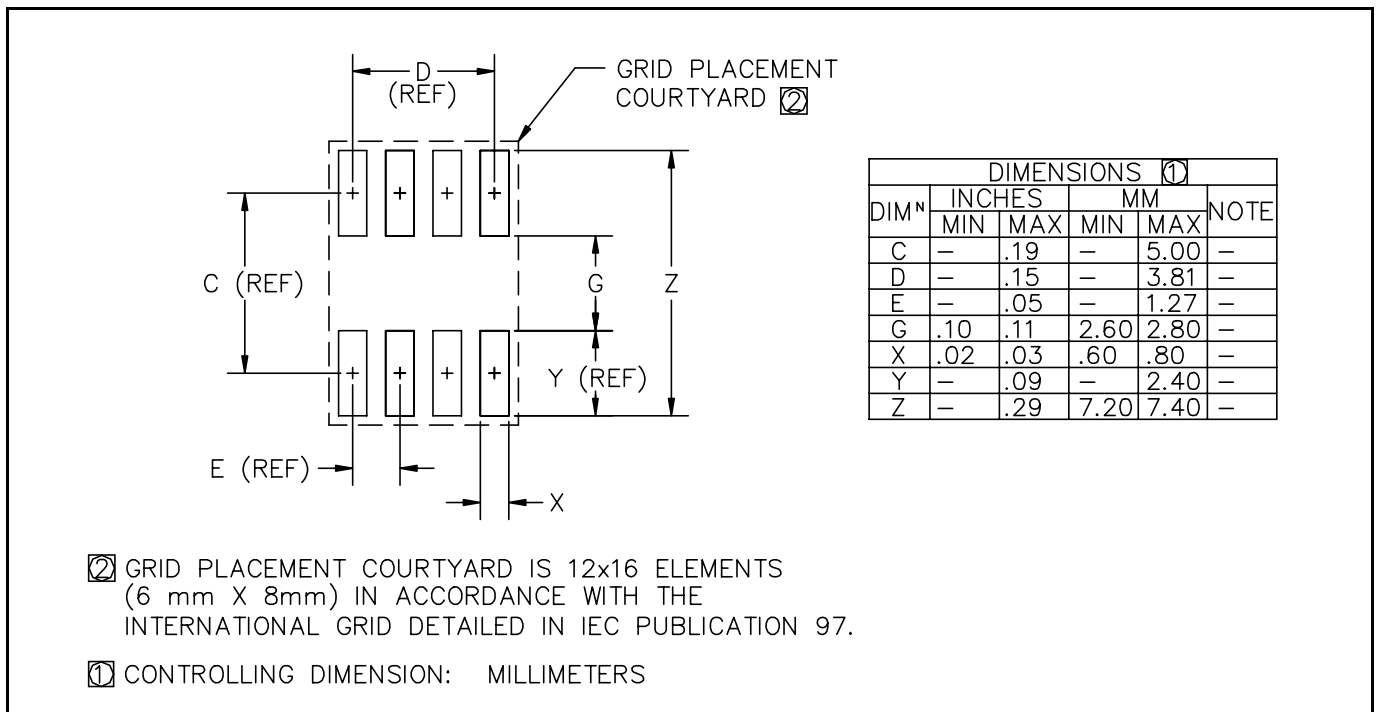
After power up, there are two possible signal sequences that the device will see. The first sequence is with SLP staying HIGH and BF_CUT transitioning from LOW to HIGH, remaining HIGH for an undetermined period and then going back to LOW. At this point, the system state is back to where it was at the end of the power up sequence. The sequence is shown in Figure 2 (below). During these BF_CUT transitions, the propagation delays, rise and fall times and going into regulation times for PDR, NDR and VO are described in Electrical Characteristics on page 3. The first sequence can start at any time after the end of the power up sequence.



Signal sequencing for the second possible sequence is shown in Figure 3. BF_CUT goes from LOW to HIGH and SLP goes from HIGH to LOW, 30μsec to 65μsec (T3) later. When BF_CUT goes HIGH, PDR and NDR go LOW and the 2.5V LDO turns ON. When SLP goes LOW, PDR and NDR return to HIGH and the 2.5V LDO turns OFF. BF_CUT will stay HIGH and SLP will stay low for an undetermined time, after which SLP will go HIGH. A minimum of 1msec (T4) later, BF_CUT will go LOW and the system is back at the end of the power up sequence. Typical measured values of T4 are ~250msec. During all transitions, the propagation delays, rise and fall times, and going into regulation times for PDR, NDR and 2.5V LDO are described in Electrical Characteristics on page 3. The second sequence can start at any time after the end of the power up sequence.



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OUTLINE DRAWING

MINIMUM LAND PATTERN - SO-8

 ECN99-694
 ECN00-831