SC4602A/B
High Efficiency Synchronous, Step Down Controller

Description

The SC4602A/B is a voltage mode step down (buck) regulator controller that provides accurate high efficiency power conversion from an input supply range of 2.75V to 5.5V. A high level of integration reduces external component count and makes it suitable for low voltage applications where cost, size and efficiency are critical.

The SC4602A/B drives external complementary power MOSFETs; P-channel on the high side and N-channel on the low side. The use of high side P-channel MOSFET eliminates the need for an external charge pump and simplifies the high side gate driver. Non-overlap protection is provided for the gate drive signals to prevent shoot through of the MOSFET pair. Voltage drop across the P-channel MOSFET during its conduction is sensed for lossless short circuit current limiting.

A low power sleep mode can be achieved by forcing the SYNC/SLEEP pin below 0.8V. A synchronous mode of operation is activated as the SYNC/SLEEP pin is driven by an external clock. The quiescent supply current in sleep mode is typically lower than 10μA. A soft start (2.4ms for the SC4602A and 1.2ms for the SC4602B) is internally provided to prevent output voltage overshoot during start-up. A 100% maximum duty cycle allows the SC4602A/B to operate as a low dropout regulator in the event of a low battery condition. The SC4602A/B has fixed switching frequency (300KHz for the SC4602A and 550KHz for the SC4602B).

The SC4602A/B is an ideal choice for 3.3V, 5V or other low input supply sytems. It's available in a 8 pin MSOP package.

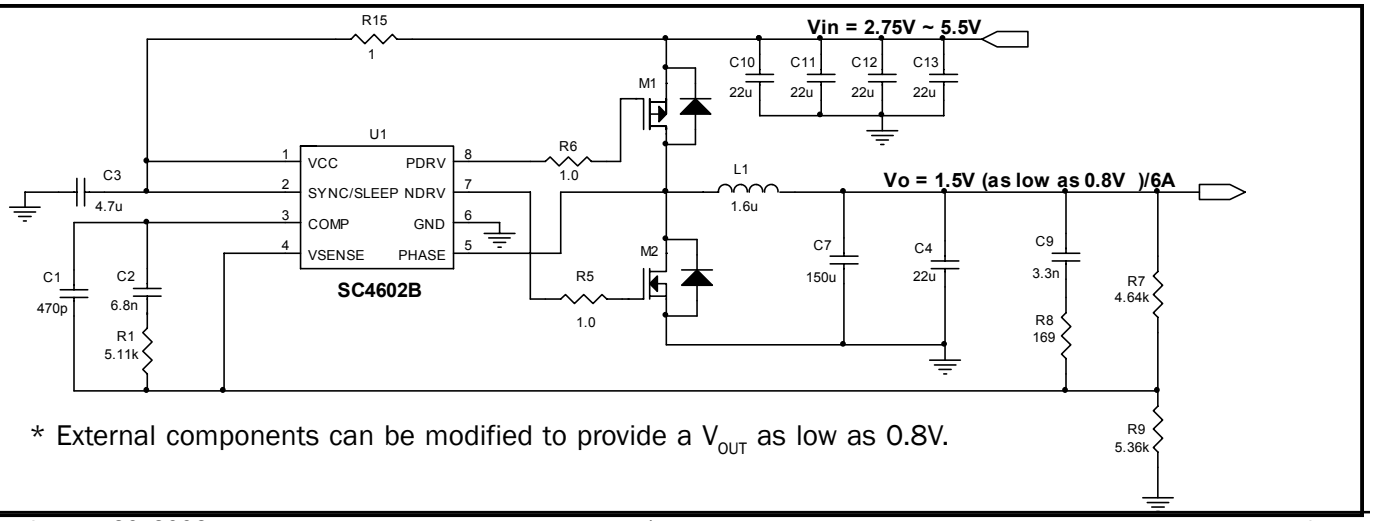
Features

- BICMOS Voltage mode PWM controller
- 2.75V to 5.5V Input voltage range
- Output voltages as low as 0.8V
- +/-1% Reference accuracy
- Sleep Mode (Icc = 10μA typ)
- Lossless short circuit current limiting
- Combination pulse by pulse & hiccup mode current limit
- High efficiency synchronous switching
- Up to 100% Duty cycle range
- Synchronization to external clock
- 8-Pin MSOP surface mount package. Lead-free package available, fully WEEE and RoHS compliant

Applications

- Distributed power system
- RF power supply
- Local microprocessor core power supplies
- DSP and I/O power supplies
- Battery powered applications
- Servers and workstations

Typical Application Circuit



* External components can be modified to provide a V_{OUT} as low as 0.8V.

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage (V_{CC})		7	V
Output Drivers (PDRV, NDRV) Currents Continuous		±0.25	A
Inputs (VSENSE, COMP, SYNC/SLEEP, FS, ISET)		-0.3 to 7	V
Phase		-0.3 to 7	V
Phase Pulse tpulse < 50ns		-2 to 7	V
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Maximum Junction Temperature	T_J	+150	°C
Thermal Impedance Junction to Case	θ_{JC}	41.9	°C/W
Thermal Impedance Junction to Ambient	θ_{JA}	113.1	°C/W
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	+300	°C
ESD Rating (Human Body Model)	ESD	2	kV

All voltages with respect to GND. Currents are positive into, negative out of the specified terminal.

Electrical Characteristics

Unless otherwise specified, V_{CC} = 3.3V, T_A = -40°C to 85°C, $T_A = T_J$.

Parameter	Test Conditions	Min	Typ	Max	Unit
Overall					
Supply Voltage		2.75		5.5	V
Supply Current, Sleep	$V_{SYNC/SLEEP}$ = 0V		10	15	µA
Supply Current, Operating			1.5	3	mA
VCC Turn-on Threshold			2.55	2.75	V
VCC Turn-off Hysteresis			150		mV
Error Amplifier					
Internal Reference	T_A = 25°C	0.792	0.8	0.808	V
	V_{CC} = 2.75V to 5.5V, T_A = 25°C	0.788	0.8	0.812	
	T_A = -40°C to 85°C	0.784	0.8	0.816	
VSENSE Bias Current			25		nA
Open Loop Gain (1)	V_{COMP} = 0.4V to 1.8V	70	80		dB
Unity Gain Bandwidth (1)			4		MHz
Slew Rate (1)			2		V/µs

Electrical Characteristics (Cont.)

Unless otherwise specified, V_{CC} = 3.3V, T_A = -40°C to 85°C, $T_A = T_J$.

Parameter	Test Conditions	Min	Typ	Max	Unit
Error Amplifier (Cont.)					
VCOMP High	I_{COMP} = -2mA	2.8	3.1		V
VCOMP Low	I_{COMP} = 2mA		0.15	0.3	V
Oscillator					
Initial Accuracy (SC4602A)	T_A = 25°C, VSYNC = HIGH	260	300	340	kHz
Initial Accuracy (SC4602B)	T_A = 25°C, VSYNC = HIGH	480	550	620	kHz
SYNC/SLEEP Low Threshold				0.8	V
SYNC/SLEEP High Threshold		2.0			V
Ramp Peak to Valley (1)		1.3	1.5	1.7	V
Ramp Peak Voltage (1)			1.85	1.9	V
Ramp Valley Voltage (1)		0.3	0.35		V
Sleep, Soft Start, Current Limit					
Sleep Input Bias Current	VSYNC/SLEEP = 0V		-1		µA
Soft Start Time (1)	SC4602A		2.4		ms
	SC4602B		1.2		
Current Limit Threshold (2)	Reference to V_{CC}, T_J = 25°C		-300		mV
	Temperature coefficient		0.4		%/°C
Current Limit Blank Time (1)			150		ns
N-Channel and P-Channel Driver Outputs					
Pull Up Resistance (PDRV) (2)	Vcc = 3.3V, I_{OUT} = -100mA (source)			3	ohms
Pull Down Resistance (PDRV) (2)	Vcc = 3.3V, I_{OUT} = 50mA (sink)			3	ohms
Pull Up Resistance (NDRV) (2)	Vcc = 3.3V, I_{OUT} = -100mA (source)			3	ohms
Pull Down Resistance (NDRV) (2)	Vcc = 3.3V, I_{OUT} = 100mA (sink)			3	ohms
PDRV Output Rise Time (1)	Vgs = 3.3V, C_{OUT} = 1.0nF		9		ns
PDRV Output Fall Time (1)	Vgs = 3.3V, C_{OUT} = 1.0nF		12		ns

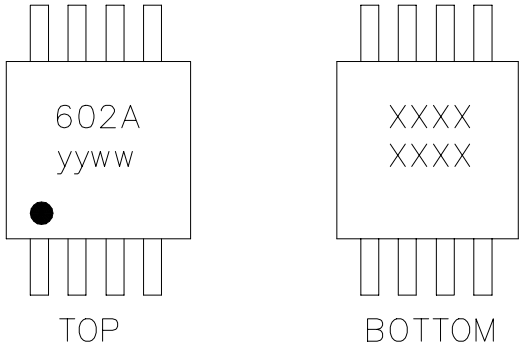
Electrical Characteristics (Cont.)

Unless otherwise specified, V_{CC} = 3.3V, T_A = -40°C to 85°C, $T_A = T_J$.

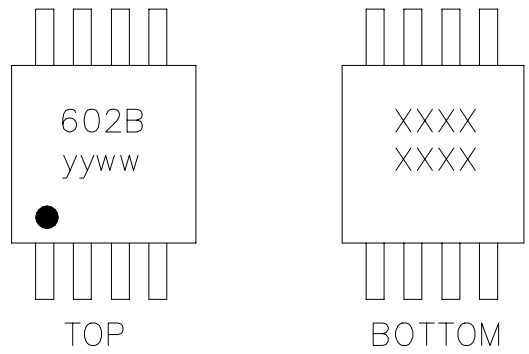
Parameter	Test Conditions	Min	Typ	Max	Unit
N-channel and P-Channel Driver Outputs (Cont.)					
NDRV Output Rise Time (1)	Vgs = 3.3V, C_{OUT} = 1.0nF		15		ns
NDRV Output Fall Time (1)	Vgs = 3.3V, C_{OUT} = 1.0nF		15		ns
Deadtime Delay (PDRV high to NDRV high) (1)			adaptive		
Deadtime Delay (NDRV low to PDRV low) (1)			50		ns

Notes:
(1) Guaranteed by design.
(2) Guaranteed by characterization.
(3) Dead time delay from PDRV high to NDRV high is adaptive. As the phase node voltage drops below 600mV due to PDRV high, NDRV will start to turn high.

Marking Information



yyww = Date Code (Example: 0012)
xxxxxxxx = Semtech Lot No. (Example: E901 01-1)



yyww = Date Code (Example: 0012)
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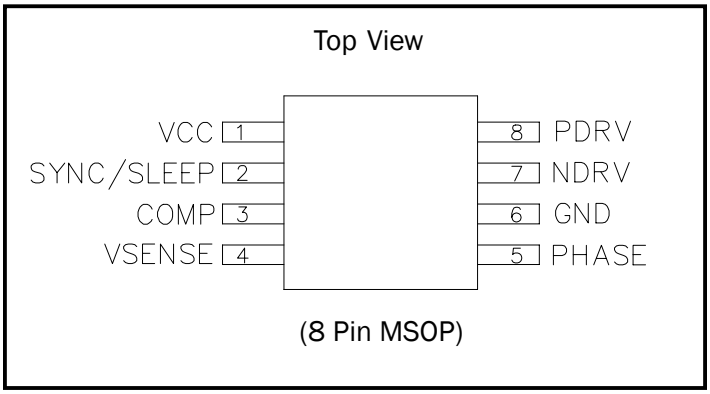
Pin Configuration



Ordering Information

Part Number(1)	kHz	Device
SC4602AIMSTR	300	MSOP-8
SC4602AIMSTRT(2)		
SC4602BIMSTR	550	MSOP-8
SC4602BIMSTRT(2)		
SC4602AEVB	Evaluation Board	
SC4602BEVB		

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

VCC: Positive supply rail for the IC. Bypass this pin to GND with a 0.1 to 4.7µF low ESL/ESR ceramic capacitor.

GND: All voltages are measured with respect to this pin. All bypass and timing capacitors connected to GND should have leads as short and direct as possible.

SYNC/SLEEP: The oscillator of SC4602A and SC4602B are set to 300kHz and 550kHz respectively when SYNC/SLEEP is pulled and held above 2V. Synchronous mode operation is activated as the SYNC/SLEEP is driven by an external clock. The oscillator and PWM are designed to provide practical operation to 450kHz for SC4602A and to 700kHz for SC4602B when synchronized. Sleep mode is invoked if SYNC/SLEEP is pulled and held below 0.8V which can be accomplished by an external gate or transistor. Sleepmode supply current is 10µA typical.

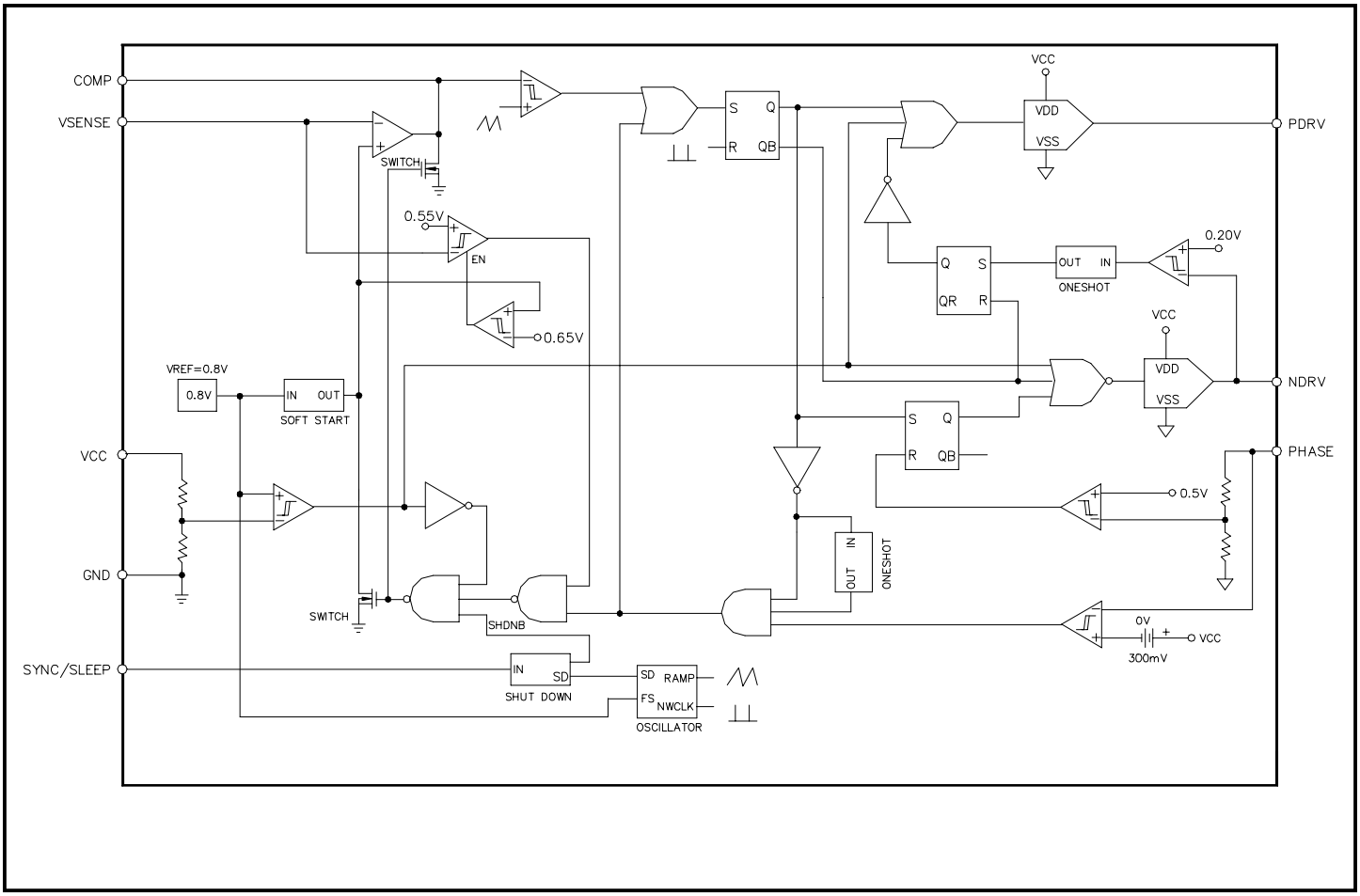
VSENSE: This pin is the inverting input of the voltage amplifier and serves as the output voltage feedback point for the Buck converter. It senses the output voltage through an external divider.

COMP: This is the output of the voltage amplifier. The voltage at this output is inverted internally and connected to the non-inverting input of the PWM comparator. A lead-lag network around the voltage amplifier compensates for the two pole LC filter characteristic inherent to voltage mode control and is required in order to optimize the dynamic performance of the voltage mode control loop.

PHASE: This input is connected to the junction between the two external power MOSFET transistors. The voltage drop across the upper P-channel device is monitored by PHASE during conduction and forms the current limit comparator. Logic sets the PWM latch and terminates the output pulse. The controller stops switching and goes through a soft start sequence once the converter output voltage drops below 68.75% its nominal voltage. This prevents excess power dissipation in the PMOSFET during a short circuit. The reverse current comparator senses the drop across the lower N-channel MOSFET during its conduction and disables the drive signal if a small positive voltage is present. To disable the overcurrent comparator, connect PHASE to VCC.

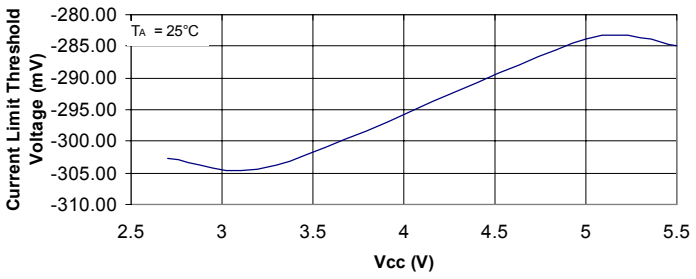
PDRV, NDRV: The PWM circuitry provides complementary drive signals to the output stages. Cross conduction of the external MOSFETS is prevented by monitoring the voltage on the P-channel and N-channel driver pins in conjunction with a time delay optimized for FET turn-off characteristics.

Block Diagram

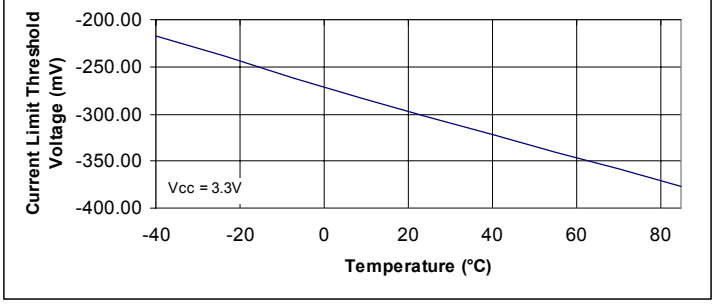


Typical Characteristic (Cont.)

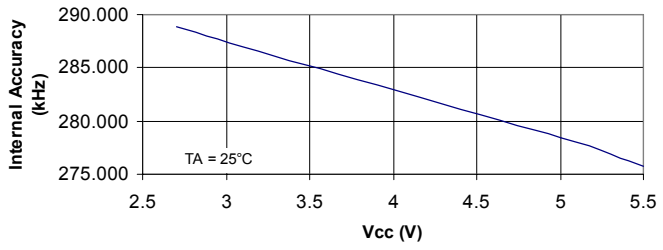
Current Limit Threshold Voltage vs Input Voltage



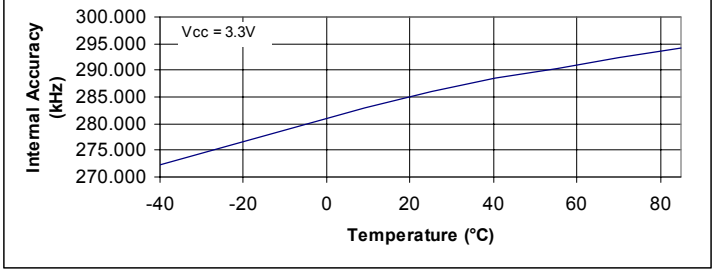
Current Limit Threshold Voltage vs Temperature



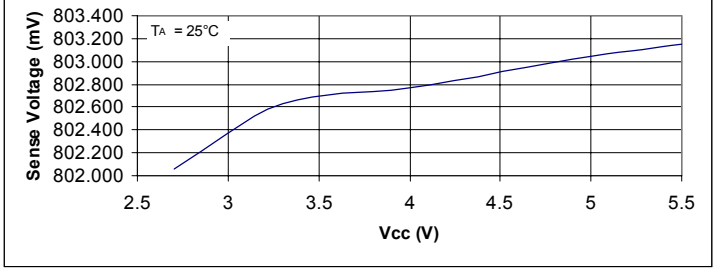
Sc4602A Oscillator Internal Accuracy vs Input Voltage



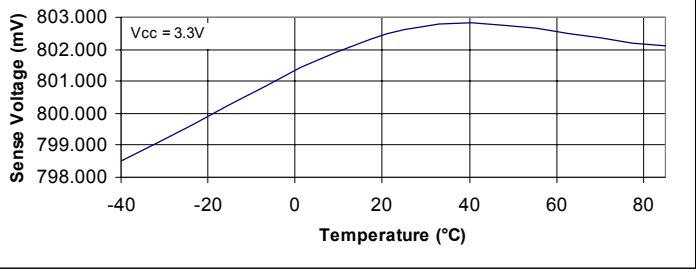
Sc4602A Oscillator Internal Accuracy vs Temperature



Sc4602A Sense Voltage vs Input Voltage

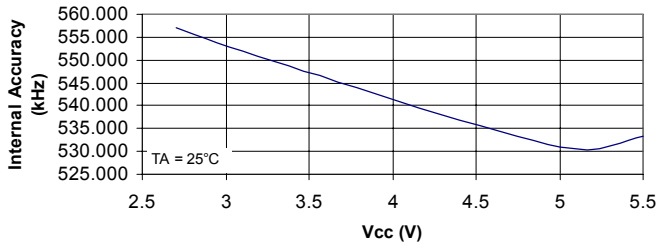


Sc4602A Sense Voltage vs Temperature

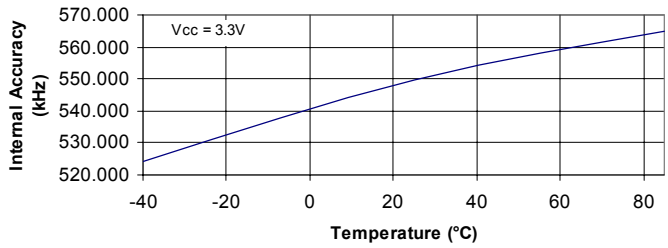


Typical Characteristic (Cont.)

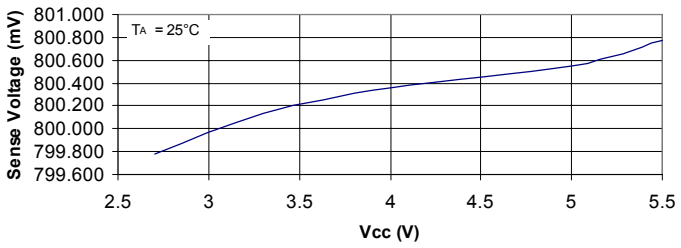
Sc4602B
Oscillator Internal Accuracy
vs
Input Voltage



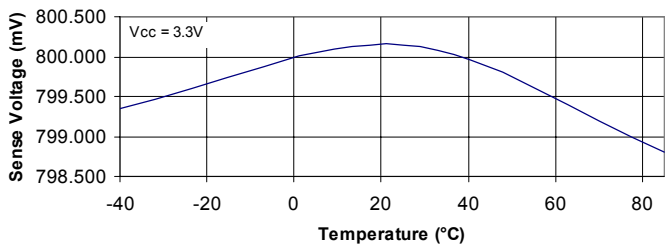
Sc4602B
Oscillator Internal Accuracy
vs
Temperature



Sc4602B
Sense Voltage
vs
Input Voltage



Sc4602B
Sense Voltage
vs
Temperature



Applications Information

Enable

Pulling and holding the SYNC/SLEEP pin below 0.8V initializes the SLEEP mode of the SC4602A/B with its typical SLEEP mode supply current of 10uA. During the SLEEP mode, the high side and low side MOSFETs are turned off and the internal soft start voltage is held low.

Oscillator

The SC4602A/B is a constant frequency, voltage mode, and synchronous step down controller ideal for low voltage, high efficiency, precisely regulated output DC/DC converters. Its internal free running oscillator sets the PWM frequency at 300kHz for the SC4602A and 550kHz for the SC4602B without any external components to set the frequency. A 100% maximum duty cycle allows the SC4602A/B to operate as a low dropout regulator in the event of a low battery condition. An external clock connected to SYNC/SLEEP activates its synchronous mode and the frequency of the clock can be up to 450kHz for the SC4602A and 700kH for the SC4602B.

UVLO

When the SYNC/SLEEP pin is pulled and held above 2V, the voltage on the Vcc pin determines the operation of the SC4602A/B. As Vcc increases during start up, the UVLO block senses Vcc and keeps the high side and low side MOSFETs off and the internal soft start voltage low until Vcc reaches 2.75V. If no faults are present, the SC4602A/B will initiate a soft start when Vcc exceeds 2.75V. A hysteresis (150mV) in the UVLO comparator provides noise immunity during its start up.

Soft Start

The soft start function is required for step down controllers to prevent excess inrush current through the DC bus during start up. Generally this can be done by sourcing a controlled current into a timing capacitor and then using the voltage across this capacitor to slowly ramp up the error amp reference. The closed loop creates narrow width driver pulses while the output voltage is low and allows these pulses to increase to their steady state duty cycle as the output voltage reaches its regulated value. With this, the inrush current from the input side is controlled. The duration of the soft start in the SC4602A/B is controlled by an internal timing circuit which is used during start up and over current to set the hiccup time. The soft start time can be calculated by:

$$T_{SOFT\_START} = \frac{720}{f_s}$$

As can be seen here, the soft start time is switching frequency dependant. For example, if f_s = 300kHz, $T_{SOFT—START}$ = 720/300k = 2.4ms. But if f_s = 600kHz, $T_{SOFT—START}$ = 720/600k = 1.2ms.

The SC4602A/B implements its soft start by ramping up the error amplifier reference voltage providing a controlled slew rate of the output voltage, then preventing overshoot and limiting inrush current during its start up.

Over Current Protection

Over current protection for the SC4602A/B is implemented by detecting the voltage drop of the high side P-MOSFET during conduction, also known as high side $R_{DS(ON)}$ detection. This loss-less detection eliminates the sense resistor and its loss. The overall efficiency is improved, and the number of components and cost of the converter are reduced. $R_{DS(ON)}$ sensing is by default inaccurate and is mainly used to protect the power supply during a fault case. The over current trigger point will vary from unit to unit as the $R_{DS(ON)}$ of P-MOSFET varies. Even for the same unit, the over current trigger point will vary as the junction temperature of P-MOSFET varies. The SC4602A/B provides a built-in 300mV voltage source. The over current trigger point can be determined based on the internal 300mV voltage source and the $R_{DS(ON)}$ of P-MOSFET as follows:

$$I_{trigger} = \frac{300mV}{R_{DS(ON)}}$$

Kelvin sensing connections should be used at the drain and source of P-MOSFET.

The $R_{DS(ON)}$ sensing used in the SC4602A/B has an additional feature that enhances the performance of the over current protection. Because the $R_{DS(ON)}$ has a positive temperature coefficient, the 300mV voltage source has a positive coefficient of about 0.4%/C° providing first order correction for current sensing vs temperature. This compensation depends on the high amount of thermal transferring that typically exists between the high side P-MOSFET and the SC4602A/B due to the compact layout of the power supply.

Applications Information (Cont.)

When the converter detects an over current condition ($I > I_{MAX}$) as shown in Figure 1, the first action the SC4602A/B takes is to enter cycle by cycle protection mode (Point B to Point C), which responds to minor over current cases. Then the output voltage is monitored. If the over current and low output voltage (set at 68.75% of nominal output voltage) occur at the same time, the Hiccup mode operation (Point C to Point D) of the SC4602A/B is invoked and the internal soft start capacitor is discharged. This is like a typical soft start cycle.

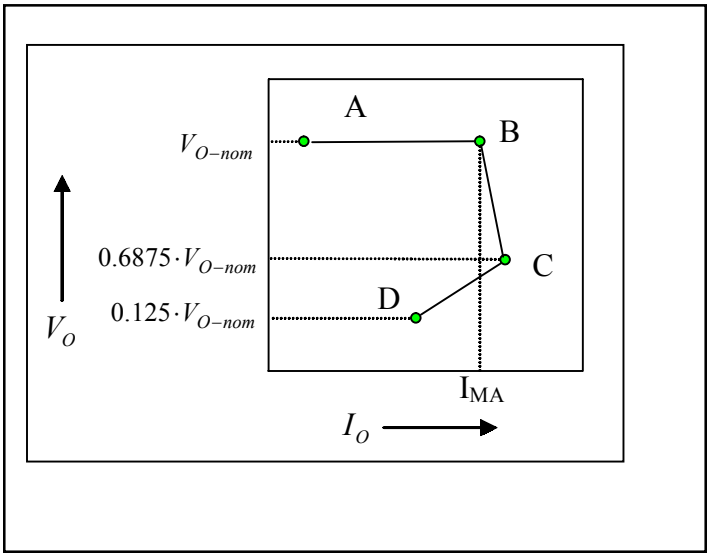


Figure 1. Over current protection characteristic of SC4602A/B

Power MOSFET Drivers

The SC4602A/B has two drivers for external complementary power MOSFETs. The driver block consists of one high side P-MOSFET, 4Ω driver, PDRV, and one low side 5Ω, N-MOSFET driver, NDRV, which are optimized for driving external power MOSFETs in a synchronous buck converter. The output drivers also have gate drive non-overlap mechanism that gives a dead time between PDRV and NDRV transitions to avoid potential shoot through problems in the external MOSFETs. By using the proper design and the appropriate MOSFETs, a 6A converter can be achieved. As shown in Figure 2, $t_{d1,}$ the delay from the P-MOSFET off to the N-MOSFET on is adaptive by detecting the voltage of the phase node. t_{d2}, the delay from the N-MOSFET off to the P-MOSFET on is fixed, is 100ns for the SC4602A/B. This control scheme guarantees avoiding the cross conduction or shoot through between two MOSFETs and minimizes the conduction loss in the bottom diode for high efficiency applications.

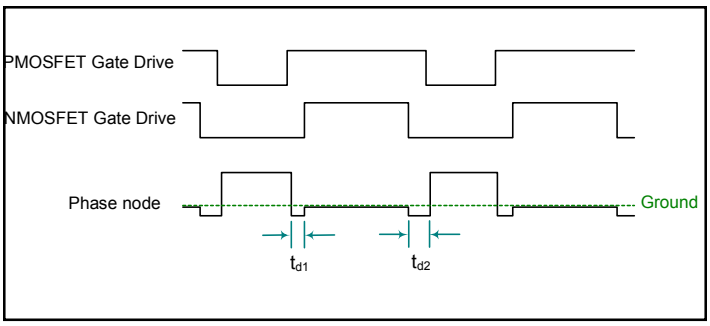


Figure 2. Timing Waveforms for Gate Drives and Phase Node

Inductor Selection

The factors for selecting the inductor include its cost, efficiency, size and EMI. For a typical SC4602A/B application, the inductor selection is mainly based on its value, saturation current and DC resistance. Increasing the inductor value will decrease the ripple level of the output voltage while the output transient response will be degraded. Low value inductors offer small size and fast transient responses while they cause large ripple currents, poor efficiencies and more output capacitance to smooth out the large ripple currents. The inductor should be able to handle the peak current without saturating and its copper resistance in the winding should be as low as possible to minimize its resistive power loss. A good trade-off among its size, loss and cost is to set the inductor ripple current to be within 15% to 30% of the maximum output current.

The inductor value can be determined according to its operating point and the switching frequency as follows:

$$L = \frac{V_O \cdot (V_I - V_O)}{V_I \cdot f_s \cdot \Delta I \cdot I_{OMAX}}$$

Where:
f_s = switching frequency and
ΔI = ratio of the peak to peak inductor current to the maximum output load current.

The peak to peak inductor current is:

$$I_{P-P} = \Delta I \bullet I_{OMAX}$$

Applications Information (Cont.)

After the required inductor value is selected, the proper selection of the core material is based on the peak inductor current and efficiency requirements. The core must be able to handle the peak inductor current I_{PEAK} without saturation and produce low core loss during the high frequency operation.

$$I_{PEAK} = I_{OMAX} + \frac{I_{p-p}}{2}$$

The power loss for the inductor includes its core loss and copper loss. If possible, the winding resistance should be minimized to reduce inductor's copper loss. The core loss can be found in the manufacturer's datasheet. The inductor' copper loss can be estimated as follows:

$$P_{COPPER} = I^2_{LRMS} \cdot R_{WINDING}$$

Where:

I_{LRMS} is the RMS current in the inductor. This current can be calculated as follows:

$$I_{LRMS} = I_{OMAX} \cdot \sqrt{1 + \frac{1}{3} \cdot \Delta I^2}$$

Output Capacitor Selection

Basically there are two major factors to consider in selecting the type and quantity of the output capacitors. The first one is the required ESR (Equivalent Series Resistance) which should be low enough to reduce the voltage deviation from its nominal one during its load changes. The second one is the required capacitance, which should be high enough to hold up the output voltage. Before the SC4602A/B regulates the inductor current to a new value during a load transient, the output capacitor delivers all the additional current needed by the load. The ESR and ESL of the output capacitor, the loop parasitic inductance between the output capacitor and the load combined with inductor ripple current are all major contributors to the output voltage ripple. Surface mount speciality polymer aluminum electrolytic chip capacitors in UE series from Panasonic provide low ESR and reduce the total capacitance required for a fast transient response. POSCAP from Sanyo is a solid electrolytic chip capacitor which has a low ESR and good performance for high frequency with a low profile and high capacitance. Above mentioned capacitors are recommended to use in SC4602A/B applications.

Input Capacitor Selection

The input capacitor selection is based on its ripple current level, required capacitance and voltage rating. This capacitor must be able to provide the ripple current by the switching actions. For the continuous conduction mode, the RMS value of the input capacitor can be calculated from:

$$I_{CIN(RMS)} = I_{OMAX} \cdot \sqrt{\frac{V_O \cdot (V_I - V_O)}{V^2_I}}$$

This current gives the capacitor's power loss as follows:

$$P_{CIN} = I^2_{CIN(RMS)} \cdot R_{CIN(ESR)}$$

This capacitor's RMS loss can be a significant part of the total loss in the converter and reduce the overall converter efficiency. The input ripple voltage mainly depends on the input capacitor's ESR and its capacitance for a given load, input voltage and output voltage. Assuming that the input current of the converter is constant, the required input capacitance for a given voltage ripple can be calculated by:

$$C_{IN} = I_{OMAX} \cdot \frac{D \cdot (1-D)}{fs \cdot (\Delta V_I - I_{OMAX} \cdot R_{CIN(ESR)})}$$

Where:

$D = V_O/V_I$, duty ratio and

DV_I = the given input voltage ripple.

Because the input capacitor is exposed to the large surge current, attention is needed for the input capacitor. If tantalum capacitors are used at the input side of the converter, one needs to ensure that the RMS and surge ratings are not exceeded. For generic tantalum capacitors, it is wise to derate their voltage ratings at a ratio of 2 to protect these input capacitors.

Power Mosfet Selection

The SC4602A/B can drive a P-MOSFET at the high side and an N-MOSFET synchronous rectifier at the low side. The use of the high side P-MOSFET eliminates the need for an external charge pump and simplifies the high side gate driver circuit.

Applications Information (Cont.)

For the top MOSFET, its total power loss includes its conduction loss, switching loss, gate charge loss, output capacitance loss and the loss related to the reverse recovery of the bottom diode, shown as follows:

$$P_{TOP\_TOTAL} = I^2_{TOP\_RMS} \cdot R_{TOP\_ON} + \frac{I_{TOP\_PEAK} \cdot V_I \cdot f_s}{V_{GATE} / R_G} \cdot (Q_{GD} + Q_{GS2}) + Q_{GT} \cdot V_{GATE} \cdot f_s + (Q_{OSS} + Q_{rr}) \cdot V_I \cdot f_s$$

Where:
R_G = gate drive resistor,
Q_{GD} = the gate to drain charge of the top MOSFET,
Q_{GS2} = the gate to source charge of the top MOSFET,
Q_{GT} = the total gate charge of the top MOSFET,
Q_{OSS} = the output charge of the top MOSFET and
Q_{rr} = the reverse recovery charge of the bottom diode.

For the top MOSFET, it experiences high current and high voltage overlap during each on/off transition. But for the bottom MOSFET, its switching voltage is the bottom diode's forward drop during its on/off transition. So the switching loss for the bottom MOSFET is negligible. Its total power loss can be determined by:

$$P_{BOT\_TOTAL} = I^2_{BOT\_RMS} \cdot R_{BOT\_ON} + Q_{GB} \cdot V_{GATE} \cdot f_s + I_{D\_AVG} \cdot V_F$$

Where:
Q_{GB} = the total gate charge of the bottom MOSFET and
V_F = the forward voltage drop of the bottom diode.

For a low voltage and high output current application such as the 3.3V/1.5V@6A case, the conduction loss is often dominant and selecting low $R_{DS(ON)}$ MOSFETs will noticeably improve the efficiency of the converter even though they give higher switching losses.

The gate charge loss portion of the top/bottom MOSFET's total power loss is derived from the SC4602A/B. This gate charge loss is based on certain operating conditions (f_s, V_{GATE}, and I_O).

The thermal estimations have to be done for both MOSFETs to make sure that their junction temperatures do not exceed their thermal ratings according to their total power losses P_{TOTAL}, ambient temperature T_a and their thermal resistances $R\theta_{ja}$ as follows:

$$T_{j(max)} < T_a + \frac{P_{TOTAL}}{R_{\theta ja}}$$

Loop Compensation Design

For a DC/DC converter, it is usually required that the converter has a loop gain of a high cross-over frequency for fast load response, high DC and low frequency gain for low steady state error, and enough phase margin for its operating stability. Often one can not have all these properties at the same time. The purpose of the loop compensation is to arrange the poles and zeros of the compensation network to meet the requirements for a specific application.

The SC4602A/B has an internal error amplifier and requires the compensation network to connect among the COMP pin and VSENSE pin, GND, and the output as shown in Figure 3. The compensation network includes C1, C2, R1, R7, R8 and C9.

R9 is used to program the output voltage according to:

$$V_O = 0.8 \cdot (1 + \frac{R_7}{R_9})$$

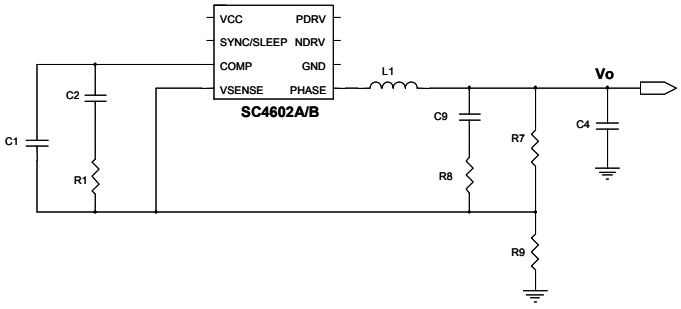


Figure 3. Compensation network provides 3 poles and 2 zeros.

For voltage mode step down applications as shown in Figure 3, the power stage transfer function is:

$$G_{VD}(s) = V_I \frac{1 + \frac{s}{\frac{1}{R_C \cdot C_4}}}{1 + s\frac{L_1}{R} + s^2 L_1 C_4}$$

Applications Information (Cont.)

Where:
R = load resistance and
R_C = C_4's ESR.

The compensation network will have the characteristic as follows:

$$G_{COMP}(s) = \frac{\omega_I}{s} \cdot \frac{1+\frac{s}{\omega_{Z1}}}{1+\frac{s}{\omega_{P1}}} \cdot \frac{1+\frac{s}{\omega_{Z2}}}{\cdot 1+\frac{s}{\omega_{P2}}}$$

Where:

$$\omega_I = \frac{1}{R_7 \cdot (C_1 + C_2)}$$

$$\omega_{Z1} = \frac{1}{R_1 \cdot C_2}$$

$$\omega_{Z2} = \frac{1}{(R_7 + R_8) \cdot C_9}$$

$$\omega_{P1} = \frac{C_1 + C_2}{R_1 \cdot C_1 \cdot C_2}$$

$$\omega_{P2} = \frac{1}{R_8 \cdot C_9}$$

After the compensation, the converter will have the following loop gain:

$$T(s) = G_{PWM} \cdot G_{COMP}(s) \cdot G_{VD}(s)$$

$$= \frac{\frac{1}{V_M} \cdot \omega_I \cdot V_I}{s} \cdot \frac{1+\frac{s}{\omega_{Z1}}}{1+\frac{s}{\omega_{P1}}} \cdot \frac{1+\frac{s}{\omega_{Z2}}}{\cdot 1+\frac{s}{\omega_{P2}}} \cdot \frac{1+\frac{s}{\frac{1}{R_C \cdot C_4}}}{1+s\frac{L_1}{R}+s^2 L_1 C_4}$$

Where:
G_{PWM} = PWM gain and
V_M = 1.5V, ramp peak to valley voltage of SC4602A/B.

The design guidelines for the SC4602A/B applications are as following:

1. Set the loop gain crossover corner frequency ω_C for given switching corner frequency ω_S =2pf_s,
2. Place an integrator at the origin to increase DC and low frequency gains,
3. Select ω_{Z1} and ω_{Z2} such that they are placed near ω_0 to damp the peaking and the loop gain has a -20dB/dec rate to go across the 0dB line for obtaining a wide bandwidth,
4. Cancel the zero from C_4's ESR by a compensator pole ω_{P1} (ω_{P1} = ω_{ESR} = 1/($R_C C_4$)),
5. Place a high frequency compensator pole ωp_2 (ωp_2 = pf_s) to get the maximum attenuation of the switching
ripple and high frequency noise with the adequate phase lag at ω_C.

The compensated loop gain will be as given in Figure 4:

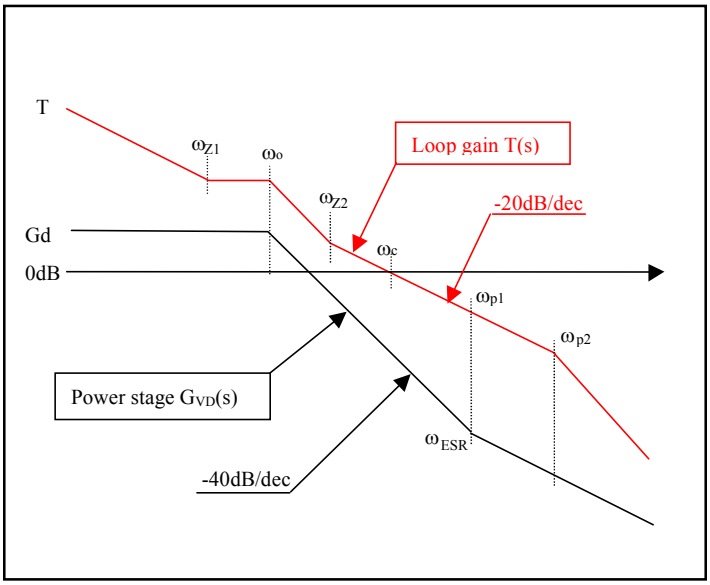


Figure 4. Asymptotic diagrams of power stage and its loop gain

Applications Information (Cont.)

Layout Guideline

In order to achieve optimal electrical, thermal and noise performance for high frequency converters, special attention must be paid to the PCB layouts. The goal of layout optimization is to identify the high di/dt loops and minimize them. The following guideline should be used to ensure proper functions of the converters.

1. A ground plane is recommended to minimize noises and copper losses, and maximize heat dissipation.
2. Start the PCB layout by placing the power components first. Arrange the power circuit to achieve a clean power flow route. Put all the connections on one side of the PCB with wide copper filled areas if possible.
3. The Vcc bypass capacitor should be placed next to the Vcc and GND pins.
4. The trace connecting the feedback resistors to the output should be short, direct and far away from the noise sources such as the phase node and switching components.
5. Minimize the traces between PDRV/NDRV and the gates of the MOSFETs to reduce their impedance to drive the MOSFETs.
6. Minimize the loop including input capacitors, top/bottom MOSFETs. This loop passes high di/dt current. Make sure the trace width is wide enough to reduce copper losses in this loop.
7. The PHASE connection to P-MOSFET for current sensing must use Kelvin connection.
8. Maximize the trace width of the loop connecting the inductor, bottom MOSFET and the output capacitors.
9. Connect the ground of the feedback divider and the compensation components directly to the GND pin of the SC4602A/B by using a separate ground trace. Then connect this pin to the ground of the output capacitor as close as possible.

A Design Example: 3.3V to1.5V @6A application with SC4602B (NH020 footprint)

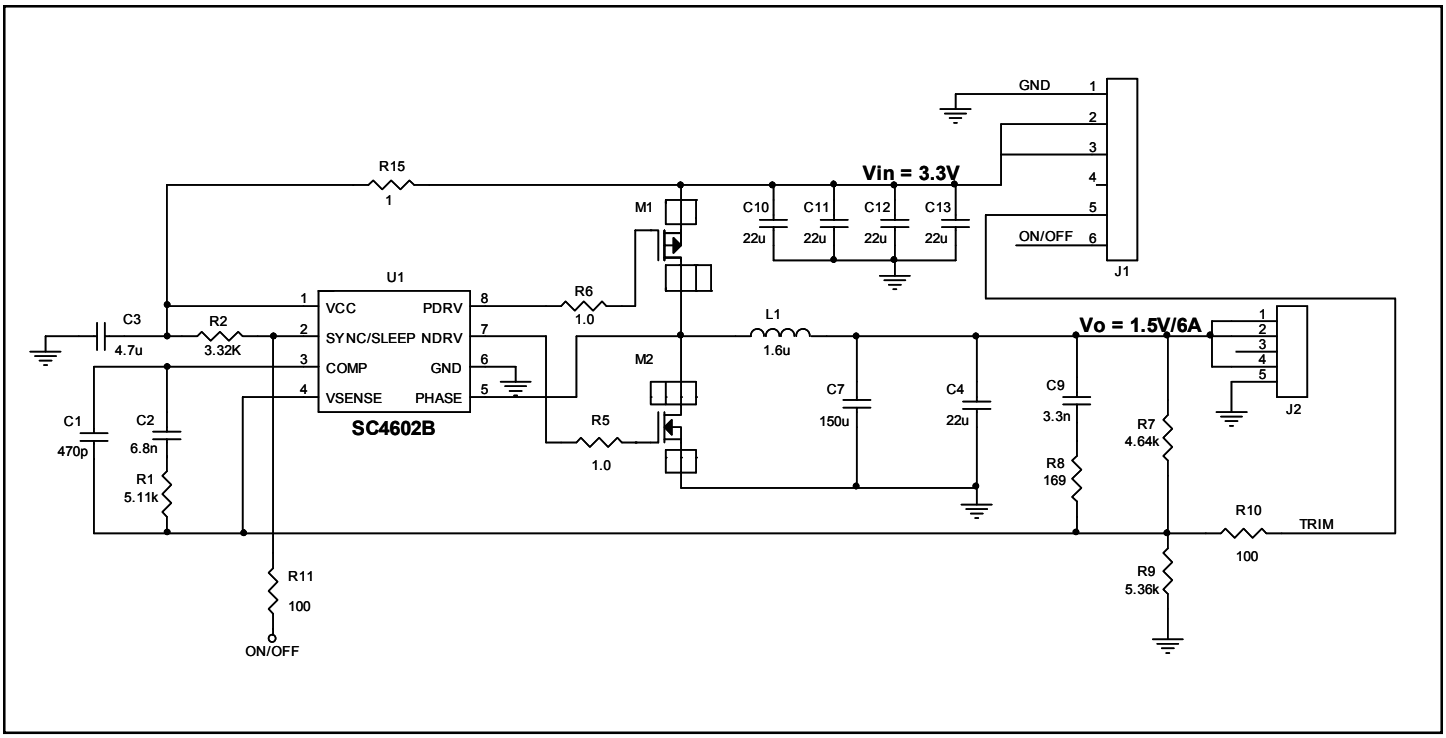


Figure 5. Schematic for 3.3V/1.5V@6A with SC4602B application

Bill of Materials - 3.3V to 1.5V @ 6A

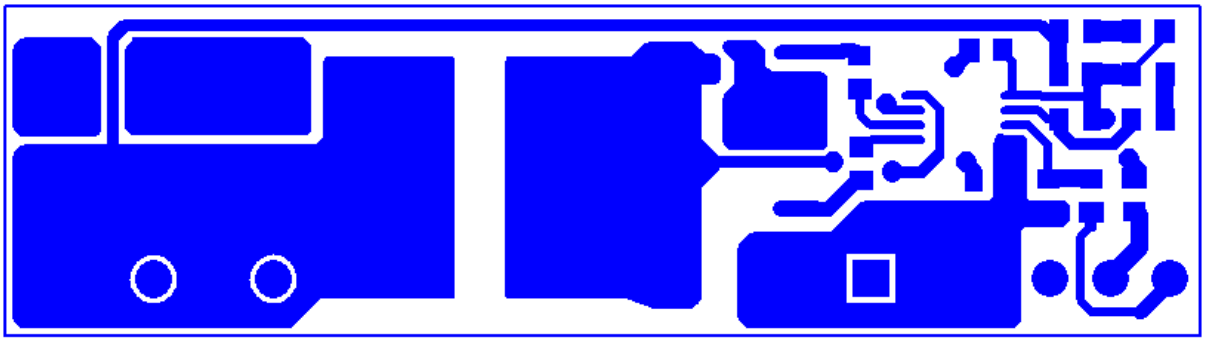
Item	Qty	Reference	Value	Part No./Manufacturer
1	1	C1	470pF	
2	1	C2	6.8nF	
3	1	C3	4.7uF	0805, ceramic
4	5	C4, C10, C11, C12, C13	22uF	TDK P/N: C3225X5R0J226M
5	1	C7	SP capacitor, 150uF, 15 mohm, 6.3V	Panasonic
6	1	C9	3.3nF	
7	1	J1	CON6	
8	1	J2	CON5	
9	1	L1	SMT power inductor, 1.6uH +/- 30%, 12.2A, 3.3 mohm max	Panasonic. P/N: ETQP6F1R6S
10	1	M1	FDS 6375, SO-8, Fairchild	SO-8 MOSFET P
11	1	M1	FDS 6680A, SO-8, Fairchild	SO-8 MOSFET N
12	1	R1	5.11k	
13	1	R2	3.32k	
14	1	R15	1	
15	2	R5, R6	1.0	
16	1	R7	4.64k	
17	1	R8	169	
18	1	R9	5.36k	
19	2	R10, R11	100	
20	1	U1	SC4602B	Semtech P/N: SC4602BIMSTR

Key components:
U1: SC4602B, Semtech
M1: FDS 6375, SO-8, Fairchild
M2: FDS 6680A, SO-8, Fairchild
C7: SP capacitor, 150uF, 15 mohm, 6.3V, Panasonic
L1: SMT power inductor, 1.6uH +/- 30%, 12.2A, 3.3 mohn max. ETQP6F1R6S Panasonic.
Unless specified, all resistors and capacitors are in SMD 0603 package.
Resistors are +/-1% and all capacitors are +/-20%

PCB Layout - 3.3V to 1.5V @ 6A

PCB layout information for 3.3V to1.5V @6A with SC4602B application (NH020 footprint)

Top



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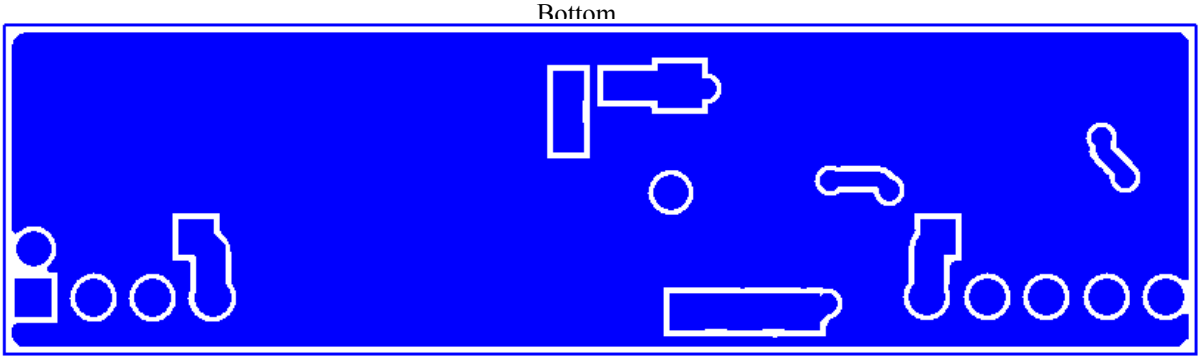

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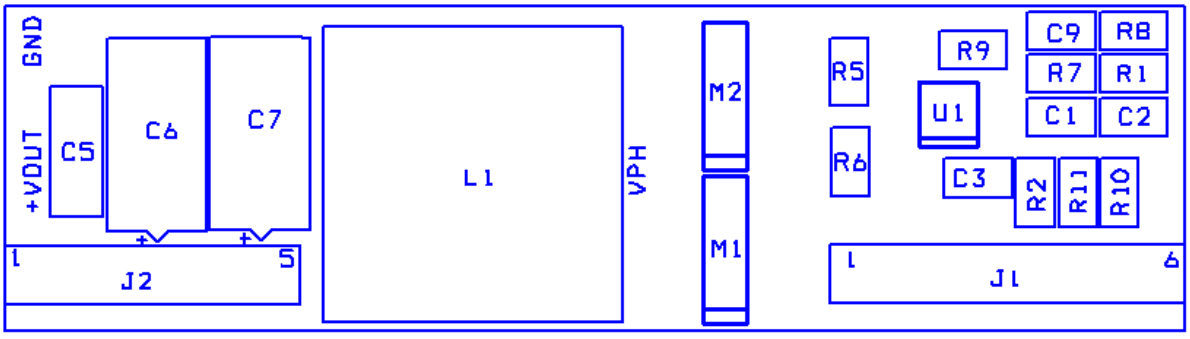

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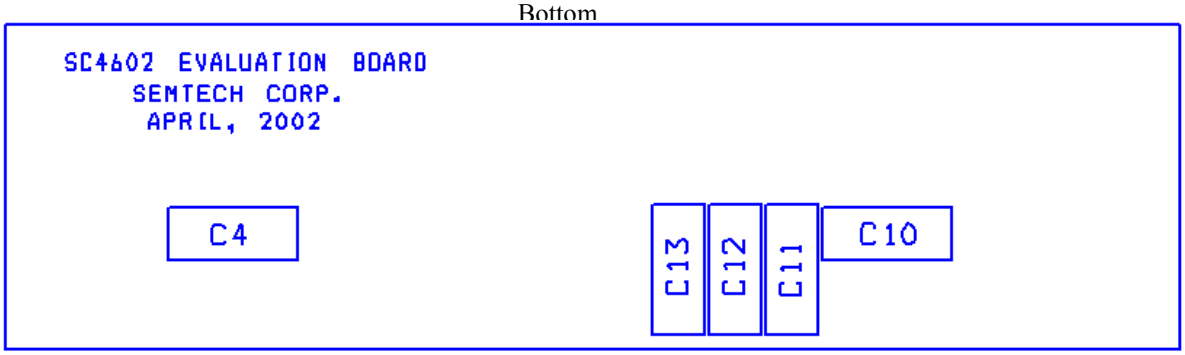
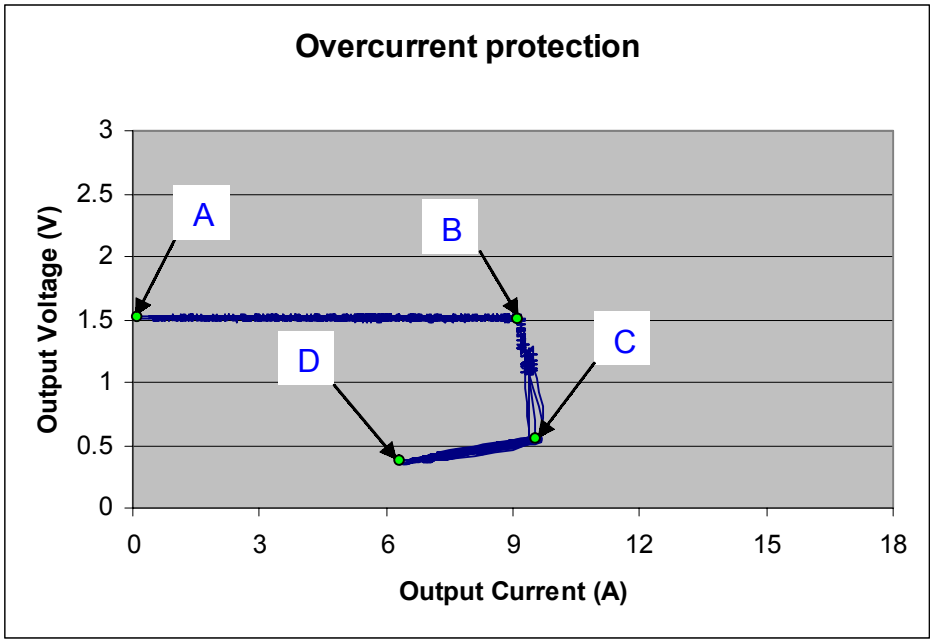


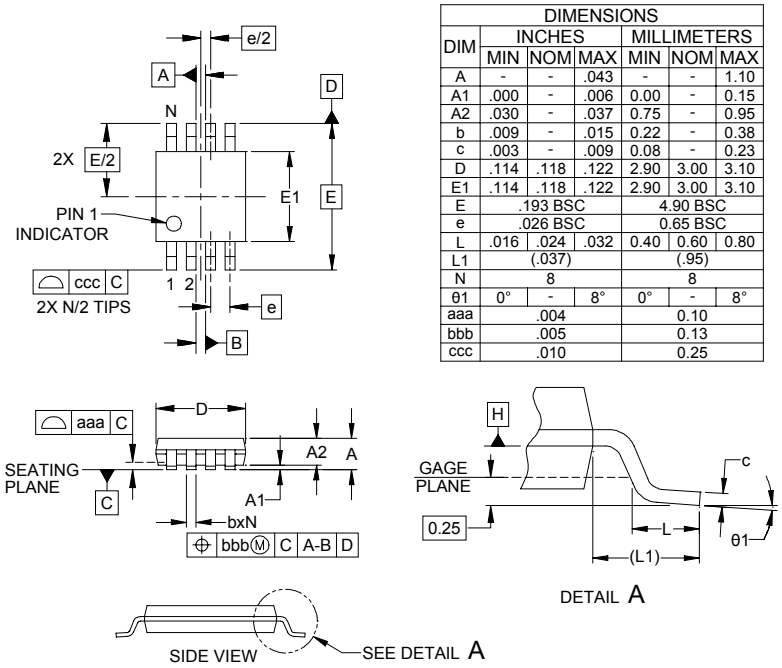
Typical Characteristic

Over current protection characteristic of SC4602B for 3.3V to1.5V @6A application:

The over current protection curve below is obtained by applying a gradually increased load while the load current and the output voltage are monitored and measured. When the load current is increased from 0 to 9A (over current trigger point), the output voltage is 1.5V, corresponding from Point A to Point B. As the load current increases further from 9A to 9.6A, the output voltage drops significantly from 1.5V (Point B) to 0.54V (Point C). Because an over current and a lower output voltage (0.54V<68.75%*1.5V=1.03V) are present at Point C, the SC4602B enters its HICCUP mode. Then the locus of the output current and the output voltage follows Line CD as shown in the curve. Due to the over current applied, the HICCUP protection will go back and forth on Line CD. This prevents excess power dissipation in the P-MOSFET during a short output conditio



Outline Drawing - MSOP-8

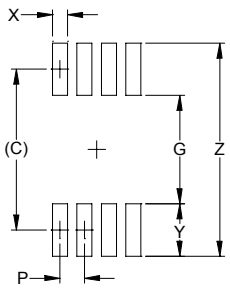


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.006	0.00	-	0.15
A2	.030	-	.037	0.75	-	0.95
b	.009	-	.015	0.22	-	0.38
c	.003	-	.009	0.08	-	0.23
D	.114	.118	.122	2.90	3.00	3.10
E1	.114	.118	.122	2.90	3.00	3.10
E	.193 BSC			4.90 BSC		
e	.026 BSC			0.65 BSC		
L	.016	.024	.032	0.40	0.60	0.80
L1	(.037)			(.95)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.005			0.13		
ccc	.010			0.25		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-187, VARIATION AA.

Land Pattern - MSOP-8



DIM	INCHES	MILLIMETERS
C	(.161)	(4.10)
G	.098	2.50
P	.026	0.65
X	.016	0.40
Y	.063	1.60
Z	.224	5.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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