SamHop Microelectronics Corp.

SC8650S

Ver 1.1

Dual N-Channel Enhancement Mode Field Effect Transistor

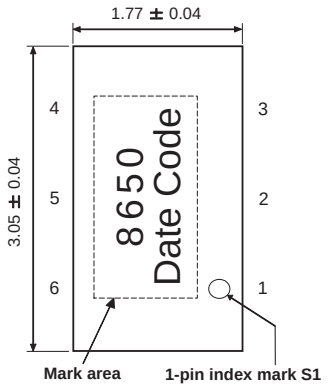
PRODUCT SUMMARY		
V_{SSS}	I_S	$R_{SS(ON)}$ (mΩ) Typ
12V	10A	2.6 @ VGS=4.5V
		2.7 @ VGS=4.0V
		2.9 @ VGS=3.8V
		3.3 @ VGS=3.1V
		4.1 @ VGS=2.5V

FEATURES

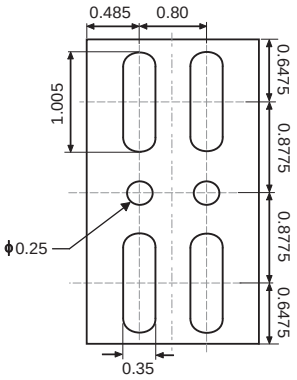
- Super high dense cell design for low $R_{DS(ON)}$.
- Rugged and reliable.
- Wafer level CSP.
- ESD Protected.

WLCSP

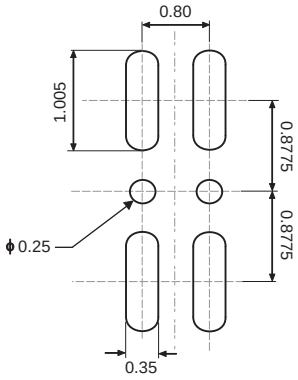
TOP VIEW



BOTTOM VIEW



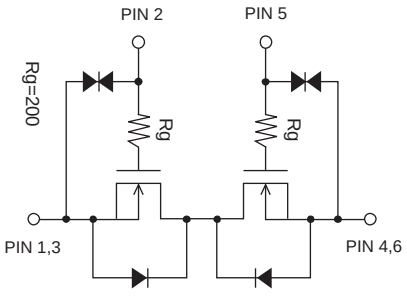
LAND PATTERN (REFERENCE)



Unit : mm

ABSOLUTE MAXIMUM RATINGS (T_A=25°C)

Symbol	Parameter	Limit	Units
V_{SSS}	Source-Source Voltage	12	V
V_{GSS}	Gate-Source Voltage	±8	V
I_S	Source Current-Continuous [c]	10	A
I_{SP}	-Pulsed [a c]	100	A
P_T	Total Power Dissipation	2.5	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C



PIN 1 : Source 1
PIN 2 : Gate 1
PIN 3 : Source 1
PIN 4 : Source 2
PIN 5: Gate 2
PIN 6 : Source 2

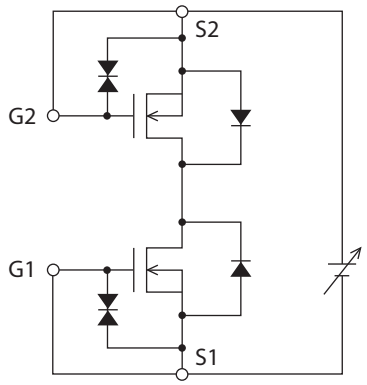
ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{SSS}	Source-Source Breakdown Voltage	V_{GS}=0V , I_S=1mA	12			V
I_{SSS}	Zero Gate Voltage Source Current	V_{SS}=10V , V_{GS}=0V			1	uA
I_{GSS}	Gate-Body Leakage Current	V_{GS}= ±5V , V_{SS}=0V			±1	uA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{SS}=V_{GS} , I_S=1mA	0.5		1.3	V
$R_{SS(ON)}$	Source-Source On-State Resistance	V_{GS}=4.5V , I_S=5.0A	1.9	2.6	3.4	m ohm
		V_{GS}=4.0V , I_S=5.0A	2.0	2.7	3.6	m ohm
		V_{GS}=3.8V , I_S=5.0A	2.1	2.9	3.8	m ohm
		V_{GS}=3.1V , I_S=5.0A	2.2	3.3	5.0	m ohm
		V_{GS}=2.5V , I_S=5.0A	2.8	4.1	6.3	m ohm
g_{FS}	Forward Transconductance	V_{SS}=5V , I_S=5.0A		19		S
SWITCHING CHARACTERISTICS [b]						
$t_{D(ON)}$	Turn-On Delay Time	V_{SS}=6V I_S=5A V_{GS}=4.5V		80		ns
t_r	Rise Time			570		ns
$t_{D(OFF)}$	Turn-Off Delay Time			38000		ns
t_f	Fall Time			17700		ns
Q_g	Total Gate Charge	V_{SS}=6V,I_S=5A, V_{GS}=4.5V		100		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V_{FSS}	Diode Forward Voltage	V_{GS}=0V,I_S=3A		0.75	1.2	V

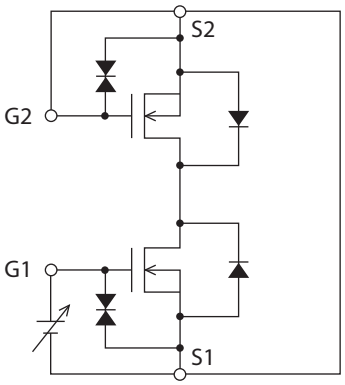
Notes

a.Pulse Test:Pulse Width ≤ 10us, Duty Cycle ≤ 1%.
b.Guaranteed by design, not subject to production testing.
c.Drain current limited by maximum junction temperature.

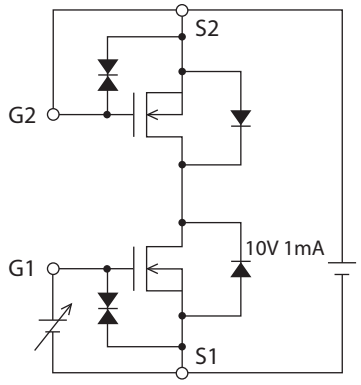
V_{SSS} / I_{SSS}



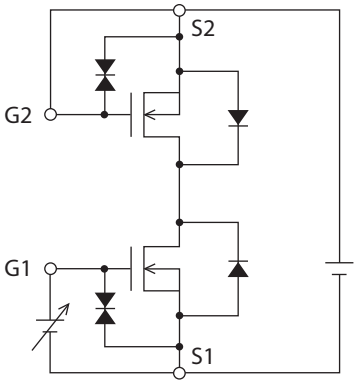
I_{GSS} (+) / (--)



V_{GS} (off)

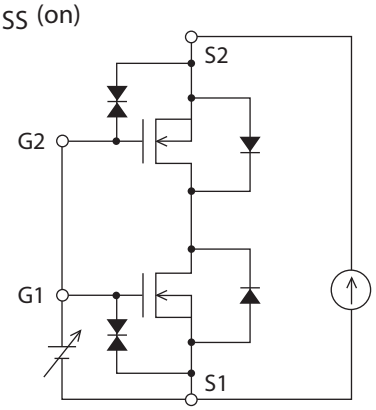


| yfs |

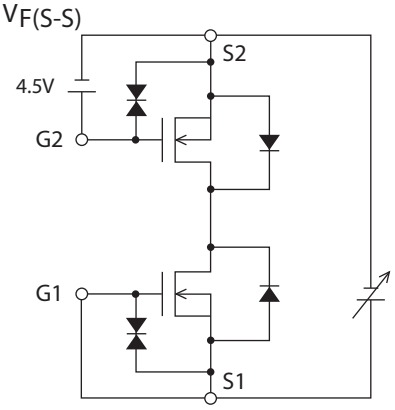


* Note: Connect the mesurement terminal reversely if you want to measure the FET2 side.

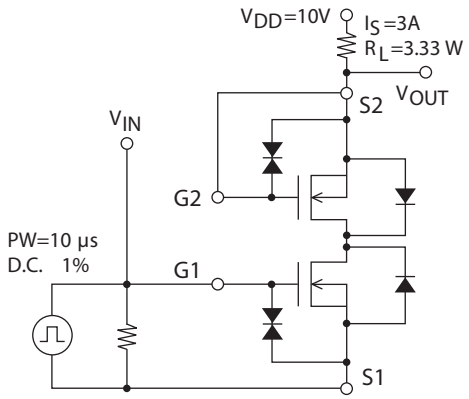
R_{SS} (on)



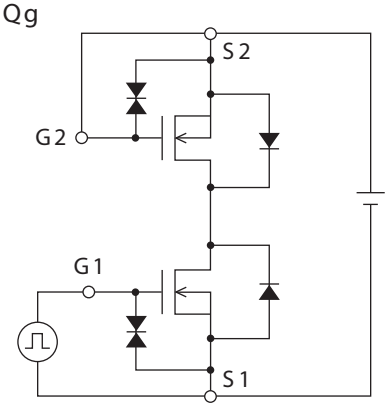
$V_{F(S-S)}$



$t_{d(on)}$, t_r, $t_{d(off)}$, t_f



Qg



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TOP MARKING DEFINITION

WLCSP