

T-35-25

TOPAZ

SEMICONDUCTOR

SD204, SD205

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

Sorted Chips in Waffle Pack	SD204CHP	SD205CHP
TO-205AF (TO-39) Package	SD204HD	SD205HD
Description	6.0 ohm, 25V	6.0 ohm, 25V

FEATURES

- Low Capacitance— c_{iss} 11pF typ.
- Inherently Temperature Stable by Design
- TTL Logic Compatible Input— $V_{GS(th)}$ 2.0V (max)

APPLICATIONS

- Broadband RF Power Amplifiers
- High Speed Switches and Drivers
- Pulse Amplifiers and Logic Buffers
- CMOS and TTL to High Current Interface

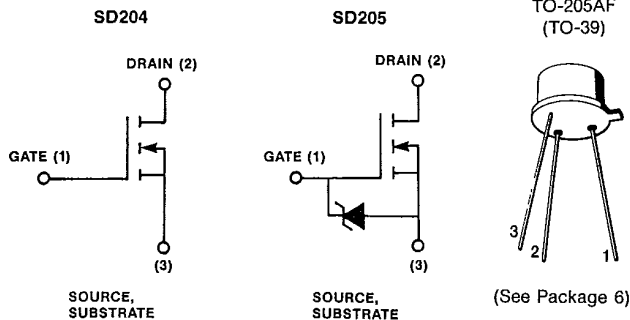
ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

V_{DS} Drain-Source Voltage	+25V
V_{DG} Drain-Gate Voltage	+25V
V_{GS} Gate-Source (Forward) Voltage	+20V
Gate-Source (Reverse) Voltage	-0.3V
I_D Continuous Drain Current (Note 1)	0.3A
Continuous Drain Current (Note 2)	0.7A
Peak Pulsed Drain Current	1.0A
P_D Continuous Power Dissipation	
$T_A = +25^\circ\text{C}$ (Note 1, Note 3)	1.0W
$T_C = +25^\circ\text{C}$ (Note 1, Note 4)	6.25W
Power Derating Factors (Note 1)	
Free Air	10mW/ $^\circ\text{C}$
Infinite Heat Sink	62.5mW/ $^\circ\text{C}$

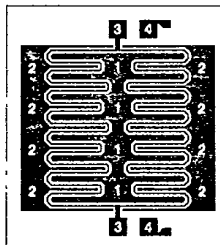
Thermal Resistance (Note 1)	
θ_{ja} Junction to Ambient	100 $^\circ\text{C}/\text{W}$
θ_{jc} Junction to Case	16 $^\circ\text{C}/\text{W}$
T_{op} Operating Junction Temperature Range	-55 to +125 $^\circ\text{C}$
T_{stg} Storage Temperature Range	-55 to +150 $^\circ\text{C}$

- Note 1: Not applicable to chips. Final value depends on mounting.
 Note 2: Pulse Test 80 μSec , 1% Duty Cycle
 Note 3: Free Air
 Note 4: Infinite Heat Sink

SCHEMATIC DIAGRAM



CHIP CONFIGURATION



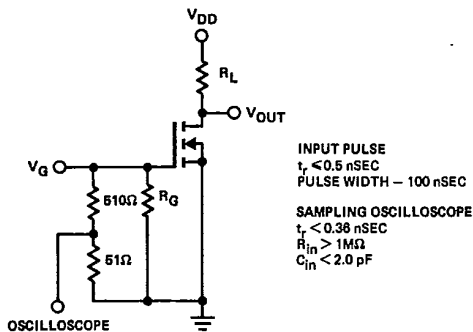
1—Drain 2—Source 3—Gate 4—Diode
 Minimum bonding required. One Drain, One Source (left), One Source (right), One Gate. Bond Gate and Adjacent Diode to Common Point to Connect Protective Diode.

Size: .040 x .044 x .013 inch.
 Body (Substrate) is backside contact.

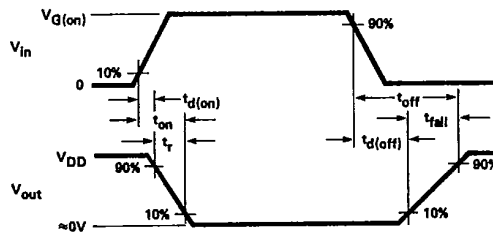
ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

#	CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	BV_{DSS}	Drain Source Breakdown Voltage	25			V	$I_D = 1.0\mu\text{A}, V_{GS} = 0$
2	$V_{GS(th)}$	Gate Source Threshold Voltage	0.5		2.0	V	$I_D = 1\text{mA}, V_{DS} = V_{GS}$
3	$I_{D(on)}$	Drain-Source ON Current	1.0			nA	$V_{DS} = 10\text{V}$ (Note 1) $V_{GS} = 10\text{V}$
4	I_{DSS}	Drain-Source OFF Leakage Current			1.0		$V_{DS} = 25\text{V}, V_{GS} = 0$
5	$r_{DS(on)}$	Drain-Source ON Resistance			8.0	ohms	$V_{GS} = 5\text{V}$ $I_D = 50\text{mA}$ (Note 1)
6					6.0		$V_{GS} = 10\text{V}$ $I_D = 500\text{mA}$ (Note 1)
7					6.0		
8	I_{GSS}	Gate Body Leakage Current	SD205		1.0	μA	$V_{GS} = 20\text{V}, V_{DS} = 0$
8A			SD204		± 10	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$
9	g_{fs}	Common-Source Forward Transconductance	100			mmhos	$V_{DS} = 15\text{V}, I_D = 200\text{mA}$ $f = 1\text{KHz}$ (Note 1)
10	C_{iss}	Common-Source Input Capacitance		11	13	pF	$V_{DS} = 10\text{V}, V_{GS} = 0$ $f = 1\text{MHz}$
11	C_{oss}	Common-Source Output Capacitance			8.0		
12	C_{rss}	Common-Source Reverse Transfer Capacitance			3.0		
13	$t_{d(on)}$	Turn-On Delay Time		<1.0	2.0		
14	t_r	Rise Time		1.0	3.0	nS	$V_{DD} = 10\text{V}, V_{G(on)} = 10\text{V}$ $R_L = 133\Omega, R_G = 51\Omega$
15	t_{off}	Turn-off Time		3.0	5.0		
16	NF	Common-Source Noise Figure			4.5		
17	G_{PS}	Common-Source Power Gain	9.0				$V_{DS} = 10\text{V}, I_D = 100\text{mA}$ $f = 300\text{MHz}$

SWITCHING TIMES TEST CIRCUIT



TEST WAVEFORMS

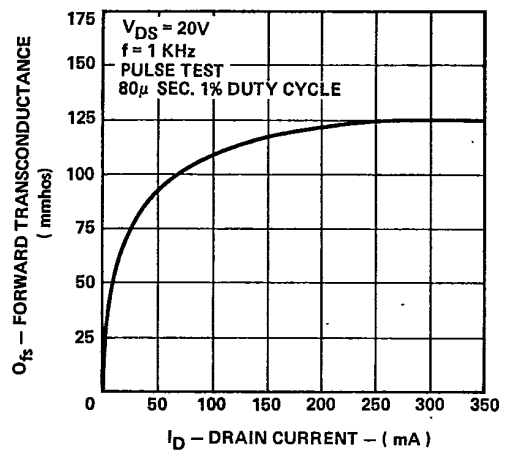


T-35-25
SD204, SD205

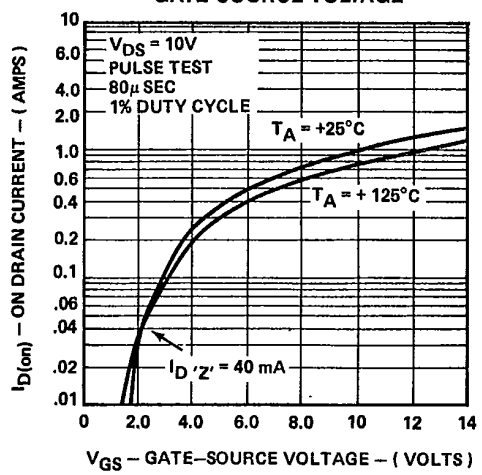


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise specified)

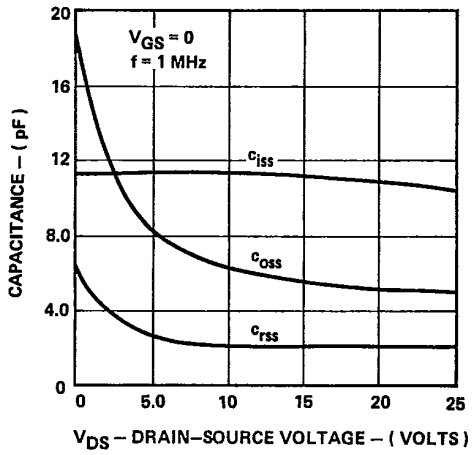
FORWARD TRANSCONDUCTANCE
—VS—
ON DRAIN CURRENT



ON DRAIN CURRENT
—VS—
GATE-SOURCE VOLTAGE



CAPACITANCES
—VS—
DRAIN-SOURCE VOLTAGE



DRAIN-SOURCE ON RESISTANCE
—VS—
GATE-SOURCE VOLTAGE

