

N-Channel 100-V (D-S) Super Trench Power MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A) ^a	Q _g (Typ.)
100	0.0082 at V _{GS} = 10 V	15.5	27.9 nC
	0.0095 at V _{GS} = 7.5 V	14.8	
	0.0105 at V _{GS} = 6.0 V	14.0	

FEATURES

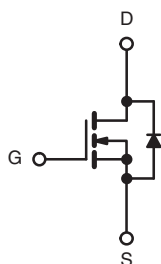
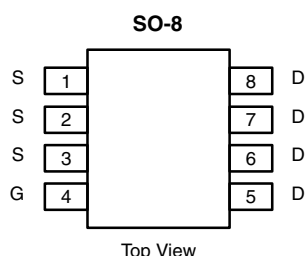
- Super Trench technology Power MOSFET
- Excellent gate charge x Rds (on) product(FOM)
- Very low on-resistance Rds (on)
- 100 % R_g and UIS Tested



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- DC/DC Primary Side Switch
- Telecom/Server
- Motor Drive Control
- Synchronous Rectification



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	100	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	15.5	
		T _C = 70 °C	13	
		T _A = 25 °C	10.2 ^{b, c}	
		T _A = 70 °C	7.4 ^{b, c}	
Pulsed Drain Current (t = 300 μs)	I _{DM}	70	A	
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C		7
		T _A = 25 °C		3.1 ^{b, c}
Single Pulse Avalanche Current	I _{AS}	30	mJ	
Avalanche Energy	E _{AS}	45		
Maximum Power Dissipation	P _D	T _C = 25 °C	7.8	
		T _C = 70 °C	5	
		T _A = 25 °C	3.5 ^{b, c}	
		T _A = 70 °C	2.2 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	29	35	°C/W	
Maximum Junction-to-Foot (Drain)	R _{thJF}	13	16		

Notes:

- Based on T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under steady state conditions is 80 °C/W.

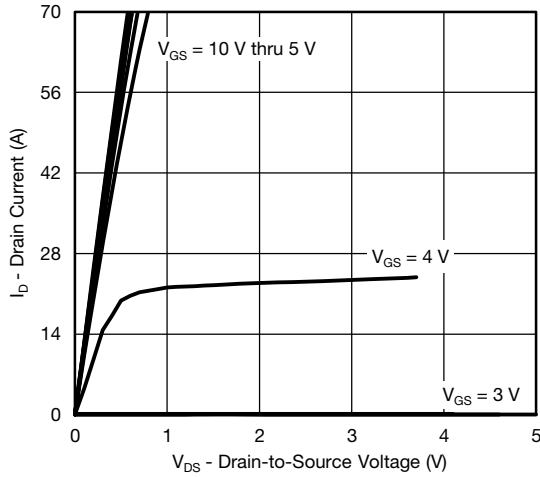
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		67		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-6.4		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2		3.3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$			0.0082	Ω
		$V_{GS} = 7.5\text{ V}, I_D = 12\text{ A}$			0.0095	
		$V_{GS} = 6.0\text{ V}, I_D = 10\text{ A}$			0.0105	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		54		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		3410		pF
Output Capacitance	C_{oss}			790		
Reverse Transfer Capacitance	C_{rss}			160		
Total Gate Charge	Q_g	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		45.6	69	nC
		$V_{DS} = 50\text{ V}, V_{GS} = 6\text{ V}, I_D = 10\text{ A}$		27.9	42	
Gate-Source Charge	Q_{gs}			8.5		
Gate-Drain Charge	Q_{gd}			9.2		
Output Charge	Q_{oss}	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		63	95	
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.4	1.3	2.6	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 5\text{ }\Omega$ $I_D \equiv 10\text{ A}, V_{GEN} = 7.5\text{ V}, R_g = 1\text{ }\Omega$		16	32	ns
Rise Time	t_r			11	22	
Turn-Off Delay Time	$t_{d(off)}$			35	70	
Fall Time	t_f			10	20	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 5\text{ }\Omega$ $I_D \equiv 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		14	28	
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			36	70	
Fall Time	t_f			10	20	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			7	A
Pulse Diode Forward Current ^a	I_{SM}				70	
Body Diode Voltage	V_{SD}	$I_S = 5\text{ A}$		0.75	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		49	95	ns
Body Diode Reverse Recovery Charge	Q_{rr}			58	115	nC
Reverse Recovery Fall Time	t_a			21		ns
Reverse Recovery Rise Time	t_b			28		

Notes:

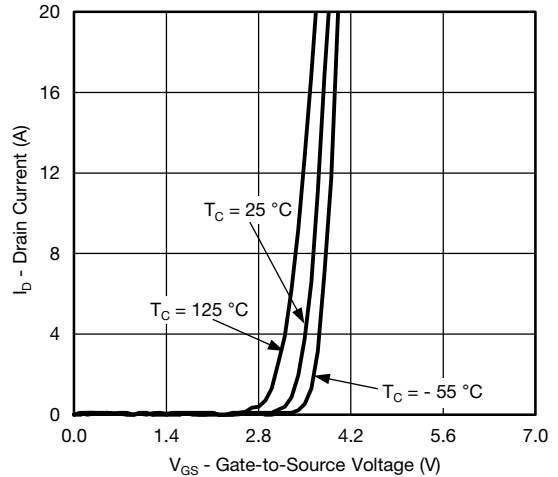
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

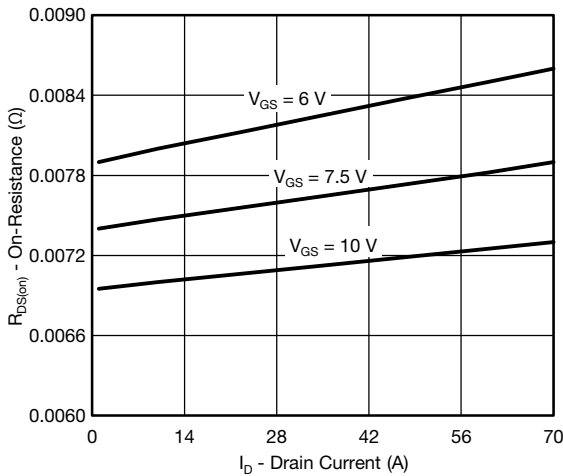
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



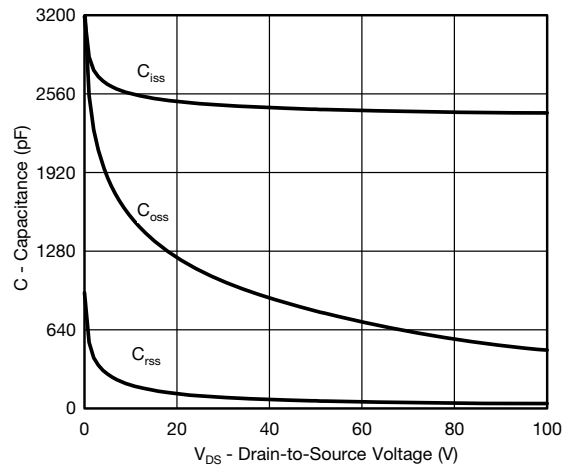
Output Characteristics



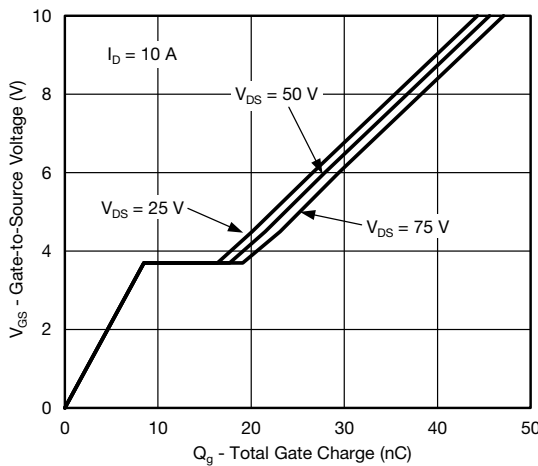
Transfer Characteristics



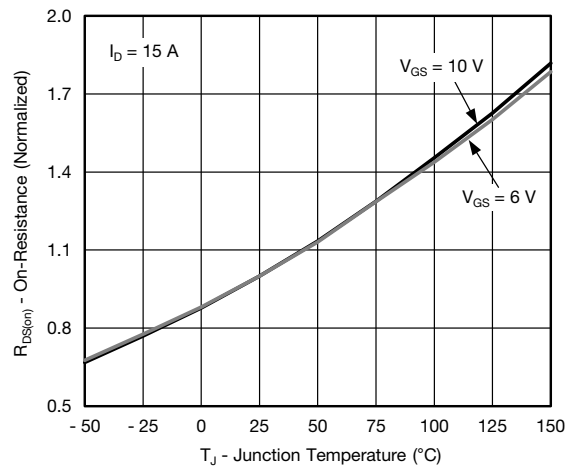
On-Resistance vs. Drain Current



Capacitance

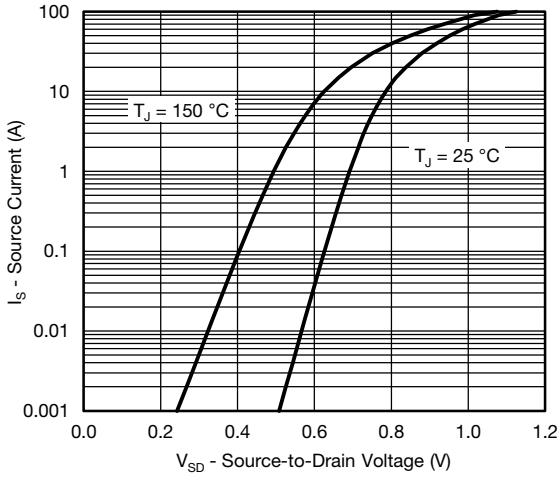


Gate Charge

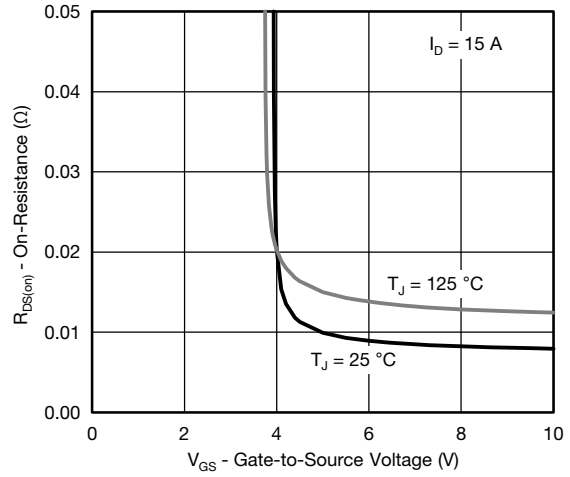


On-Resistance vs. Junction Temperature

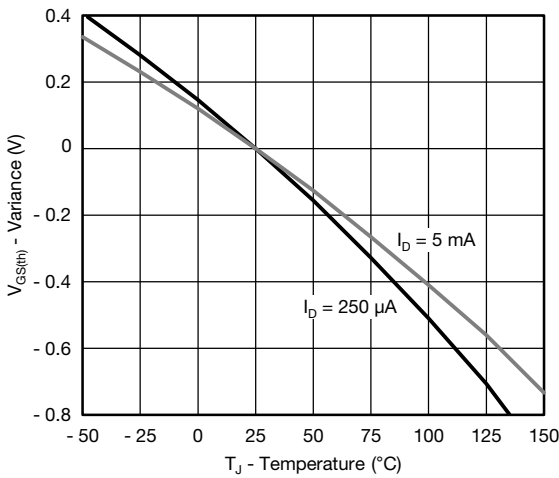
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



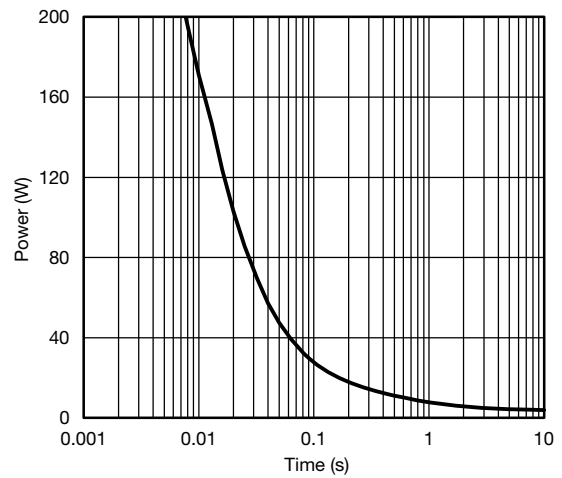
Source-Drain Diode Forward Voltage



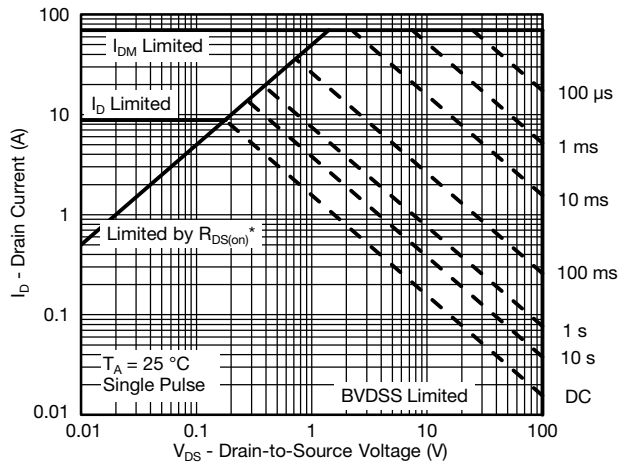
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

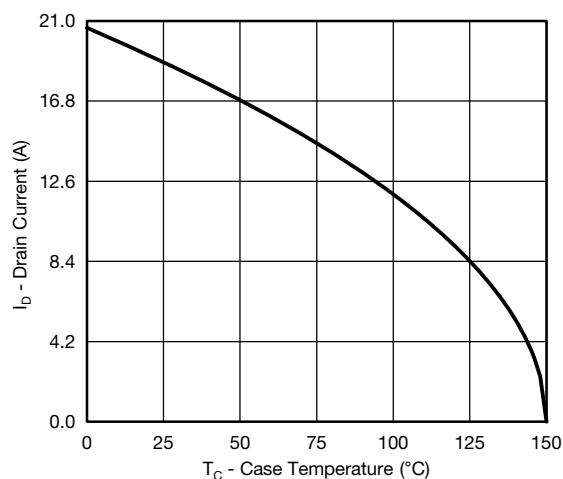


Single Pulse Power, Junction-to-Ambient

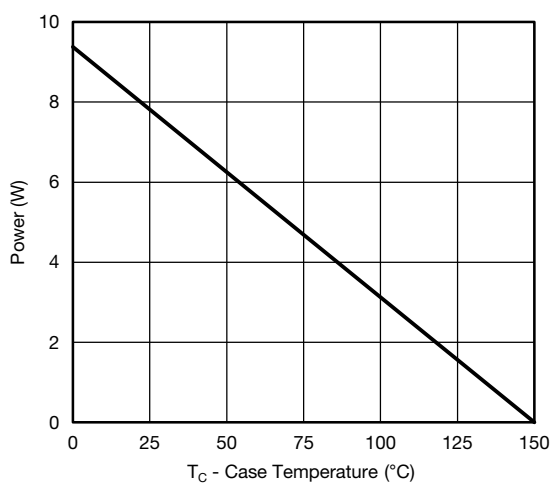


Safe Operating Area, Junction-to-Ambient

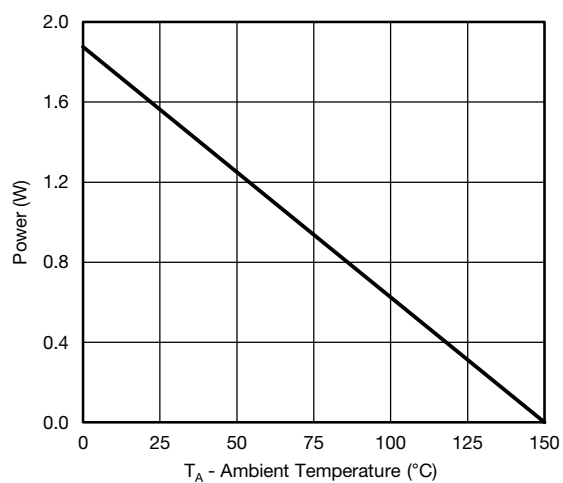
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



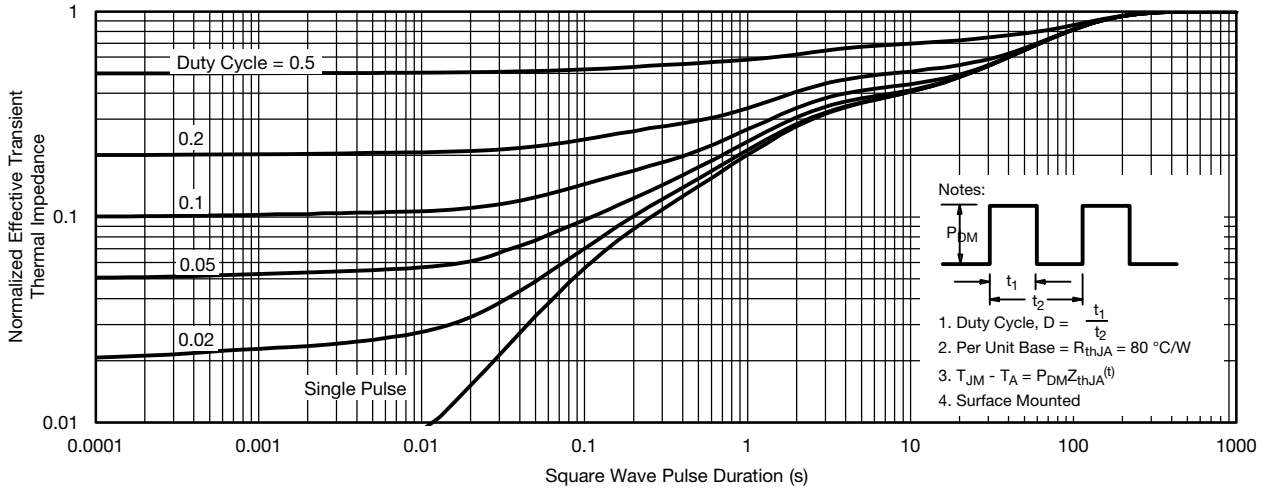
Power, Junction-to-Foot



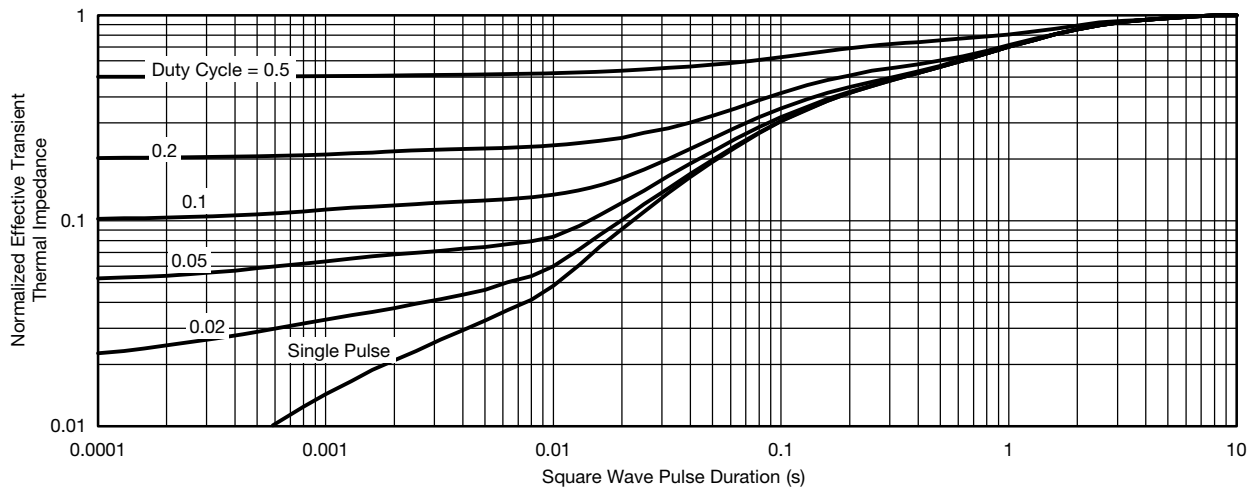
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

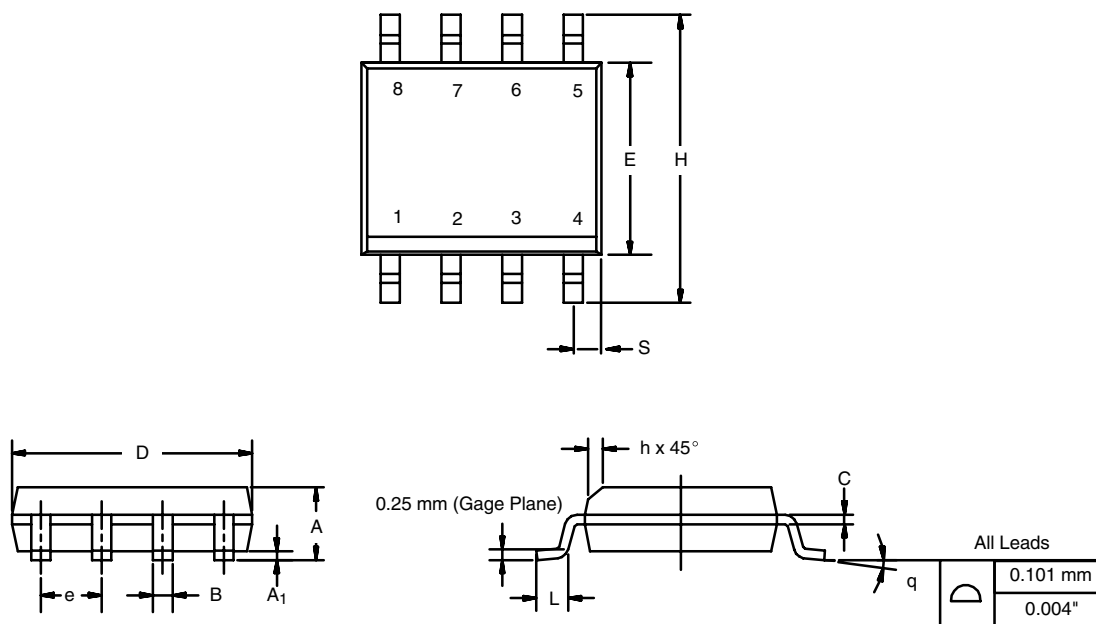


Normalized Thermal Transient Impedance, Junction-to-Ambient



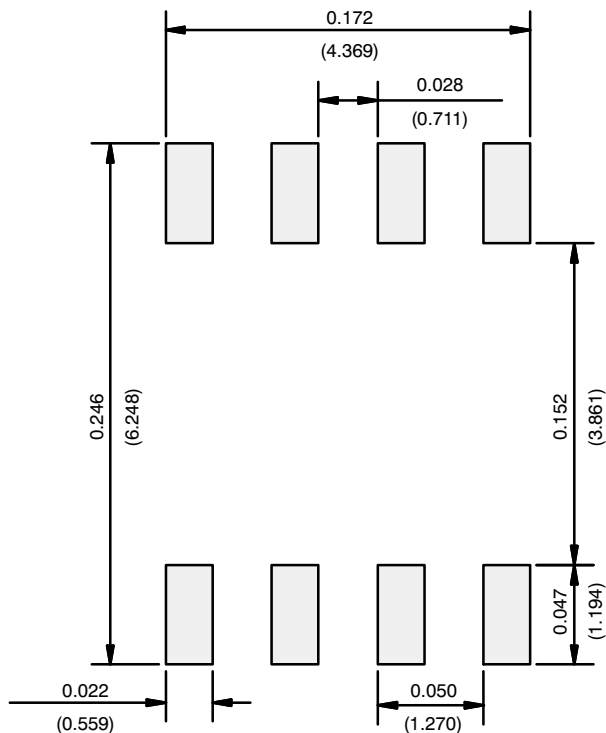
Normalized Thermal Transient Impedance, Junction-to-Foot

SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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