

N-Channel Synchronous MOSFETs With Break-Before-Make

DESCRIPTION

The Si4724CY N-Channel synchronous MOSFET with break-before-make (BBM) is a high speed driver designed to operate in high frequency DC/DC switchmode power supplies. Its purpose is to simplify the use of N-Channel MOSFETs in high frequency buck regulators. This device is designed to be used with any single output PWM IC or ASIC to produce a highly efficient low cost synchronous rectifier converter. A synchronous enable pin (disable = low, enable = high) controls the synchronous function for light load conditions.

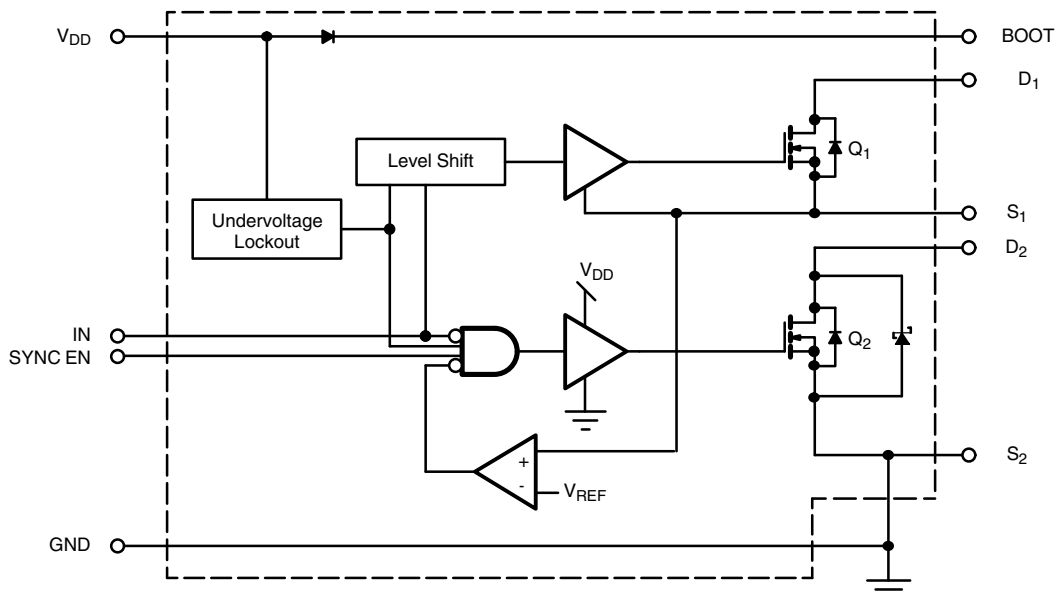
The Si4724CY is packaged in Vishay Siliconix's high performance LITTLE FOOT® SO-16 package.

FEATURES

- 0 V to 30 V operation
- Driver impedance-3
- Undervoltage lockout
- Fast switching times
- 30 V MOSFETs
- High side: 0.0375 at $V_{DD} = 4.5\text{ V}$
- Low side: 0.029 at $V_{DD} = 4.5\text{ V}$
- Switching frequency: 250 kHz to 1 MHz
- Integrated schottky



FUNCTIONAL BLOCK DIAGRAM



| ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | |
|--|----------------------------------|----------------|-------------------------|------------------|
| Parameter | | Symbol | Steady State | Unit |
| Logic Supply | | V_{DD} | 7 | V |
| Logic Inputs | | V_{IN} | - 0.7 to $V_{DD} + 0.3$ | |
| Drain Voltage | | V_{D1} | 30 | |
| Bootstrap Voltage | | V_{BOOT} | $V_{S1} + 7$ | |
| Synchronous pin Voltage | | V_{SYNC} | - 0.7 to $V_{DD} + 0.3$ | |
| Continuous Drain Current | $T_A = 25\text{ }^\circ\text{C}$ | I_{D1} | 5.1 | A |
| | $T_A = 70\text{ }^\circ\text{C}$ | | 4.09 | |
| | $T_A = 25\text{ }^\circ\text{C}$ | I_{D2} | 6.5 | |
| | $T_A = 70\text{ }^\circ\text{C}$ | | 5.2 | |
| Maximum Power Dissipation ^a | | P_D | 1.2 | W |
| Operating Junction and Storage Temperature Range | Driver | T_J, T_{stg} | - 65 to 125 | $^\circ\text{C}$ |
| | MOSFETs | | - 65 to 150 | |

Notes:

a. Surface mounted on 1" x 1" FR4 board, full copper two sides.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| RECOMMENDED OPERATING CONDITIONS | | | | |
|---|--|------------|---------------------------------|------------------|
| Parameter | | Symbol | Steady State | Unit |
| Drain Voltage | | V_{D1} | 0 to 30 | V |
| Logic Supply | | V_{DD} | 4.5 to 5.5 | |
| Input Logic High Voltage | | V_{IH} | $0.7 \times V_{DD}$ to V_{DD} | |
| Input Logic Low Voltage | | V_{IL} | - 0.3 to $0.3 \times V_{DD}$ | |
| Bootstrap Capacitor | | C_{BOOT} | 0.1 to 1 | μ |
| Ambient Temperature | | T_A | - 40 to 85 | $^\circ\text{C}$ |

| THERMAL RESISTANCE RATINGS | | | | | |
|--|--------------|-------------|---------|---------|--------------------|
| Parameter | | Symbol | Typical | Maximum | Unit |
| Highside Junction-to-Ambient ^a | Steady State | R_{thJA1} | 85 | 105 | $^\circ\text{C/W}$ |
| Lowside Junction-to-Ambient ^a | | R_{thJA2} | 68 | 85 | |
| Highside Junction-to-Foot (Drain) ^b | | R_{thJF1} | 28 | 35 | |
| Lowside Junction-to-Foot (Drain) ^b | | R_{thJF2} | 19 | 24 | |

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. Junction-to-foot thermal impedance represents the effective thermal impedance of all heat carrying leads in parallel and is intended for use in conjunction with the thermal impedance of the PC board pads to ambient ($R_{thJA} = R_{thJF} + R_{thPCB-A}$). It can also be used to estimate chip temperature if power dissipation and the lead temperature of a heat carrying (drain) lead is known.



| SPECIFICATIONS | | | | | | | |
|---|------------------|---|--|------|------|---------------|------------------|
| Parameter | Symbol | Test Conditions Unless Specified $T_A = 25\text{ }^\circ\text{C}$ $4.5\text{ V} < V_{DD} < 5.5\text{ V}, 4.5\text{ V} < V_{D1} < 30\text{ V}$ | Limits | | | Unit | |
| | | | Min. | Typ. | Max. | | |
| Power Supplies | | | | | | | |
| Logic Voltage | V_{DD} | | 4.5 | | 5.5 | V | |
| Logic Current | $I_{DD(EN)}$ | $V_{DD} = 4.5\text{ V}, V_{IN} = 4.5\text{ V}$ | | 280 | 500 | μA | |
| | $I_{DD(DIS)}$ | $V_{DD} = 4.5\text{ V}, V_{IN} = 0\text{ V}$ | | 220 | 500 | | |
| Logic Input | | | | | | | |
| Logic Input Voltage (V_{IN}) | High | V_{IH} | $V_{DD} = 4.5$ $-40\text{ }^\circ\text{C} \leq T_A \leq 85\text{ }^\circ\text{C}$ | 3.15 | 2.3 | V | |
| | Low | V_{IL} | | -0.3 | 2.25 | | 0.8 |
| Protection | | | | | | | |
| Break-Before-Make Reference | V_{BBM} | $V_{DD} = 5.5$ | | 2.4 | | V | |
| Undervoltage Lockout | V_{UVLO} | SYNC = 4.5 | 3.75 | 4 | 4.25 | | |
| Undervoltage Lockout Hysteresis | V_H | | | | 0.4 | | |
| MOSFET Drivers | | | | | | | |
| Driver Impedance | R_{DR1} | $V_{DD} = 4.5\text{ V}$ | Driver 1 | | 3 | V | |
| | R_{DR2} | | Driver 2 | | 2 | | |
| MOSFETs | | | | | | | |
| Drain-Source Voltage | V_{DS} | $I_D = 250\text{ }\mu\text{A}$ | 30 | | | V | |
| Drain Source On State Resistance ^a | $R_{DS(on)1}$ | $V_{DD} = 4.5\text{ V}, I_D = 5\text{ A}$ $T_A = 25\text{ }^\circ\text{C}$ | Q1 | | 30 | 37.5 | $\text{m}\Omega$ |
| | $R_{DS(on)2}$ | | Q2 | | 24 | 29 | |
| Diode Forward Voltage ^a | V_{SD1} | $I_S = 2\text{ A}, V_{GS} = 0$ | Q1 | | 0.7 | 1.1 | V |
| | V_{SD2} | | Q2 | | 0.7 | 1.1 | |
| Dynamic^b (Unless Specified-$F_s = 250\text{ kHz}, V_{IN} = 12\text{ V}, V_{DD} = 5\text{ V}, I = 5\text{ A}$, Refer to Switching Test Setup) | | | | | | | |
| Turn Off Delay | $t_{d(off)1}$ | See Timing Diagram | V_{IN} to G_1 | | 28 | 56 | ns |
| | $t_{d(off)2}$ | | V_{IN} to G_2 | | 17 | 40 | |
| Δt | Δt_{1-2} | | G_1 to G_2 | | 16 | 32 | |
| | Δt_{2-1} | | G_2 to G_1 | | 38 | 80 | |
| Source-Drain Reverse Recovery Time- Q_2 | t_{frr} | | $I_F 2.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ | | 50 | 80 | |

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

| SCHOTTKY SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | |
|--|----------|---|-----|-------|-------|------|
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
| Forward Voltage Drop | V_F | $I_F = 1\text{ A}$ | | 0.47 | 0.50 | V |
| | | $I_F = 1\text{ A}, T_J = 125\text{ }^\circ\text{C}$ | | 0.36 | 0.42 | |
| Maximum Reverse Leakage Current | I_{rm} | $V_r = 30\text{ V}$ | | 0.004 | 0.100 | mA |
| | | $V_r = 30\text{ V}, T_J = 100\text{ }^\circ\text{C}$ | | 0.7 | 10 | |
| | | $V_r = -30\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | | 3 | 20 | |
| Junction Capacitance | C_T | $V_r = 10\text{ V}$ | | 50 | | pF |

APPLICATION CIRCUIT

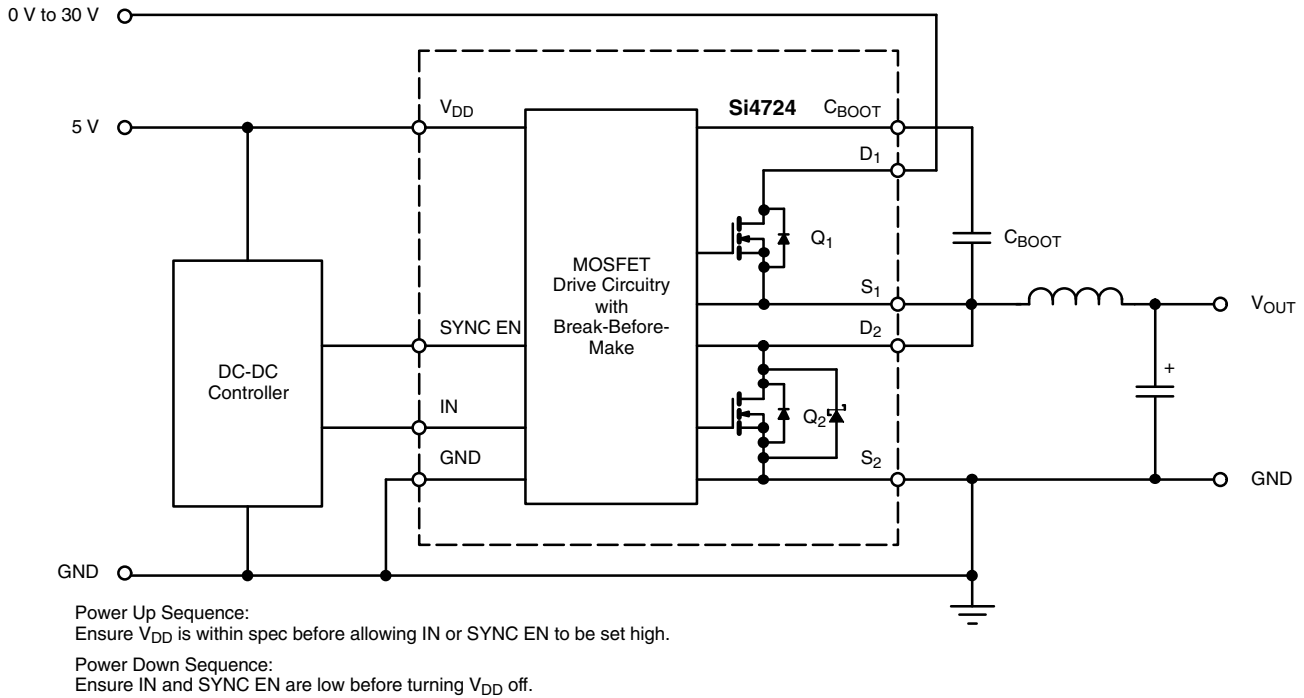
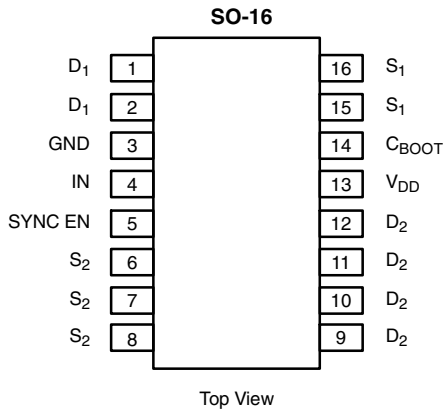


Figure 1.

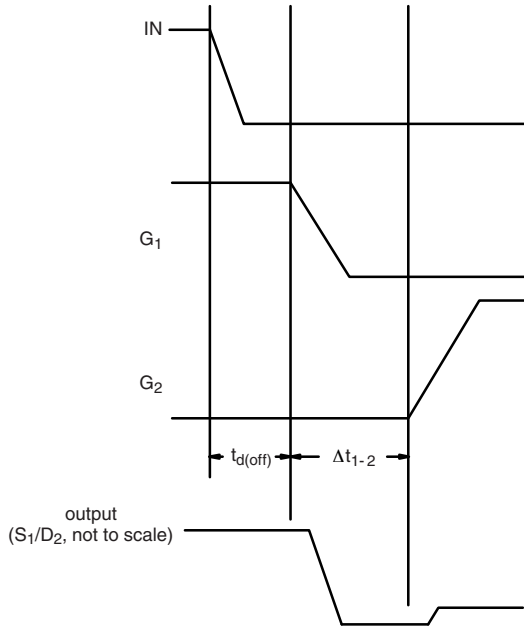
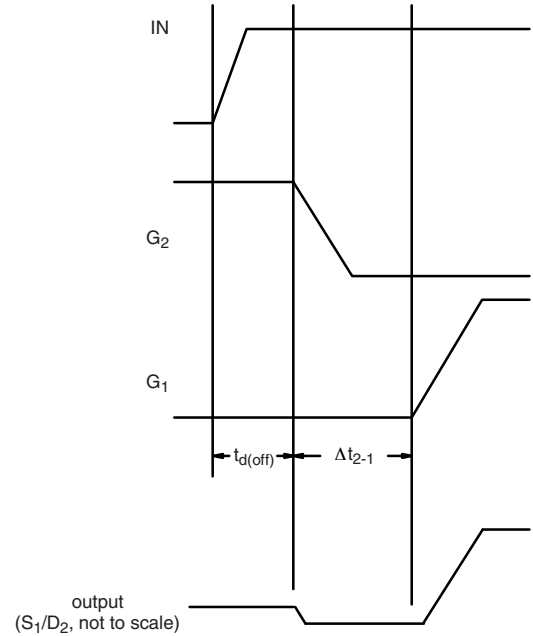
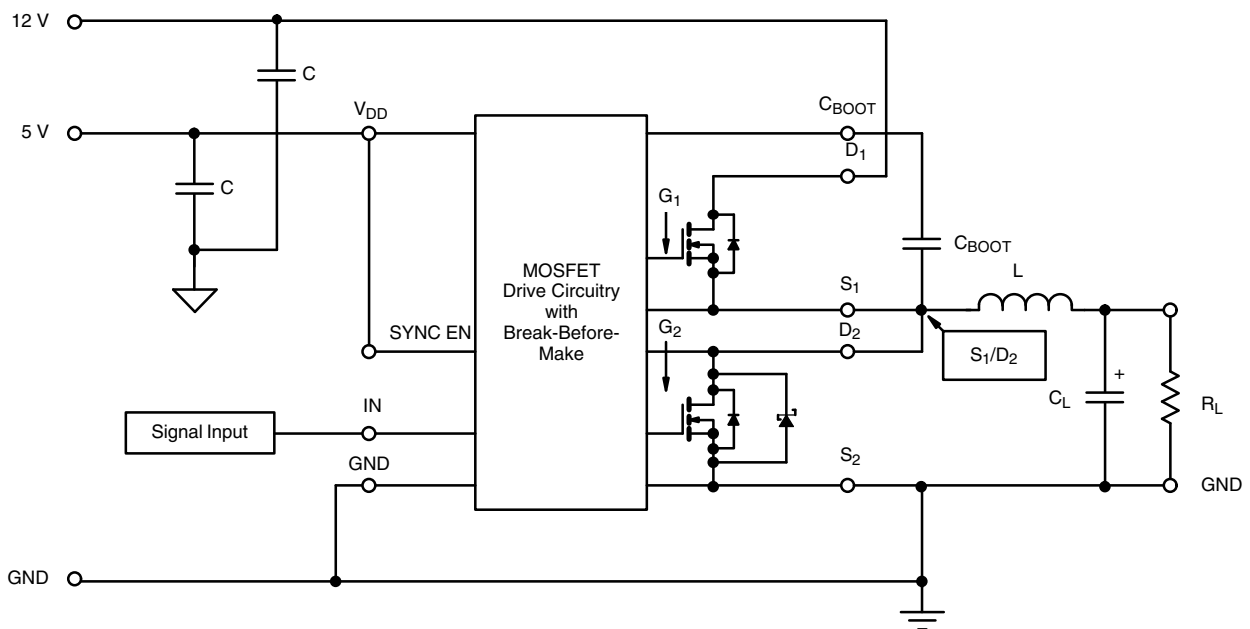
PIN CONFIGURATION



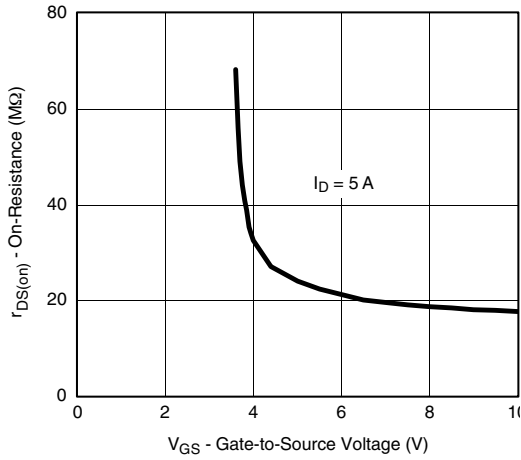
Ordering Information: Si4724CY-T1
Si4724CY-T1-E3 (Lead (Pb)-free)

| TRUTH TABLE | | | |
|-------------|-----|-------|-------|
| Sync EN | CLK | Q_1 | Q_2 |
| H | H | ON | OFF |
| H | L | OFF | ON |
| L | H | ON | OFF |
| L | L | OFF | OFF |

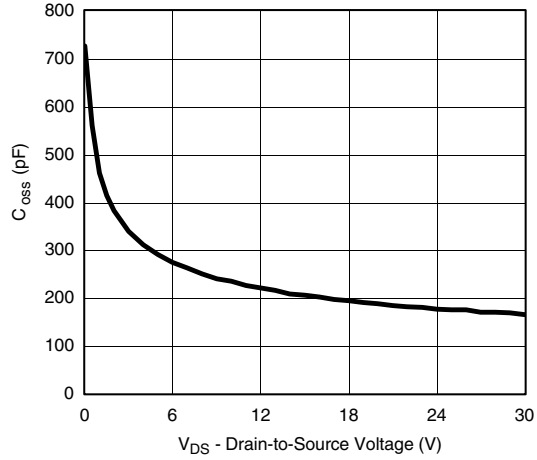
| PIN DESCRIPTION | | |
|-----------------|------------|---|
| Pin Number | Symbol | Description |
| 1, 2 | D_1 | Highside MOSFET Drain |
| 3 | GND | Ground |
| 4 | IN | Input Logic Signal |
| 5 | SYNC EN | Synchronous Enable |
| 6, 7, 8 | S_2 | Lowside MOSFET Source |
| 9, 10, 11, 12 | D_2 | Lowside MOSFET Drain |
| 13 | V_{DD} | Logic Supply, decoupling to GND with a cap is strongly recommended. |
| 14 | C_{BOOT} | Bootstrap Capacitor for Upper MOSFET |
| 15, 16 | S_1 | Highside MOSFET Source |

TIMING DIAGRAM

Figure 2. Δt_{1-2}

Figure 3. Δt_{2-1}
SWITCHING TEST SET-UP

Figure 4.

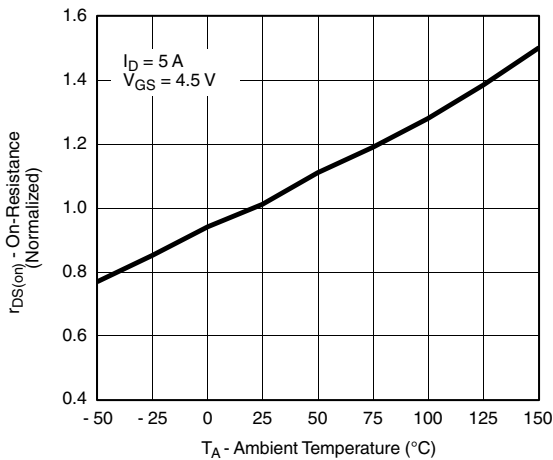
TYPICAL CHARACTERISTICS (25 °C unless noted)



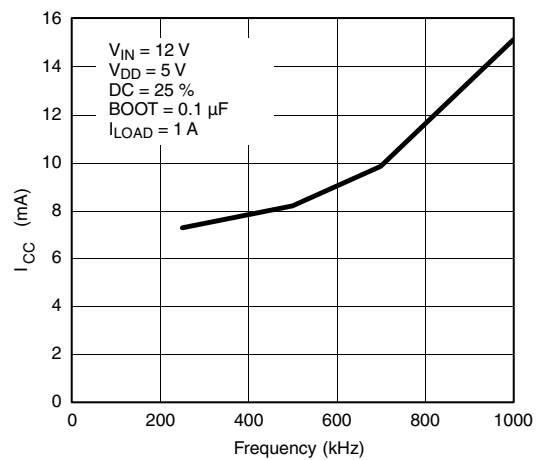
On-Resistance vs. Gate-to-Source Voltage (Q_1)



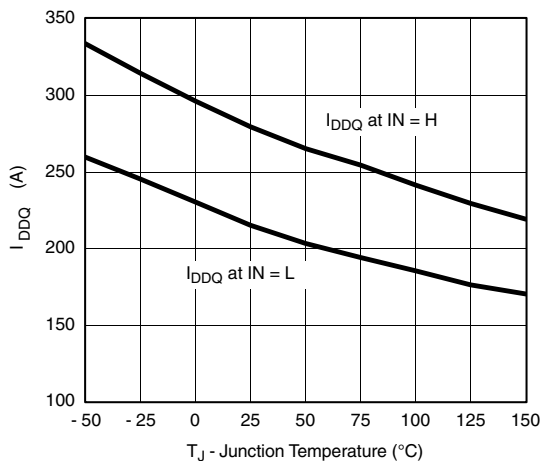
Output Capacitance vs. Drain Voltage (Q_1 and Q_2)



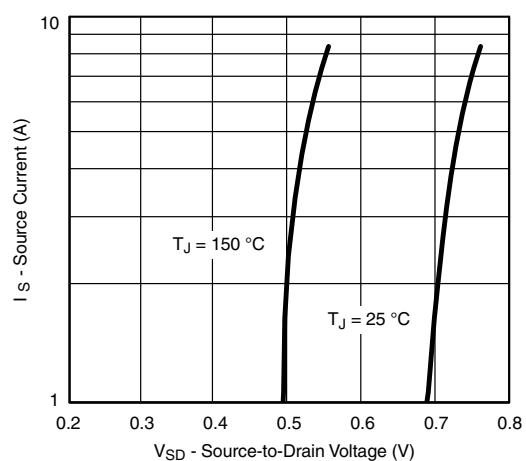
On-Resistance vs. Ambient Temperature



I_{CC} vs. Frequency

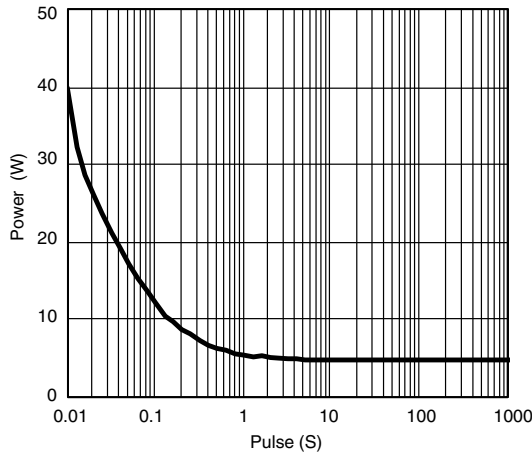


Input Current vs. Junction Temperature

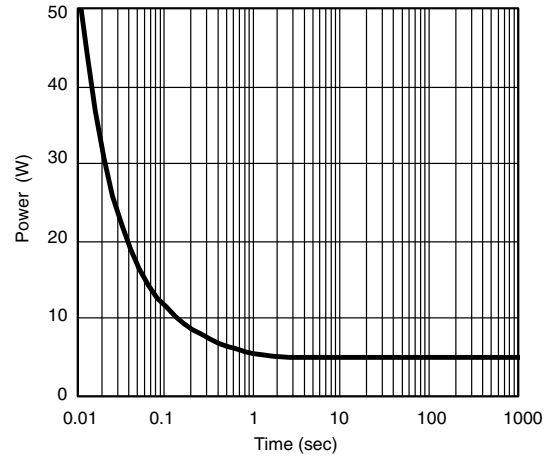


Source-Drain Diode Forward Voltage

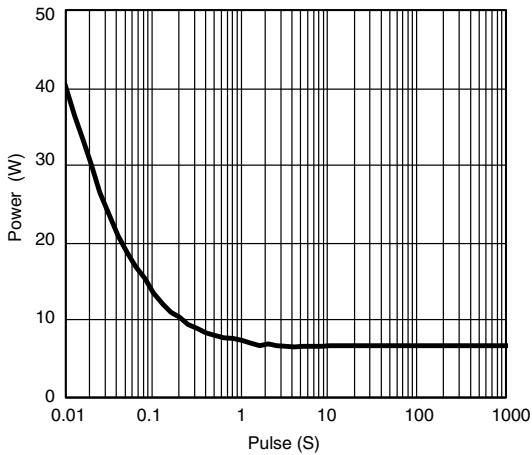
TYPICAL CHARACTERISTICS (25 °C unless noted)



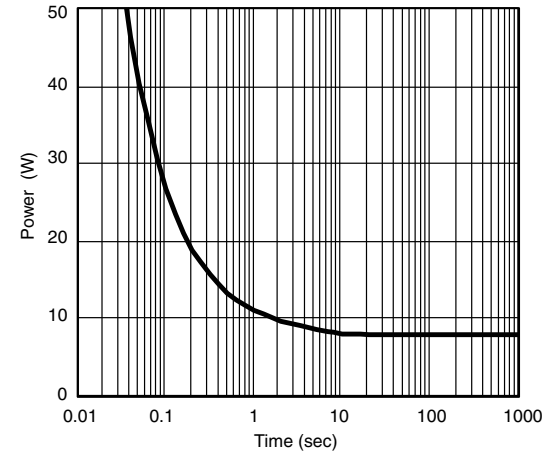
Single Pulse Power, Junction-to-Foot (Q₁)



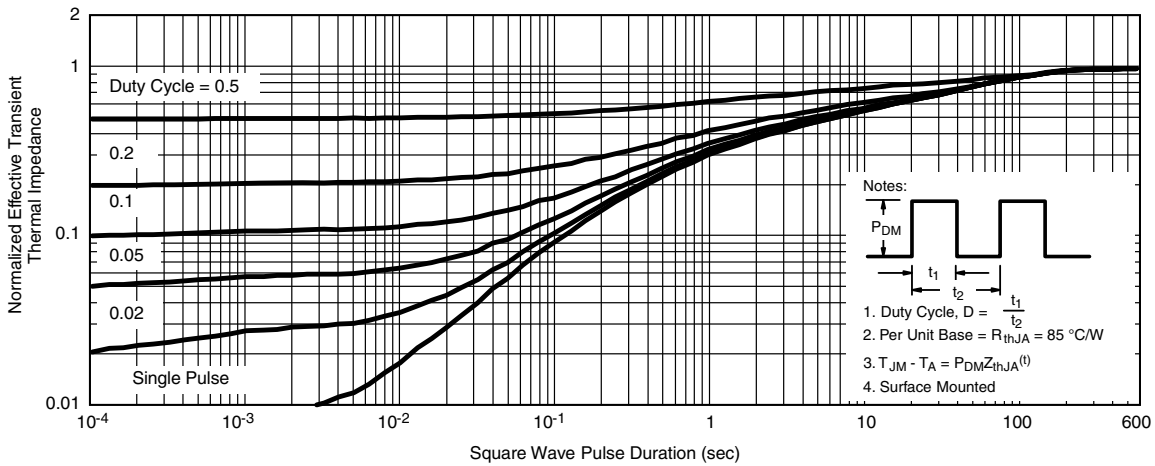
Single Pulse Power, Junction-to-Ambient (Q₁)



Single Pulse Power, Junction-to-Foot (Q₂)

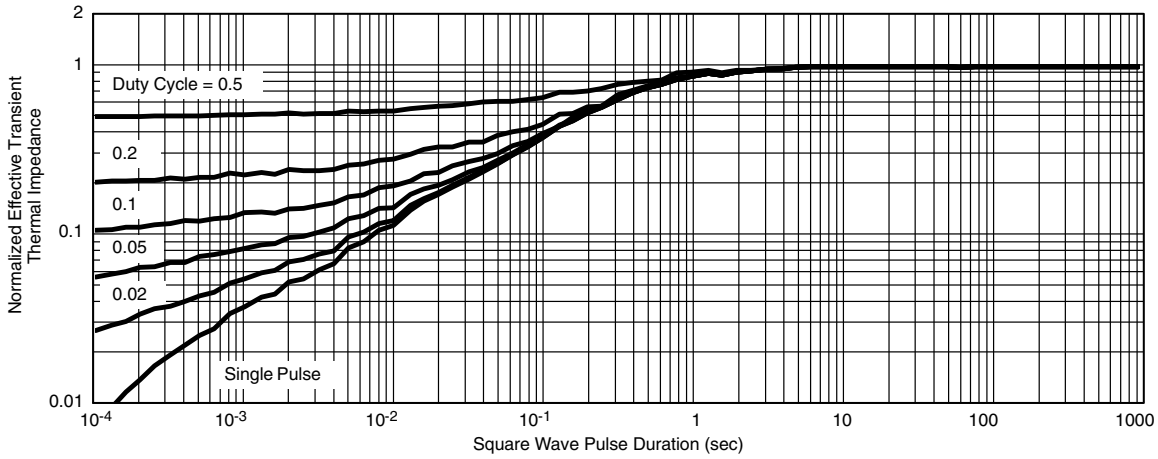


Single Pulse Power, Junction-to-Ambient (Q₂)

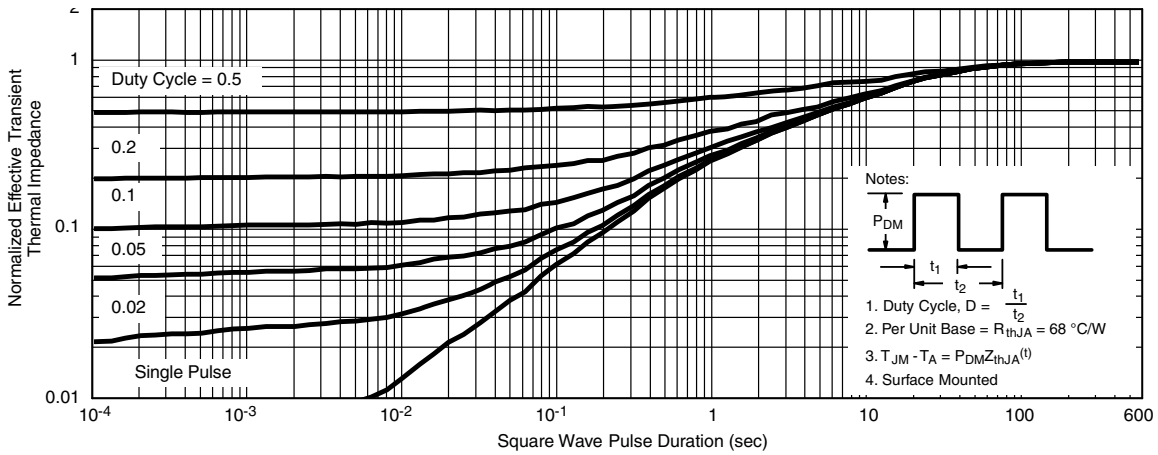


Normalized Thermal Transient Impedance, Junction-to-Ambient (Q₁)

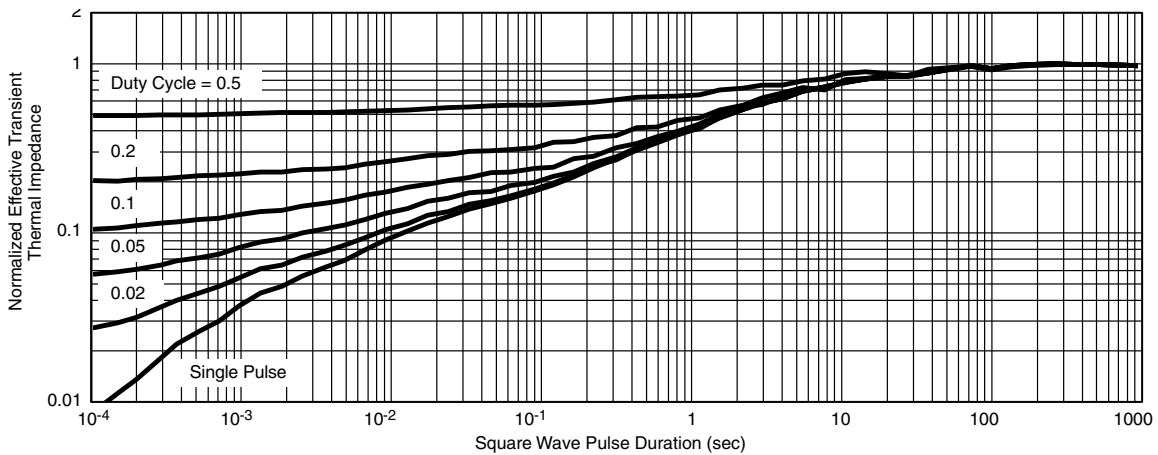
TYPICAL CHARACTERISTICS (25 °C unless noted)



Normalized Thermal Transient Impedance, Junction-to-Foot (Q₁)



Normalized Thermal Transient Impedance, Junction-to-Ambient (Q₂)



Normalized Thermal Transient Impedance, Junction-to-Foot (Q₂)

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71863.



SOIC (NARROW): 16-LEAD
JEDEC Part Number: MS-012

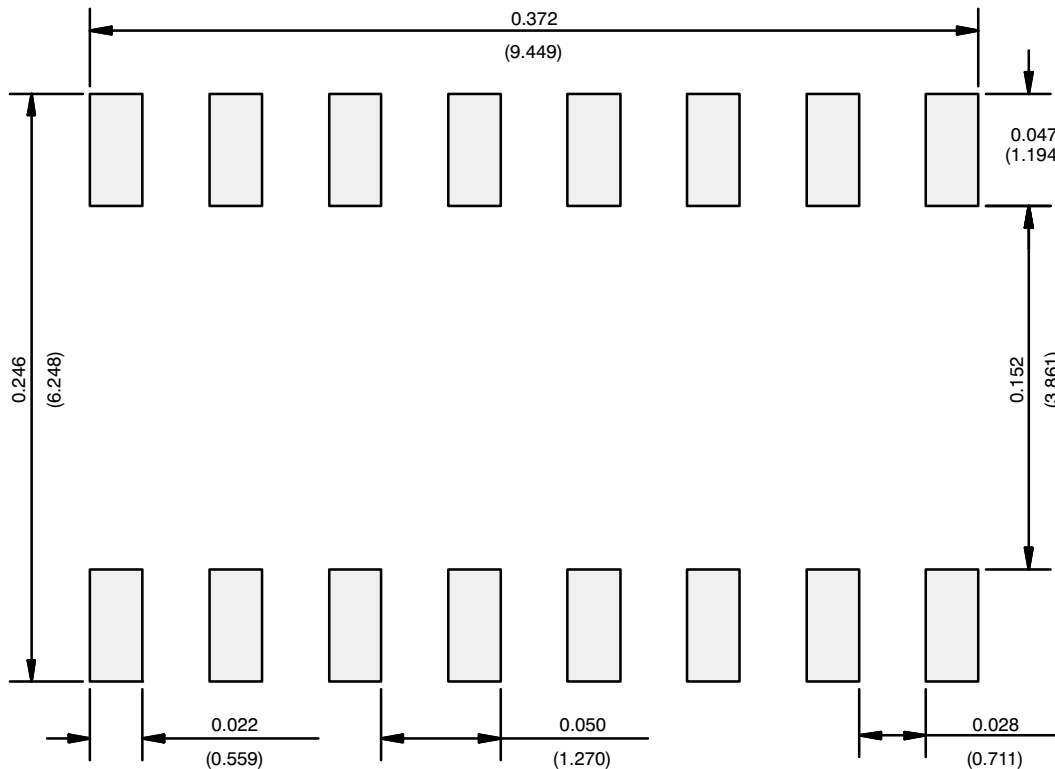


| Dim | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A ₁ | 0.10 | 0.20 | 0.004 | 0.008 |
| B | 0.38 | 0.51 | 0.015 | 0.020 |
| C | 0.18 | 0.23 | 0.007 | 0.009 |
| D | 9.80 | 10.00 | 0.385 | 0.393 |
| E | 3.80 | 4.00 | 0.149 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| L | 0.50 | 0.93 | 0.020 | 0.037 |
| ∅ | 0° | 8° | 0° | 8° |

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300



RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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