# Si5319

**PRELIMINARY DATA SHEET**

# ANY-RATE PRECISION CLOCK MULTIPLIER/JITTER ATTENUATOR

## Description

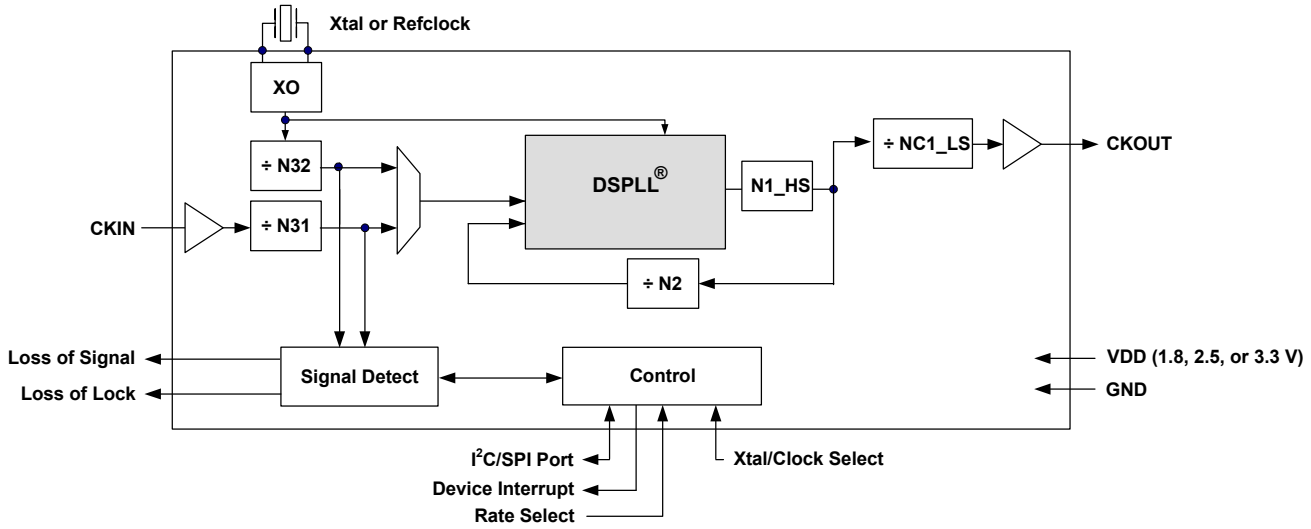
The Si5319 is a jitter-attenuating precision M/N clock multiplier for applications requiring sub 1 ps jitter performance. The Si5319 accepts one clock input ranging from 2 kHz to 710 MHz and generates one clock output ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The Si5319 can also use its crystal oscillator as a clock source for frequency synthesis. The device provides virtually any frequency translation combination across this operating range. The Si5319 input clock frequency and clock multiplication ratio are programmable through an $I^2C$ or SPI interface. The Si5319 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5, or 3.3 V supply, the Si5319 is ideal for providing clock multiplication and jitter attenuation in high performance timing applications.

## Applications

- SONET/SDH OC-48/STM-16 and OC-192/STM-64 line cards
- GbE/10GbE, 1/2/4/8/10GFC line cards
- ITU G.709 and custom FEC line cards
- Optical modules
- Wireless basestations
- Data converter clocking
- xDSL
- Synchronous Ethernet
- Test and measurement
- Discrete PLL replacement
- Broadcast video

## Features

- Generates any frequency from 2 kHz to 945 MHz and select frequencies to 1.4 GHz from an input frequency of 2 kHz to 710 MHz
- Ultra-low jitter clock outputs with jitter generation as low as 0.3 ps rms (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (60 Hz to 8.4 kHz)
- Meets OC-192 GR-253-CORE jitter specifications
- Clock or crystal input with manual clock selection
- Clock output selectable signal format (LVPECL, LVDS, CML, CMOS)
- Support for ITU G.709 and custom FEC ratios (255/238, 255/237, 255/236)
- Supports various frequency translations for Synchronous Ethernet
- LOL, LOS alarm outputs
- $I^2C$ or SPI programmable
- On-chip voltage regulator for 1.8 V ±5%, 2.5 or 3.3 V ±10% operation
- Small size: 6 x 6 mm 36-lead QFN
- Pb-free, ROHS compliant



### Table 1. Performance Specifications[1]

($V_{DD}$ = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 ºC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Temperature Range | $T_A$ | | –40 | 25 | 85 | ºC |
| Supply Voltage | $V_{DD}$ | | 2.97 | 3.3 | 3.63 | V |
| | | | 2.25 | 2.5 | 2.75 | V |
| | | | 1.71 | 1.8 | 1.89 | V |
| Supply Current | $I_{DD}$ | $f_{OUT}$ = 622.08 MHz<br>CKOUT enabled<br>LVPECL format output | — | 217 | 243 | mA |
| | | $f_{OUT}$ = 19.44 MHz<br>CKOUT enabled<br>CMOS format output | — | 194 | 220 | mA |
| | | Tristate/Sleep Mode | — | 165 | TBD | mA |
| Input Clock Frequency (CKIN) | $CK_F$ | Input frequency and clock multiplication ratio determined by programming device PLL dividers. Consult Silicon Laboratories configuration software DSPLL-*sim* to determine PLL divider settings for a given input frequency/clock multiplication ratio combination. | 0.002 | — | 710 | MHz |
| Output Clock Frequency (CKOUT) | $CK_{OF}$ | | 0.002<br>970<br>1213 | — | 945<br>1134<br>1400 | MHz |
| **3-Level Input Pins** | | | | | | |
| Input Mid Current | $I_{IMM}$ | See Note 2. | –2 | — | 2 | µA |
| **Input Clock (CKIN)** | | | | | | |
| Differential Voltage Swing | $CKN_{DPP}$ | | 0.25 | — | 1.9 | VPP |
| Common Mode Voltage | $CKN_{VCM}$ | 1.8 V ±5% | 0.9 | — | 1.4 | V |
| | | 2.5 V ±10% | 1.0 | — | 1.7 | V |
| | | 3.3 V ±10% | 1.1 | — | 1.95 | V |
| Rise/Fall Time | $CKN_{TRF}$ | 20–80% | — | — | 11 | ns |
| Duty Cycle (Minimum Pulse Width) | $CKN_{DC}$ | Whichever is smaller | 40 | — | 60 | % |
| | | | 2 | — | — | ns |
| **Output Clock (CKOUT)** | | | | | | |
| Common Mode | $V_{OCM}$ | LVPECL<br>100 Ω load<br>line-to-line | $V_{DD}$ – 1.42 | — | $V_{DD}$ – 1.25 | V |
| Differential Output Swing | $V_{OD}$ | | 1.1 | — | 1.9 | |
| Single Ended Output Swing | $V_{SE}$ | | 0.5 | — | 0.93 | V |
| Rise/Fall Time | $CKO_{TRF}$ | 20–80% | — | 230 | 350 | ps |
| Output Duty Cycle Differential Uncertainty | $CKO_{DC}$ | 100 Ω load<br>line-to-line<br>measured at 50% point | — | — | ±40 | ps |

**Notes:**

1. For a more comprehensive listing of device specifications, consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual.
2. This is the amount of leakage that the 3-level input can tolerate from an external driver. See the Family Reference Manual. In most designs an external resistor voltage divider is recommended.

**Table 1. Performance Specifications[1] (Continued)**
($V_{DD}$ = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, $T_A$ = –40 to 85 ºC)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **PLL Performance** | | | | | | |
| Jitter Generation | $J_{GEN}$ | $f_{IN}$ = $f_{OUT}$ = 622.08 MHz, LVPECL output format 50 kHz–80 MHz | — | 0.3 | TBD | ps rms |
| | | 12 kHz–20 MHz | — | 0.3 | TBD | ps rms |
| | | 800 Hz–80 MHz | — | 0.4 | TBD | ps rms |
| Jitter Transfer | $J_{PK}$ | | — | 0.05 | 0.1 | dB |
| External Reference Jitter Transfer | $J_{PKEXTN}$ | | — | TBD | TBD | dB |
| Phase Noise | $CKO_{PN}$ | $f_{IN}$ = $f_{OUT}$ = 622.08 MHz 100 Hz offset | — | TBD | TBD | dBc/Hz |
| | | 1 kHz offset | — | TBD | TBD | dBc/Hz |
| | | 10 kHz offset | — | TBD | TBD | dBc/Hz |
| | | 100 kHz offset | — | TBD | TBD | dBc/Hz |
| | | 1 MHz offset | — | TBD | TBD | dBc/Hz |
| Subharmonic Noise | $SP_{SUBH}$ | Phase Noise @ 100 kHz Offset | — | TBD | TBD | dBc |
| Spurious Noise | $SP_{SPUR}$ | Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz) | — | TBD | TBD | dBc |
| **Package** | | | | | | |
| Thermal Resistance Junction to Ambient | Theta JA | Still Air | — | 38 | — | ºC/W |

**Notes:**
1. For a more comprehensive listing of device specifications, consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual.
2. This is the amount of leakage that the 3-level input can tolerate from an external driver. See the Family Reference Manual. In most designs an external resistor voltage divider is recommended.

**Table 2. Absolute Maximum Ratings**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltage | $V_{DD}$ | –0.5 to 3.6 | V |
| LVCMOS Input Voltage | $V_{DIG}$ | –0.3 to ($V_{DD}$ + 0.3) | V |
| Operating Junction Temperature | $T_{JCT}$ | –55 to 150 | ºC |
| Storage Temperature Range | $T_{STG}$ | –55 to 150 | ºC |
| ESD HBM Tolerance (100 pF, 1.5 kΩ), Except CKIN Pins | | 2 | kV |
| ESD HBM Tolerance (100 pF, 1.5 kΩ), CKIN Pins | | 700 | V |
| ESD MM Tolerance, Except CKIN Pins | | 200 | V |
| ESD MM Tolernace, CKIN Pins | | 150 | V |
| Latch-Up Tolerance | | JESD78 Compliant | |

**Note:** Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

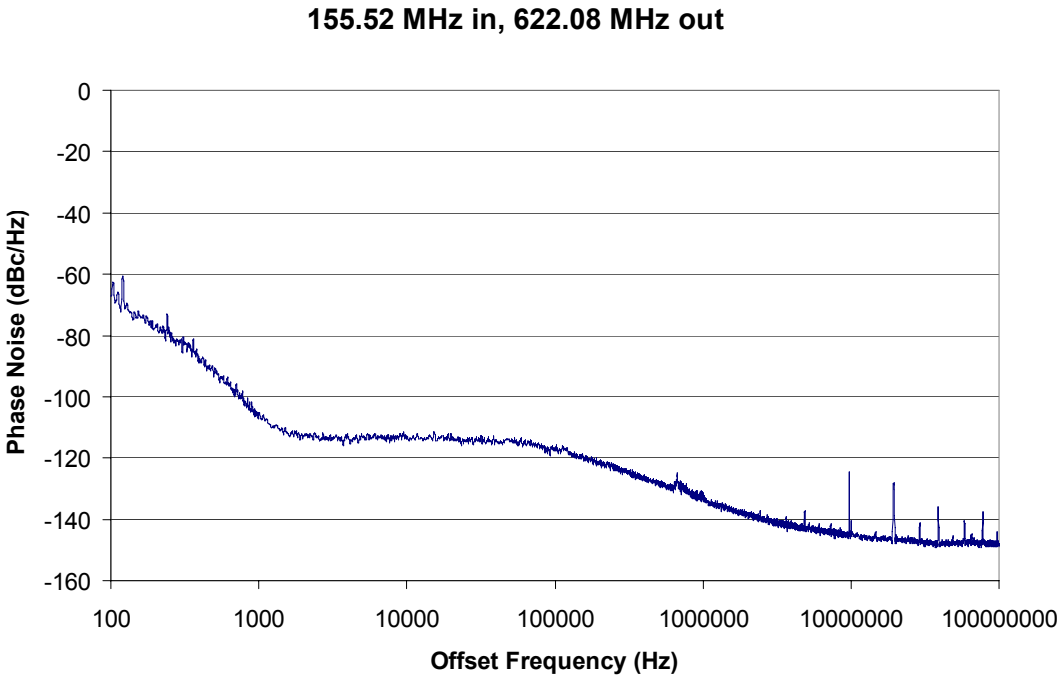



**Figure 1. Typical Phase Noise Plot**

| Jitter Band | Jitter, RMS |
|---|---|
| Brick Wall, 100 Hz to 100 MHz | 1,279 fs |
| SONET_OC48, 12 kHz to 20 MHz | 315 fs |
| SONET_OC192_A, 20 kHz to 80 MHz | 335 fs |
| SONET_OC192_B, 4 MHz to 80 MHz | 194 fs |
| SONET_OC192_C, 50 kHz to 80 MHz | 318 fs |
| Brick Wall, 800 Hz to 80 MHz | 343 fs |

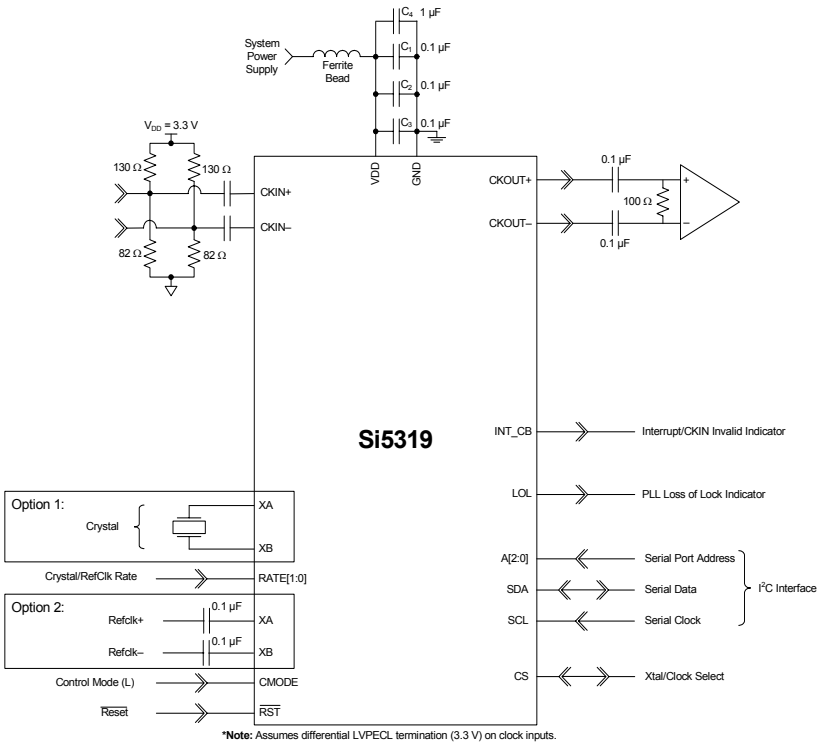



**Figure 2. Si5319 Typical Application Circuit ($I^2C$ Control Mode)**

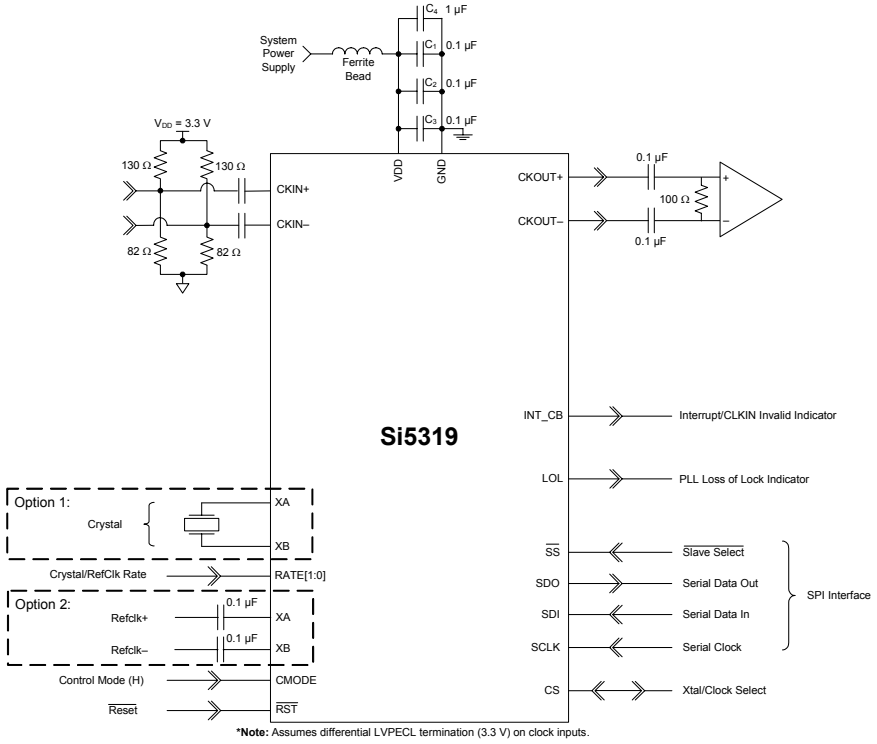



**Figure 3. Si5319 Typical Application Circuit (SPI Control Mode)**

# 1. Functional Description

The Si5319 is a jitter-attenuating precision clock multiplier for applications requiring sub 1 ps jitter performance. The Si5319 accepts one clock input ranging from 2 kHz to 710 MHz and generates one clock output ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The Si5319 can also use its crystal oscillator as a clock source for frequency synthesis. The device provides virtually any frequency translation combination across this operating range. The Si5319 input clock frequency and clock multiplication ratio are programmable through an $I^2C$ or SPI interface. Silicon Laboratories offers a PC-based software utility, DSPLL*sim*, that can be used to determine the optimum PLL divider settings for a given input frequency/clock multiplication ratio combination that minimizes phase noise and power consumption. This utility can be downloaded from http://www.silabs.com/timing.

The Si5319 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5319 PLL loop bandwidth is digitally programmable and supports a range from 60 Hz to 8.4 kHz. The DSPLL*sim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5319 monitors the input clock for loss-of-signal and provides a LOS alarm when it detects missing pulses on the input clock. The device monitors the lock status of the PLL. The lock detect algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock.

The Si5319 provides a digital hold capability that allows the device to continue generation of a stable output clock when the selected input reference is lost. During digital hold, the DSPLL freezes its VCO settings and uses its XO as its frequency reference.

The Si5319 has one differential clock output. The electrical format of the clock output is programmable to support LVPECL, LVDS, CML, or CMOS loads. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

## 1.1. External Reference

A low-cost 114.285 MHz 3rd overtone crystal or an external reference oscillator is used as part of a fixed-frequency oscillator within the DSPLL. This external reference is required for the device to perform jitter attenuation. Silicon Laboratories recommends using a high quality crystal. Specific recommendations may be found in the Family Reference Manual. An external oscillator as well as other crystal frequencies can also be used as a reference for the device.

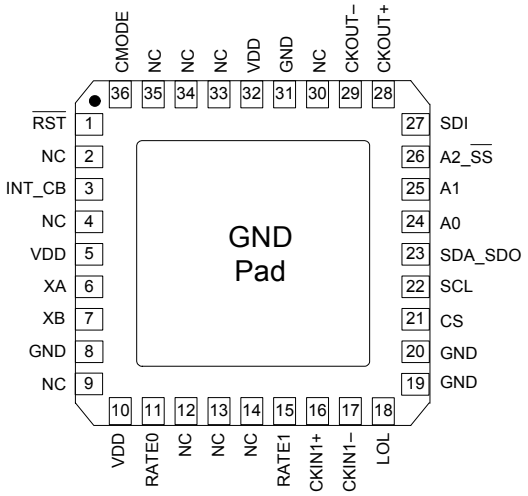
In digital hold, the DSPLL remains locked to this external reference. Any changes in the frequency of this reference when the DSPLL is in digital hold will be tracked by the output of the device. Note that crystals can have temperature sensitivities.

## 1.2. Further Documentation

Consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual (FRM) for detailed information about the Si5319. Additional design support is available from Silicon Laboratories through your distributor.

Silicon Laboratories has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection. The FRM and this utility can be downloaded from http://www.silabs.com/timing; click on Documentation.

## 2. Pin Descriptions: Si5319




Pin numbers are preliminary and subject to change.

| Pin # | Pin Name | I/O | Signal Level | Description |
|---|---|---|---|---|
| 1 | $\overline{\text{RST}}$ | I | LVCMOS | **External Reset.**<br>Active low input that performs external hardware reset of device. Resets all internal logic to a known state and forces the device registers to their default value. Clock outputs are disabled during reset. The part must be programmed after a reset or power-on to get a clock output. See Family Reference Manual for details.<br>This pin has a weak pull-up. |
| 2, 4, 9, 12–14, 30, 33–35 | NC | — | — | **No Connect.**<br>This pin must be left unconnected for normal operation. |
| 3 | INT_CB | O | LVCMOS | **Interrupt/CKIN Invalid Indicator.**<br>This pin functions as a device interrupt output or an alarm output for CKIN. If used as an interrupt output, *INT_PIN* must be set to 1. The pin functions as a maskable interrupt output with active polarity controlled by the *INT_POL* register bit.<br>If used as an alarm output, the pin functions as a LOS alarm indicator for CKIN. Set *CK_BAD_PIN* = 1 and *INT_PIN* = 0.<br>0 = CKIN present.<br>1 = LOS on CKIN.<br>The active polarity is controlled by *CK_BAD_POL*. If no function is selected, the pin tristates. |
| **Note:** Internal register names are indicated by underlined italics (e.g., *INT_PIN*. See Si5319 Register Map). | | | | |

| Pin # | Pin Name | I/O | Signal Level | Description |
|---|---|---|---|---|
| 5, 10, 32 | $V_{DD}$ | $V_{DD}$ | Supply | **Supply.**<br>The device operates from a 1.8, 2.5, or 3.3 V supply. Bypass capacitors should be associated with the following $V_{DD}$ pins:<br>5 0.1 µF<br>10 0.1 µF<br>32 0.1 µF<br>A 1.0 µF should also be placed as close to the device as is practical. |
| 7<br>6 | XB<br>XA | I | Analog | **External Crystal or Reference Clock.**<br>External crystal should be connected to these pins to use internal oscillator based reference. Refer to the Family Reference Manual for interfacing to an external reference. The external reference must be from a high-quality clock source (TCXO, OCXO). Frequency of crystal or external clock is set by the RATE pins. |
| 8, 31 | GND | GND | Supply | **Ground.**<br>**Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device.** |
| 11<br>15 | RATE0<br>RATE1 | I | 3-Level | **External Crystal or Reference Clock Rate.**<br>Three level inputs that select the type and rate of external crystal or reference clock to be applied to the XA/XB port. Refer to the Family Reference Manual for settings. These pins have both a weak pull-up and a weak pull-down; they default to M. The "HH" setting is not supported.<br>Some designs may require an external resistor voltage divider when driven by an active device that will tri-state. |
| 16<br>17 | CKIN+<br>CKIN– | I | Multi | **Clock Input.**<br>Differential input clock. This input can also be driven with a single-ended signal. Input frequency range is 2 kHz to 710 MHz. |
| 18 | LOL | O | LVCMOS | **PLL Loss of Lock Indicator.**<br>This pin functions as the active high PLL loss of lock indicator if the *LOL_PIN* register bit is set to 1.<br>0 = PLL locked.<br>1 = PLL unlocked.<br>If *LOL_PIN* = 0, this pin will tristate. Active polarity is controlled by the *LOL_POL* bit. The PLL lock status will always be reflected in the *LOL_INT* read only register bit. |
| 21 | CS | I | LVCMOS | **Xtal/Input Clock Select.**<br>This pin selects the active DSPLL input clock, which can be a clock input or a crystal input. See the *FREE_EN* register for free run settings.<br>0 = Select clock input (CKIN).<br>1 = Select crystal input.<br>This pin should not be left open. |
| 22 | SCL | I | LVCMOS | **Serial Clock/Serial Clock.**<br>This pin functions as the serial clock input for both SPI and $I^2C$ modes. This pin has a weak pull-down. |
| **Note:** Internal register names are indicated by underlined italics (e.g., *INT_PIN*. See Si5319 Register Map). | | | | |

| Pin # | Pin Name | I/O | Signal Level | Description |
|---|---|---|---|---|
| 23 | SDA_SDO | I/O | LVCMOS | **Serial Data.**<br>In $I^2C$ control mode (CMODE = 0), this pin functions as the bidirectional serial data port.<br>In SPI control mode (CMODE = 1), this pin functions as the serial data output. |
| 25<br>24 | A1<br>A0 | I | LVCMOS | **Serial Port Address.**<br>In $I^2C$ control mode (CMODE = 0), these pins function as hardware controlled address bits. The $I^2C$ address is 1101 [A2] [A1] [A0].<br>In SPI control mode (CMODE = 1), these pins are ignored.<br>These pins have a weak pull-down. |
| 26 | A2_$\overline{SS}$ | I | LVCMOS | **Serial Port Address/Slave Select.**<br>In $I^2C$ control mode (CMODE = 0), this pin functions as a hardware controlled address bit [A2].<br>In SPI control mode (CMODE = 1), this pin functions as the slave select input.<br>This pin has a weak pull-down. |
| 27 | SDI | I | LVCMOS | **Serial Data In.**<br>In $I^2C$ control mode (CMODE = 0), this pin is ignored.<br>In SPI control mode (CMODE = 1), this pin functions as the serial data input.<br>This pin has a weak pull-down. |
| 29<br>28 | CKOUT–<br>CKOUT+ | O | Multi | **Output Clock.**<br>Differential output clock with a frequency range of 10 MHz to 1.4175 GHz. Output signal format is selected by *SFOUT1_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs. |
| 36 | CMODE | I | LVCMOS | **Control Mode.**<br>Selects $I^2C$ or SPI control mode for the Si5319.<br>0 = $I^2C$ Control Mode<br>1 = SPI Control Mode |
| GND PAD | GND | GND | Supply | **Ground Pad.**<br>**The ground pad must provide a low thermal and electrical impedance to a ground plane.** |

**Note:** Internal register names are indicated by underlined italics (e.g., *INT_PIN*. See Si5319 Register Map).

## 3. Ordering Guide

| Ordering Part Number | Output Clock Frequency Range | Package | ROHS6, Pb-Free | Temperature Range |
|---|---|---|---|---|
| Si5319A-C-GM | 2 kHz–945 MHz<br>970–1134 MHz<br>1.213–1.417 GHz | 36-Lead 6 x 6 mm QFN | Yes | –40 to 85 °C |
| Si5319B-C-GM | 2 kHz–808 MHz | 36-Lead 6 x 6 mm QFN | Yes | –40 to 85 °C |
| Si5319C-C-GM | 2 kHz–346 MHz | 36-Lead 6 x 6 mm QFN | Yes | –40 to 85 °C |

## 4. Package Outline: 36-Pin QFN

Figure 4 illustrates the package details for the Si5319. Table 3 lists the values for the dimensions shown in the illustration.

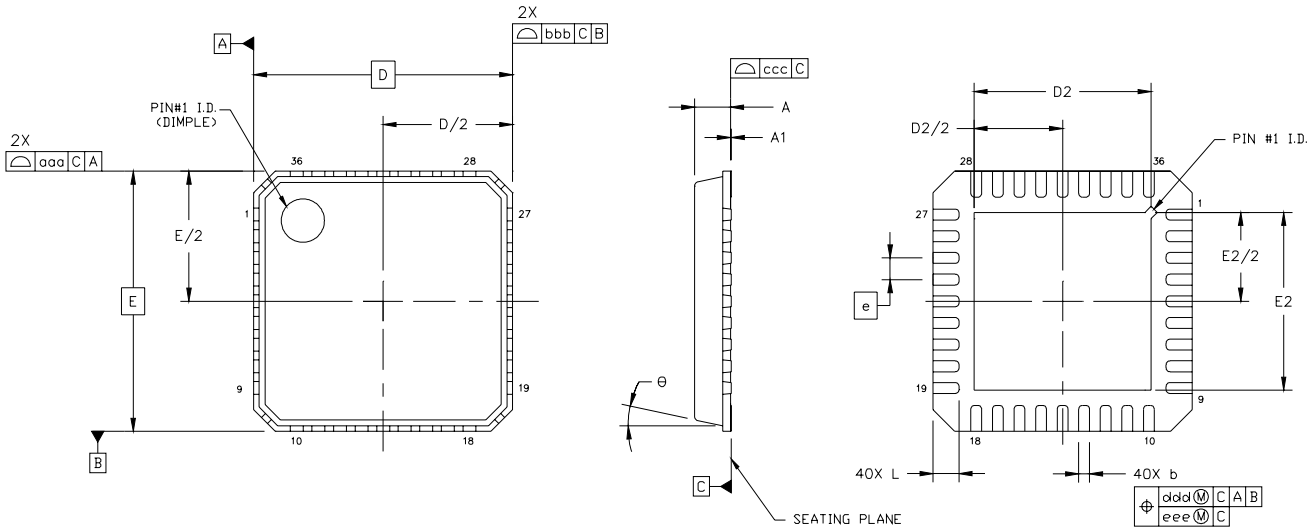



**Figure 4. 36-Pin Quad Flat No-lead (QFN)**

**Table 3. Package Dimensions**

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| D | | 6.00 BSC | |
| D2 | 3.95 | 4.10 | 4.25 |
| e | | 0.50 BSC | |
| E | | 6.00 BSC | |
| E2 | 3.95 | 4.10 | 4.25 |

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| L | 0.50 | 0.60 | 0.70 |
| θ | — | — | 12º |
| aaa | — | — | 0.10 |
| bbb | — | — | 0.10 |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.10 |
| eee | — | — | 0.05 |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VJJD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

## 5. Recommended PCB Layout

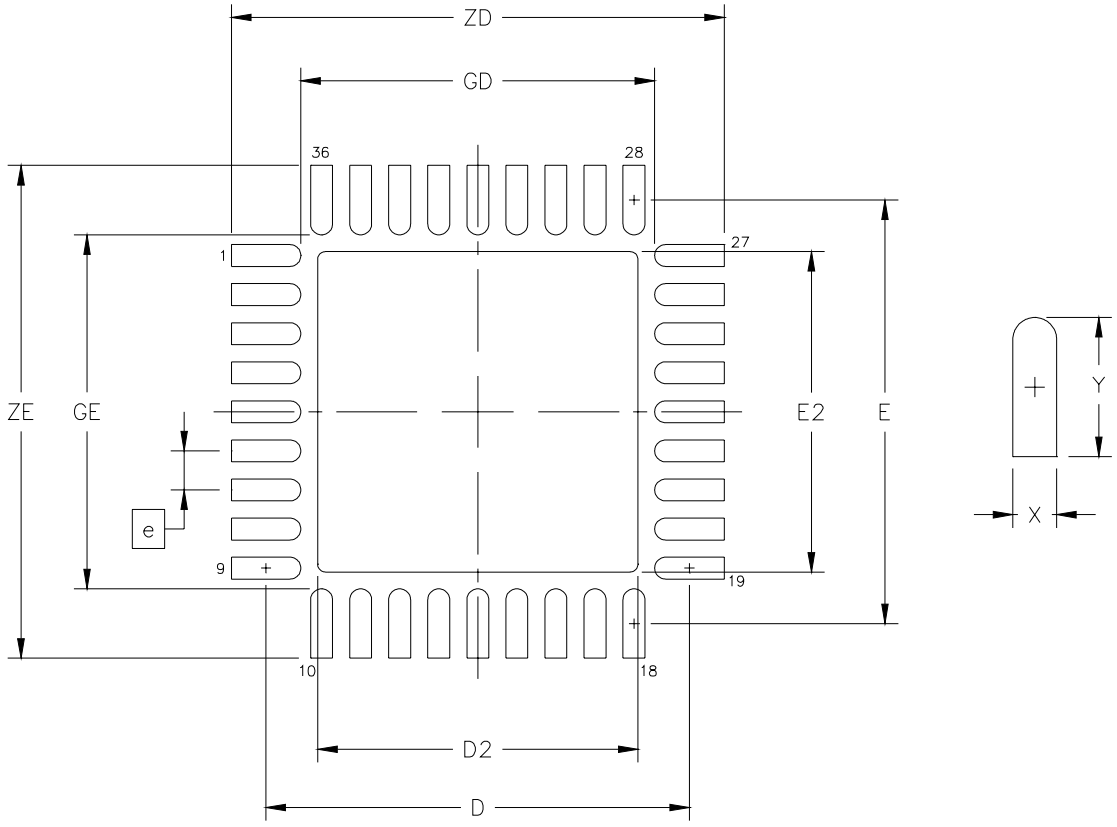



**Figure 5. PCB Land Pattern Diagram**

**Table 4. PCB Land Pattern Dimensions**

| Dimension | MIN | MAX |
|---|---|---|
| e | 0.50 BSC. | |
| E | 5.42 REF. | |
| D | 5.42 REF. | |
| E2 | 4.00 | 4.20 |
| D2 | 4.00 | 4.20 |
| GE | 4.53 | — |
| GD | 4.53 | — |
| X | — | 0.28 |
| Y | 0.89 REF. | |
| ZE | — | 6.31 |
| ZD | — | 6.31 |

**Notes (General):**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Notes (Solder Mask Design):**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Notes (Stencil Design):**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

**Notes (Card Assembly):**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

# DOCUMENT CHANGE LIST

## Revision 0.1 to Revision 0.2

- Changed 1.8 V operating range to ±5%.
- Updated Table 1 on page 2.
- Updated Table 2 on page 3.
- Added table under Figure 1 on page 4.
- Updated "1. Functional Description" on page 6.
- Clarified "2. Pin Descriptions: Si5319" on page 7.

## Revision 0.2 to Revision 0.3

- Updated "2. Pin Descriptions: Si5319" on page 7.
  - Corrected Pins 11 and 15 description in table.

## NOTES:

## CONTACT INFORMATION

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