Si5338

I²C-Programmable Any-Frequency, Any-Output Quad Clock Generator

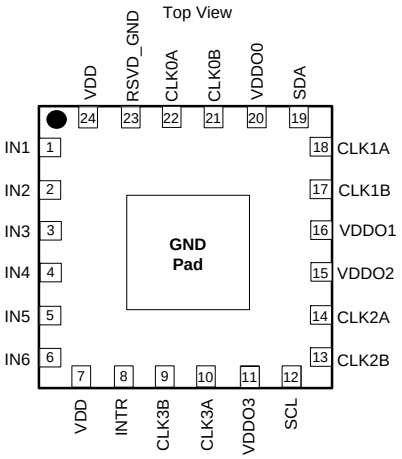
Features

- Low power MultiSynth™ technology enables independent, any-frequency synthesis on four differential output drivers
- Highly-configurable output drivers with up to four differential outputs, eight single-ended clock outputs, or a combination of both
- Low phase jitter of 0.7 ps RMS typ
- High precision synthesis allows true zero ppm frequency accuracy on all outputs
- Flexible input reference:
  - External crystal: 8 to 30 MHz
  - CMOS input: 5 to 200 MHz
  - SSTL/HSTL input: 5 to 350 MHz
  - Differential input: 5 to 710 MHz
- Independently configurable outputs support any frequency or format:
  - LVPECL/LVDS: 0.16 to 710 MHz
  - HCSL: 0.16 to 250 MHz
  - CMOS: 0.16 to 200 MHz
  - SSTL/HSTL: 0.16 to 350 MHz
- Independent output voltage per driver: 1.5, 1.8, 2.5, or 3.3 V
- Single supply core with excellent PSRR: 1.8, 2.5, 3.3 V
- Independent frequency increment/decrement feature enables glitchless frequency adjustments in 1 ppm steps
- Independent phase adjustment on each of the output drivers with an accuracy of ≤20 ps steps
- Highly configurable spread spectrum (SSC) on any output:
  - Any frequency from 5 to 350 MHz
  - Any spread from 0.5 to 5.0%
  - Any modulation rate from 33 to 63 kHz
- External feedback mode allows zero-delay mode
- Loss of lock and loss of signal alarms
- I²C/SMBus compatible interface
- Easy to use programming software
- Small size: 4 x 4 mm, 24-QFN
- Low power: 45 mA core supply typ
- Wide temperature range: –40 to +85 °C

Ordering Information:

See page 168.

Pin Assignments



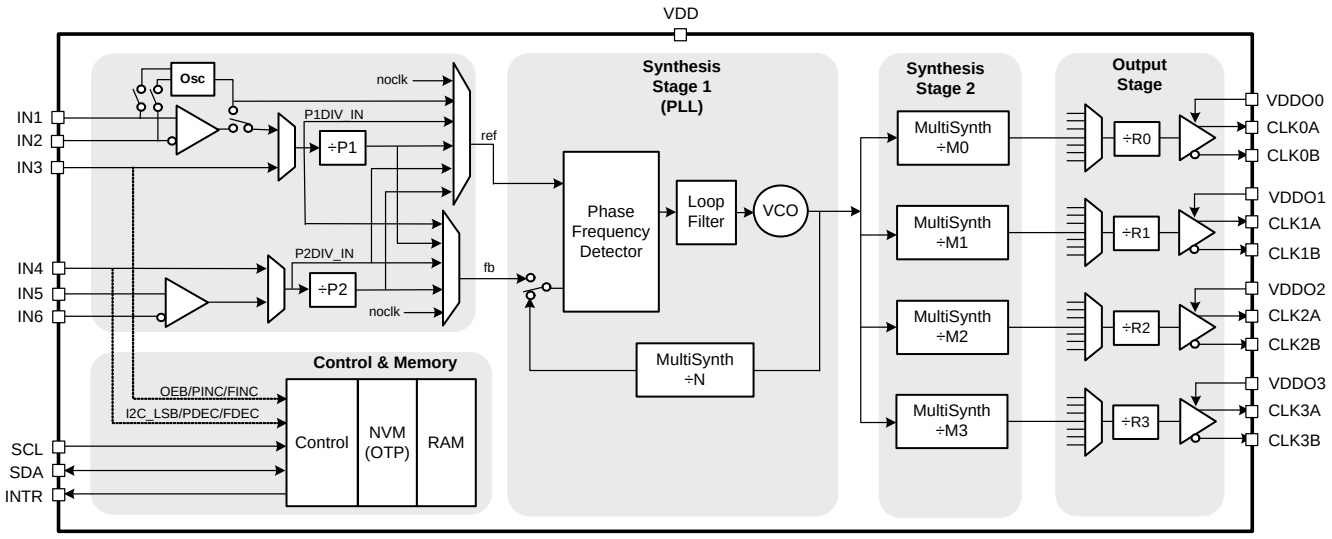
Applications

- Ethernet switch/router
- PCI Express 2.0/3.0
- Broadcast video/audio timing
- Processor and FPGA clocking
- Any-frequency clock conversion
- MSAN/DSLAM/PON
- Fibre Channel, SAN
- Telecom line cards

Description

The Si5338 is a high-performance, low-jitter clock generator capable of synthesizing any frequency on each of the device's four output drivers. This timing IC is capable of replacing up to four different frequency crystal oscillators or operating as a frequency translator. Using its patented MultiSynth™ technology, the Si5338 allows generation of four independent clocks with 0 ppm precision. Each output clock is independently configurable to support various signal formats and supply voltages. The Si5338 provides low-jitter frequency synthesis in a space-saving 4 x 4 mm QFN package. The device is programmable via an I²C/SMBus-compatible serial interface and supports operation from a 1.8, 2.5, or 3.3 V core supply. I²C device programming is made easy with the ClockBuilder™ Desktop software available at www.silabs.com/ClockBuilder.

Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Core Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
			1.71	1.8	1.98	V
Output Buffer Supply Voltage	V_{DDOn}		1.4	—	3.63	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
Storage Temperature Range	T_{STG}		–55 to 150	°C
ESD Tolerance		HBM (100 pF, 1.5 kΩ)	2.5	kV
ESD Tolerance		CDM	550	V
ESD Tolerance		MM	175	V
Latch-up Tolerance			JESD78 Compliant	
Junction Temperature	T_J		150	°C

Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. DC Characteristics

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current	I_{DD}	100 MHz on all outputs, 25 MHz refclk	—	45	60	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL, 710 MHz	—	—	30	mA
		LVDS, 710 MHz	—	—	8	mA
		HCSL, 250 MHz 2 pF load	—	—	20	mA
		SSTL, 350 MHz	—	—	19	mA
		CMOS, 50 MHz 15 pF load	—	—	28	mA
		CMOS, 200 MHz 2 pF load, 3.3 V VDD0	—	—	20	mA
		CMOS, 200 MHz 2 pF load, 2.5 V	—	13	17	mA
		CMOS, 200 MHz 2 pF load, 1.8 V	—	11	15	mA
		HSTL, 350 MHz	—	—	19	mA

Table 4. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	37	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	25	°C/W

Table 5. Performance Characteristics
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Acquisition Time	t_{ACQ}		—	—	25	ms
PLL Lock Range	f_{LOCK}		5000	—	—	ppm
PLL Loop Bandwidth	f_{BW}		—	1.6	—	MHz
MultiSynth Frequency Synthesis Resolution	f_{RES}	Output frequency ≤ Fvco/8	0	0	1	ppb
CLKIN Loss of Signal Detect Time	t_{LOS}		—	2.6	5	µs
CLKIN Loss of Signal Release Time	t_{LOSRLS}		0.01	0.2	1	µs
PLL Loss of Lock Detect Time	t_{LOL}		—	5	10	ms
POR to Output Clock Valid (Pre-programmed Devices)	t_{RDY}		—	—	2	ms
Input-to-Output Propagation Delay	t_{PROP}	Buffer Mode (PLL Bypass)	—	2.5	—	ns
Output-Output Skew	t_{DSKEW}	Rn divider = 1[1]	—	—	100	ps
POR to I^2C Ready			—	—	15	ms
Programmable Initial Phase Offset	P_{OFFSET}		–45	—	+45	ns
Phase Increment/Decrement Accuracy	P_{STEP}		—	—	20	ps
Phase Increment/Decrement Range	P_{RANGE}		–45	—	+45	ns
Frequency range for phase increment/decrement	f_{PRANGE}		—	—	350[2]	MHz
Phase Increment/Decrement Update Time	P_{UPDATE}	Pin control[2,3] MultiSynth output >18 MHz	667	—	—	ns

Notes:
1. Outputs at integer-related frequencies and using the same driver format. See "3.9.3. Initial Phase Offset" on page 24.
2. The maximum step size is only limited by the register lengths; however, the MultiSynth output frequency must be kept between 5 MHz and Fvco/8.
3. Update rate via I^2C is also limited by the time it takes to perform a write operation.
4. Default value is 0.5% down spread.
5. Default value is ~31.5 kHz.

Table 5. Performance Characteristics (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase Increment/Decrement Update Time	P_{UPDATE}	Pin control[2,3] MultiSynth output <18 MHz Number of periods of MultiSynth output frequency	—	12	—	Periods
Frequency Increment/ Decrement Step Size	f_{STEP}	R divider not used	1	—	See Note [2]	ppm
Frequency Increment/ Decrement Range	f_{RANGE}	R divider not used	—	—	350[2]	MHz
Frequency Increment/ Decrement Update Time	f_{UPDATE}	Pin control[2,3] MultiSynth output >18 MHz	667	—	—	ns
Frequency Increment/ Decrement Update Time	f_{UPDATE}	Pin control[2,3] MultiSynth output <18 MHz Number of periods of MultiSynth output frequency	—	12	—	Periods
Spread Spectrum PP Frequency Deviation	SS_{DEV}	MultiSynth Output ≤ ~Fvco/8	0.1	—	5.0[4]	%
Spread Spectrum Modulation Rate	SS_{DEV}	MultiSynth Output ≤ ~Fvco/8	30	—	63[5]	kHz

Notes:
1. Outputs at integer-related frequencies and using the same driver format. See "3.9.3. Initial Phase Offset" on page 24.
2. The maximum step size is only limited by the register lengths; however, the MultiSynth output frequency must be kept between 5 MHz and Fvco/8.
3. Update rate via I^2C is also limited by the time it takes to perform a write operation.
4. Default value is 0.5% down spread.
5. Default value is ~31.5 kHz.

Table 6. Input and Output Clock Characteristics
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Clock (AC Coupled Differential Input Clocks on Pins IN1/2, IN5/6)						
Frequency	f_{IN}		5	—	710	MHz
Differential Voltage Swing	V_{PP}	710 MHz input	0.4	—	2.4	V_{PP}
Rise/Fall Time	t_R/t_F	20%–80%	—	—	1.0	ns
Duty Cycle[1]	DC	< 1 ns tr/tf	40	—	60	%

Notes:
1. For best jitter performance, keep the input slew rate on pins 1,2,5,6 faster than 0.3 V/ns
2. Not in PLL bypass mode.
3. For best jitter performance, keep the input single ended slew rate on pins 3 or 4 faster than 1 V/ns
4. Only two unique frequencies above 350 MHz can be simultaneously output, Fvco/4 and Fvco/6.
5. Includes effect of internal series 22 Ω resistor.

Table 6. Input and Output Clock Characteristics (Continued)

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Impedance	R_{IN}		10	—	—	kΩ
Input Capacitance	C_{IN}		—	3.5	—	pF
Input Clock (DC-Coupled Single-Ended Input Clock on Pins IN3/4)						
Frequency	f_{IN}	CMOS	5	—	200	MHz
Input Voltage	V_I		–0.1	—	3.63	V
Input Voltage Swing		200 MHz	0.8	—	VDD+10%	Vpp
Rise/Fall Time	t_R/t_F	20%–80%	—	—	2	ns
Duty Cycle[2,3]	DC	< 4 ns tr/tf	40	—	60	%
Input Capacitance	C_{IN}		—	2.0	—	pF
Output Clocks (Differential)						
Frequency[4]	f_{OUT}	LVPECL, LVDS	0.16	—	350	MHz
			367	—	473.33	MHz
			550	—	710	MHz
		HCSL	0.16	—	250	MHz
LVPECL Output Voltage	V_{OC}	common mode	—	V_{DDO}–1.45 V	—	V
	V_{SEPP}	peak-to-peak single-ended swing	0.55	0.8	0.96	V_{PP}
LVDS Output Voltage (2.5/3.3 V)	V_{OC}	common mode	1.125	1.2	1.275	V
	V_{SEPP}	peak-to-peak single-ended swing	0.25	0.35	0.45	V_{PP}
LVDS Output Voltage (1.8 V)	V_{OC}	common mode	0.8	0.875	0.95	V
	V_{SEPP}	peak-to-peak single-ended swing	0.25	0.35	0.45	V_{PP}
HCSL Output Voltage	V_{OC}	common mode	0.35	0.375	0.400	V
	V_{SEPP}	peak-to-peak single-ended swing	0.575	0.725	0.85	V_{PP}
Rise/Fall Time	t_R/t_F	20%–80%	—	—	450	ps
Duty Cycle[2]	DC		45	—	55	%

Notes:

1. For best jitter performance, keep the input slew rate on pins 1,2,5,6 faster than 0.3 V/ns
2. Not in PLL bypass mode.
3. For best jitter performance, keep the input single ended slew rate on pins 3 or 4 faster than 1 V/ns
4. Only two unique frequencies above 350 MHz can be simultaneously output, Fvco/4 and Fvco/6.
5. Includes effect of internal series 22 Ω resistor.

Table 6. Input and Output Clock Characteristics (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output Clocks (Single-Ended)						
Frequency	f_{OUT}	CMOS	0.16	—	200	MHz
		SSTL, HSTL	0.16	—	350	MHz
CMOS 20%–80% Rise/Fall Time	t_R/t_F	2 pF load	—	0.45	0.85	ns
CMOS 20%–80% Rise/Fall Time	t_R/t_F	15 pF load	—	—	1.7	ns
CMOS Output Resistance			—	50	—	Ω
SSTL Output Resistance			—	50	—	Ω
HSTL Output Resistance			—	50	—	Ω
CMOS Output Voltage[5]	V_{OH}	4 mA load	VDDO – 0.3	—		V
	V_{OL}	4 mA load		—	0.3	V
SSTL Output Voltage	V_{OH}	SSTL-3 VDDOx = 2.97 to 3.63 V	0.45xVDDO+0.41	—	—	V
	V_{OL}		—	—	0.45xVDDO–0.41	V
	V_{OH}	SSTL-2 VDDOx = 2.25 to 2.75 V	0.5xVDDO+0.41	—	—	V
	V_{OL}		—	—	0.5xVDDO–0.41	V
	V_{OH}	SSTL-18 VDDOx = 1.71 to 1.98 V	0.5xVDDO+0.34	—		V
	V_{OL}		—	—	0.5xVDDO–0.34	V
HSTL Output Voltage	V_{OH}	VDDO = 1.4 to 1.6 V	0.5xVDDO+0.3	—	—	V
	V_{OL}		—	—	0.5xVDDO –0.3	V
Duty Cycle[2]	DC		45	—	55	%

Notes:
1. For best jitter performance, keep the input slew rate on pins 1,2,5,6 faster than 0.3 V/ns
2. Not in PLL bypass mode.
3. For best jitter performance, keep the input single ended slew rate on pins 3 or 4 faster than 1 V/ns
4. Only two unique frequencies above 350 MHz can be simultaneously output, Fvco/4 and Fvco/6.
5. Includes effect of internal series 22 Ω resistor.

Table 7. Control Pins
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Control Pins (IN3, IN4)						
Input Voltage Low	V_{IL}		–0.1	—	0.3 x VDD	V
Input Voltage High	V_{IH}		0.7 x VDD	—	3.63	V
Input Capacitance	C_{IN}		—	—	4	pF
Input Resistance	R_{IN}		—	20	—	kΩ
Output Control Pins (INTR)						
Output Voltage Low	V_{OL}	I_{SINK} = 3 mA	0	—	0.4	V
Rise/Fall Time 20–80%	t_R/t_F	C_L < 10 pf, pull up ≤ 1 kΩ	—	—	10	ns

Table 8. Crystal Specifications for 8 to 11 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	8	—	11	MHz
Load Capacitance (on-chip differential)	c_L	11	12	13	pF
Crystal Output Capacitance	c_O	—	—	6	pF
Equivalent Series Resistance	r_{ESR}	—	—	300	Ω
Crystal Max Drive Level	d_L	100	—	—	µW

Table 9. Crystal Specifications for 11 to 19 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	11	—	19	MHz
Load Capacitance (on-chip differential)	c_L	11	12	13	pF
Crystal Output Capacitance	c_O	—	—	5	pF
Equivalent Series Resistance	r_{ESR}	—	—	200	Ω
Crystal Max Drive Level	d_L	100	—	—	µW

Table 10. Crystal Specifications for 19 to 26 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	19		26	MHz
Load Capacitance (on-chip differential)	c_L	11	12	13	pF
Crystal Output Capacitance	c_O			5	pF
Equivalent Series Resistance	r_{ESR}			100	Ω
Crystal Max Drive Level	d_L	100			µW

Table 11. Crystal Specifications for 26 to 30 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	26		30	MHz
Load Capacitance (on-chip differential)	c_L	11	12	13	pF
Crystal Output Capacitance	c_O			5	pF
Equivalent Series Resistance	r_{ESR}			75	Ω
Crystal Max Drive Level	d_L	100			µW

Table 12. Jitter Specifications[1,2]

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
GbE Random Jitter (12 kHz–20 MHz)[3]	J_{GBE}	CLKIN = 25 MHz All CLKn at 125 MHz[4]	—	0.7	1	ps RMS
GbE Random Jitter (1.875–20 MHz)	R_{JGBE}	CLKIN = 25 MHz All CLKn at 125 MHz[4]	—	0.38	0.79	ps RMS
OC-12 Random Jitter (12 kHz–5 MHz)	J_{OC12}	CLKIN = 19.44 MHz All CLKn at 155.52 MHz[4]	—	0.7	1	ps RMS
PCI Express 3.0 Random Jitter (1.5 MHz—50 MHz)[3]	$J_{PCIERJ1}$	CLKIN = 25 MHz All CLKn at 100 MHz Spread Spectrum not enabled[4]	—	0.6	1	ps RMS
PCI Express 3.0 Random Jitter (12 kHz—20 MHz)[3]	$J_{PCIERJ2}$	CLKIN = 25 MHz All CLKn at 100 MHz Spread Spectrum not enabled[4]	—	0.7	1	ps RMS
PCI Express 3.0 Period Jitter		CLKIN = 25 MHz All CLKn at 100 MHz Spread Spectrum not enabled[4]	—	8	15	ps pk-pk
PCI Express 3.0 Cycle-Cycle Jitter		CLKIN = 25 MHz All CLKn at 100 MHz Spread Spectrum not enabled[4]	—	13	30	ps pk-pk
Period Jitter	J_{PER}	N = 10,000 cycles[5]	—	10	30	ps pk-pk
Cycle-Cycle Jitter	J_{CC}	N = 10,000 cycles Output MultiSynth operated in integer or fractional mode[5]	—	9	29	ps pk[6]
Random Jitter (12 kHz–20 MHz)	R_J	Output and feedback MultiSynth in integer or fractional mode[5]	—	0.7	1.5	ps RMS

Notes:

1. All jitter measurements apply for LVDS/HCSL/LVPECL output format with a low noise differential input clock and are made with an Agilent 90804 oscilloscope. All RJ measurements use RJ/DJ separation.
2. For best jitter performance, keep the single ended clock input slew rates at Pins 3 and 4 more than 1.0 V/ns and the differential clock input slew rates more than 0.3 V/ns.
3. D_J for PCI and GBE is < 5 ps pp
4. Output MultiSynth in Integer mode.
5. Input frequency to the Phase Detector between 25 and 40 MHz and any output frequency ≥ 5 MHz.
6. Measured in accordance with JEDEC standard 65.
7. Rj is multiplied by 14; estimate the pp jitter from Rj over 2^{12} rising edges.

Table 12. Jitter Specifications[1,2] (Continued)

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Deterministic Jitter	D_J	Output MultiSynth operated in fractional mode[5]	—	3	15	ps pk-pk
		Output MultiSynth operated in integer mode[5]	—	2	10	ps pk-pk
Total Jitter (12 kHz–20 MHz)	$T_J = D_J+14xR_J$ (See Note [7])	Output MultiSynth operated in fractional mode[5]	—	13	36	ps pk-pk
		Output MultiSynth operated in integer mode[5]	—	12	20	ps pk-pk

Notes:

1. All jitter measurements apply for LVDS/HCSL/LVPECL output format with a low noise differential input clock and are made with an Agilent 90804 oscilloscope. All RJ measurements use RJ/DJ separation.
2. For best jitter performance, keep the single ended clock input slew rates at Pins 3 and 4 more than 1.0 V/ns and the differential clock input slew rates more than 0.3 V/ns.
3. D_J for PCI and GBE is < 5 ps pp
4. Output MultiSynth in Integer mode.
5. Input frequency to the Phase Detector between 25 and 40 MHz and any output frequency ≥ 5 MHz.
6. Measured in accordance with JEDEC standard 65.
7. Rj is multiplied by 14; estimate the pp jitter from Rj over 2^{12} rising edges.

Table 13. Typical Phase Noise Performance

Offset Frequency	25MHz XTAL to 156.25 MHz	27 MHz Ref In to 148.3517 MHz	19.44 MHz Ref In to 155.52 MHz	Units
100 Hz	–90	–87	–110	dBc/Hz
1 kHz	–120	–117	–116	
10 kHz	–126	–123	–123	
100 kHz	–132	–130	–128	
1 MHz	–132	–132	–128	
10 MHz	–145	–145	–145	

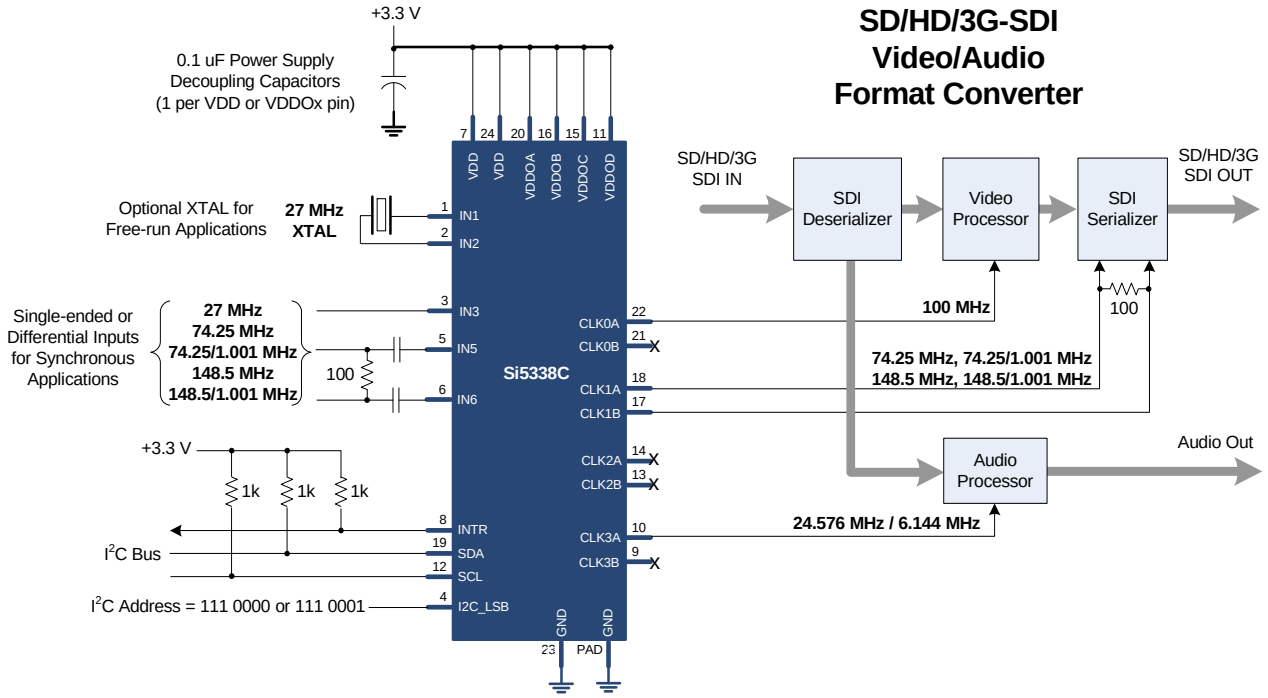
Table 14. I²C Specifications (SCL,SDA)[1]

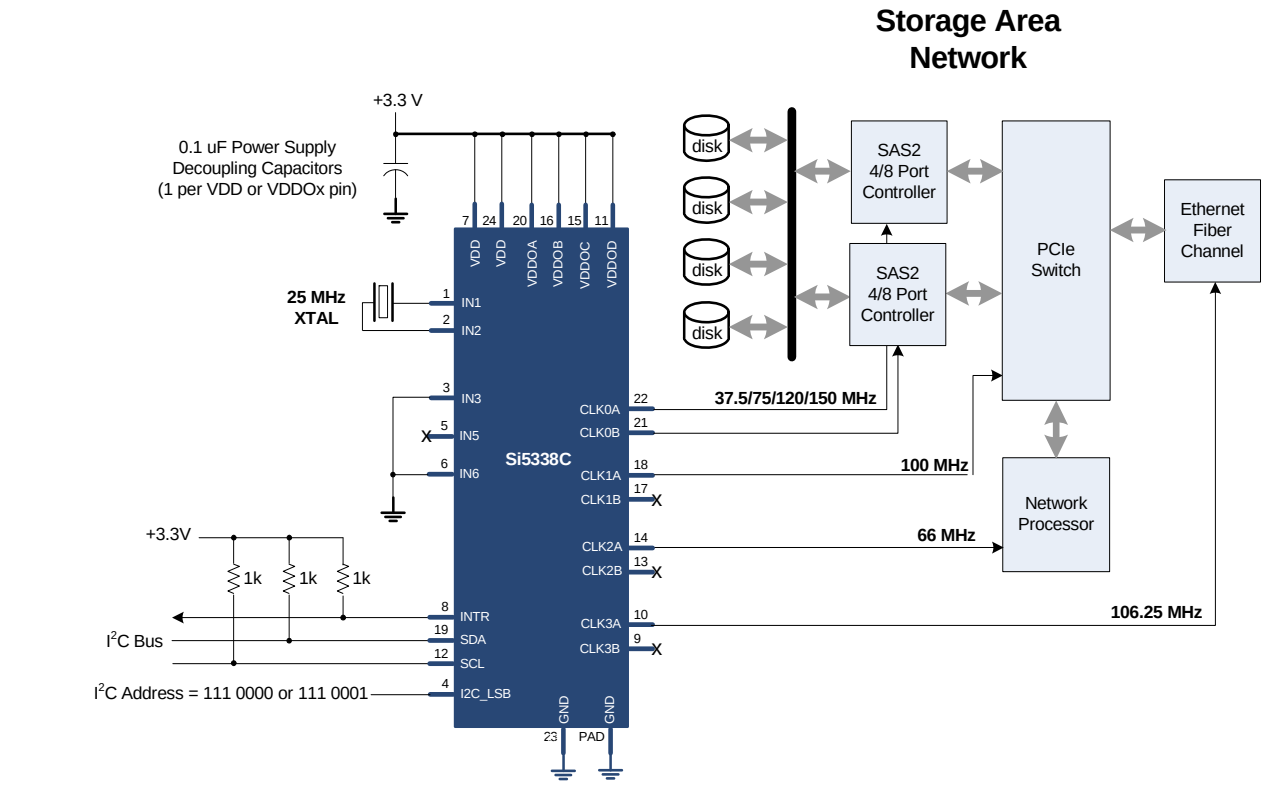
Parameter	Symbol	Test Condition	Standard Mode		Fast Mode		Unit
			Min	Max	Min	Max	
LOW Level Input Voltage	V_{ILI2C}		–0.5	0.3 x V_{DDI2C}	–0.5	0.3 x V_{DDI2C}[2]	V
HIGH Level Input Voltage	V_{IHI2C}		0.7 x V_{DDI2C}	3.63	0.7 x V_{DDI2C}[2]	3.63	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		N/A	N/A	0.1	—	V
LOW Level Output Voltage (open drain or open collector) at 3 mA Sink Current	V_{OLI2C}[2]	V_{DDI2C}[2] = 2.5/3.3 V	0	0.4	0	0.4	V
		V_{DDI2C}[2] = 1.8 V	N/A	N/A	0	0.2 x V_{DDI2C}	V
Input Current	I_{I2C}		–10	10	–10	10	µA
Capacitance for each I/O Pin	C_{I2C}	V_{IN} = –0.1 to V_{DDI2C}	—	4	—	4	pF
I²C Bus Timeout	—	Timeout Enabled	25	35	25	35	ms

Notes:

1. Refer to NXP's UM10204 I²C-bus specification and user manual, Revision 03, for further details: www.nxp.com/acrobat_download/usermanuals/UM10204_3.pdf.
2. Only I²C pullup voltages (VDDI2C) of 1.71 to 3.63 V are supported. Must write register 27[7] = 1 if the I²C bus voltage is less than 2.5 V to maintain compatibility with the I²C bus standard.

2. Typical Application Circuits





3. Functional Description

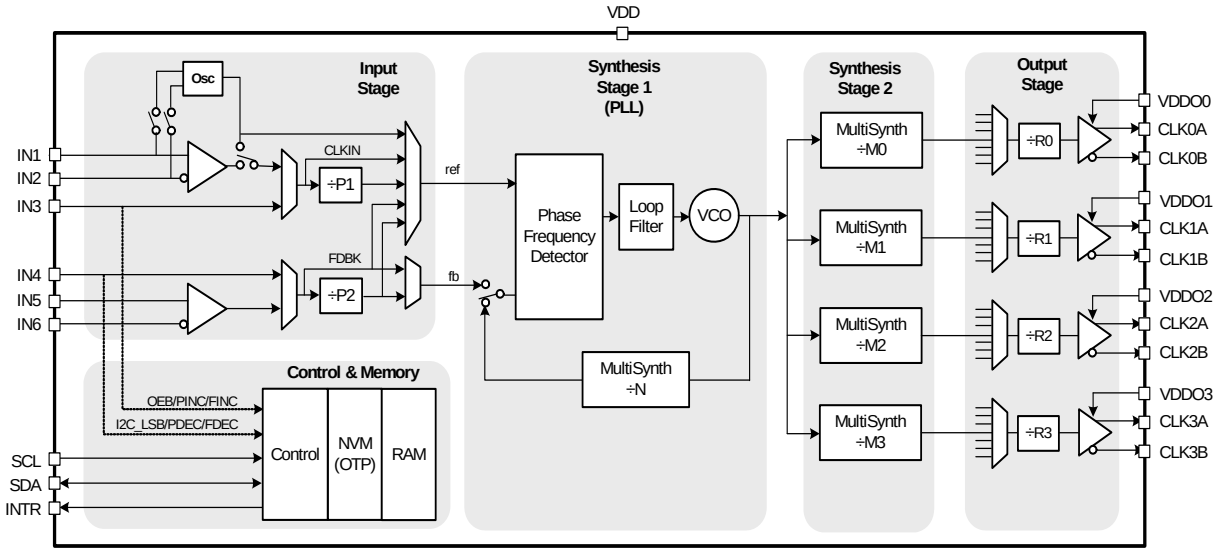


Figure 1. Si5338 Block Diagram

3.1. Overview

The Si5338 is a high-performance, low-jitter clock generator capable of synthesizing four independent user-programmable clock frequencies up to 350 MHz and select frequencies up to 710 MHz. The device supports free-run operation using an external crystal, or it can lock to an external clock for generating synchronous clocks. The output drivers support four differential clocks or eight single-ended clocks or a combination of both. The output drivers are configurable to support common signal formats, such as LVPECL, LVDS, HCSL, CMOS, HSTL, and SSTL. Separate output supply pins allow supply voltages of 3.3, 2.5, 1.8, and 1.5 V to support the multi-format output driver. The core voltage supply accepts 3.3, 2.5, or 1.8 V and is independent from the output supplies.

Using its two-stage synthesis architecture and patented high-resolution MultiSynth technology, the Si5338 can generate four independent frequencies from a single input frequency. In addition to clock generation, the inputs can bypass the synthesis stage enabling the Si5338 to be used as a high-performance clock buffer or a combination of a buffer and generator.

For applications that need fine frequency adjustments, such as clock margining, each of the synthesized frequencies can be incremented or decremented in user-defined steps as low as 1 ppm per step.

Output-to-output phase delays are also adjustable in user-defined steps with an error of <20 ps to compensate for PCB trace delays or for fine tuning of setup and hold margins.

A zero-delay mode is also available to help minimize input-to-output delay. Spread spectrum is available on each of the clock outputs for EMI-sensitive applications, such as PCI Express.

Configuration and control of the Si5338 is mainly handled through the I^2C/SMBus interface. Some features, such as output enable and frequency or phase adjustments, can optionally be pin controlled. The device has a maskable interrupt pin that can be monitored for loss of lock or loss of input signal conditions.

The device also provides the option of storing a user-definable clock configuration in its non-volatile memory (NVM), which becomes the default clock configuration at power-up.

3.1.1. ClockBuilder™ Desktop Software

To simplify device configuration, Silicon Labs provides ClockBuilder Desktop software. To ease these steps, Silicon Labs has released ClockBuilder Desktop. The software serves two purposes: configure the Si5338 with optimal divider ratios based on the desired frequencies, and to control the EVB, if connected to the host PC. The optimal configuration can be saved from the software in text files that can be used in any system, which configures the device over I^2C.

ClockBuilder Desktop can be downloaded from www.silabs.com/ClockBuilder and runs on Windows XP, Windows Vista, and Windows 7.

3.2. Input Stage

The input stage supports four inputs. Two are used as the *clock inputs* to the synthesis stage, and the other two are used as *feedback inputs* for zero delay or external feedback mode. In cases where external feedback is not required, all four inputs are available to the synthesis stage. The *reference selector* selects one of the inputs as the reference to the synthesis stage. The input configuration is selectable through the I^2C interface. The input MUXes are set automatically in ClockBuilder Desktop (see "3.1.1. ClockBuilder™ Desktop Software"). For information on setting the input MUXs manually, see "AN411: Configuring the Si5338".

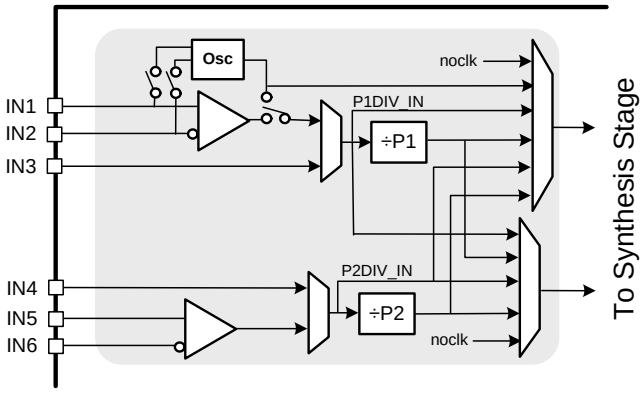


Figure 2. Input Stage

IN1/IN2 and IN5/IN6 are differential inputs capable of accepting clock rates from 5 to 710 MHz. The differential inputs are capable of interfacing to multiple signals, such as LVPECL, LVDS, HSCL, HCSL, and CML. Differential signals must be ac-coupled as shown in Figure 3. A termination resistor of 100 Ω placed close to the input pins is also required. Refer to Table 6 for signal voltage limits.

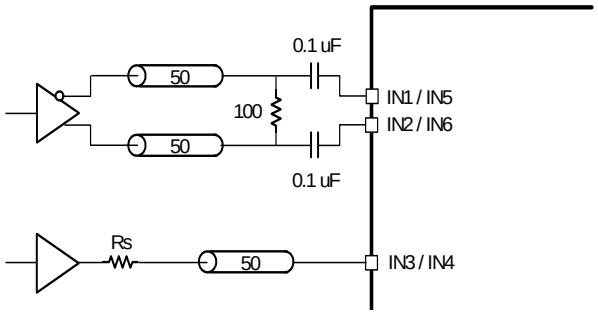


Figure 3. Interfacing Differential and Single-Ended Signals to the Si5338

IN3 and IN4 accept single-ended signals from 5 MHz to 200 MHz. The single-ended inputs are internally ac-coupled; so, they can accept a wide variety of signals without requiring a specific dc level. The input signal only needs to meet a minimum voltage swing and must not exceed a maximum VIH or a minimum VIL. Refer to Table 6 for signal voltage limits. A typical single-ended connection is shown in Figure 3. For additional termination options, refer to "AN408: Termination Options for Any-Frequency, Any-Output Clock Generators and Clock Buffers—Si5338, Si5334, Si5330".

For free-run operation, the internal oscillator can operate from a low-frequency fundamental mode crystal (XTAL) with a resonant frequency between 8 and 30 MHz. A crystal can easily be connected to pins IN1 and IN2 without external components as shown in Figure 4. See Tables 8–11 for crystal specifications that are guaranteed to work with the Si5338.

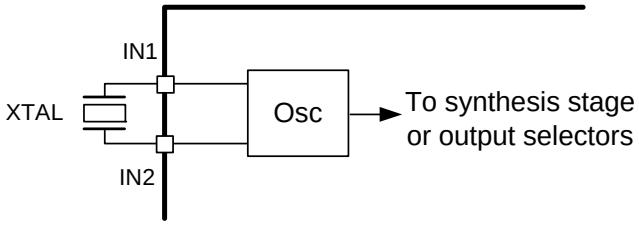


Figure 4. Connecting an XTAL to the Si5338

Refer to "AN360: Crystal Selection Guide for Si533x/5x Devices" for information on the crystal selection.

3.2.1. Loss-of-Signal (LOS) Alarm Detectors

There are two LOS detectors: LOS_CLKIN and LOS_FDBK. These detectors are tied to the outputs of the P1 and P2 frequency dividers, which are always enabled. See "3.6. Status Indicators" on page 22 for details on the alarm indicators. These alarms are used during programming to ensure that a valid input clock is detected. The input MUXs are set automatically in ClockBuilder Desktop (see AN411 to set manually).

3.3. Synthesis Stages

Next-generation timing applications require a wide range of frequencies that are often non-integer related. Traditional clock architectures address this by using multiple single PLL ICs, often at the expense of BOM complexity and power. The Si5338 uses patented MultiSynth technology to dramatically simplify timing architectures by integrating the frequency synthesis capability of four Phase-Locked Loops (PLLs) in a single device, greatly reducing size and power requirements versus traditional solutions.

Synthesis of the output clocks is performed in two stages, as shown in Figure 5. The first stage consists of a high-frequency analog phase-locked loop (PLL) that multiplies the input stage to a frequency within the range of 2.2 to 2.84 GHz. Multiplication of the input frequency is accomplished using a proprietary and highly precise MultiSynth feedback divider (N), which allows the PLL to generate any frequency within its VCO range with much less jitter than typical fractional N PLL.

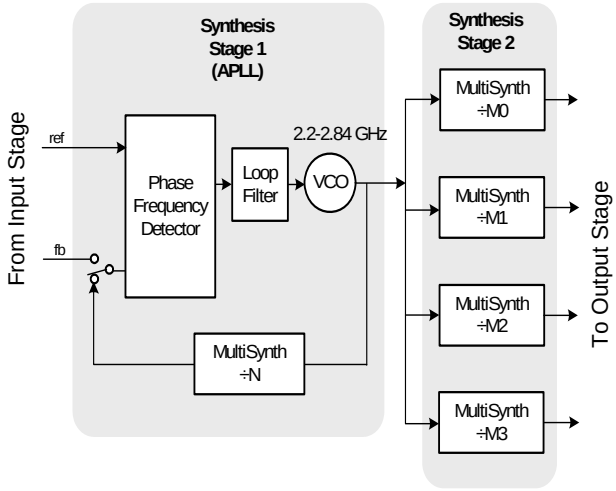


Figure 5. Synthesis Stages

The second stage of synthesis consists of the output MultiSynth dividers (M_x). Based on a fractional N divider, the MultiSynth divider shown in Figure 6 switches seamlessly between the two closest integer divider values to produce the exact output clock frequency with 0 ppm error.

To eliminate phase error generated by this process, the MultiSynth block calculates the relative phase difference between the clock produced by the fractional-N divider and the desired output clock and dynamically adjusts the phase to match the ideal clock waveform. This novel approach makes it possible to generate any output clock frequency without sacrificing jitter performance.

This architecture allows the output of each MultiSynth to produce any frequency from 5 to $F_{VCO}/8$ MHz. To support higher frequency operation, the MultiSynth divider can be bypassed. In bypass mode, integer divide ratios of 4 and 6 are supported. This allows for output frequencies of $F_{VCO}/4$ and $F_{VCO}/6$ MHz, which translates to 367–473.33 MHz and 550–710 MHz respectively. Because each MultiSynth uses the same VCO output, there are output frequency limitations when output frequencies greater than $F_{VCO}/8$ are desired.

For example, if 375 MHz is needed at the output of MultiSynth0, the VCO frequency would need to be 2.25 GHz. Now, all the other MultiSynths can produce any frequency from 5 MHz up to a maximum frequency of 2250/8 = 281.25 MHz. MultiSynth1,2,3 could also produce $F_{VCO}/4$ = 562.5 MHz or $F_{VCO}/6$ = 375 MHz. Only two unique frequencies above $F_{VCO}/8$ can be output: $F_{VCO}/6$ and $F_{VCO}/4$.

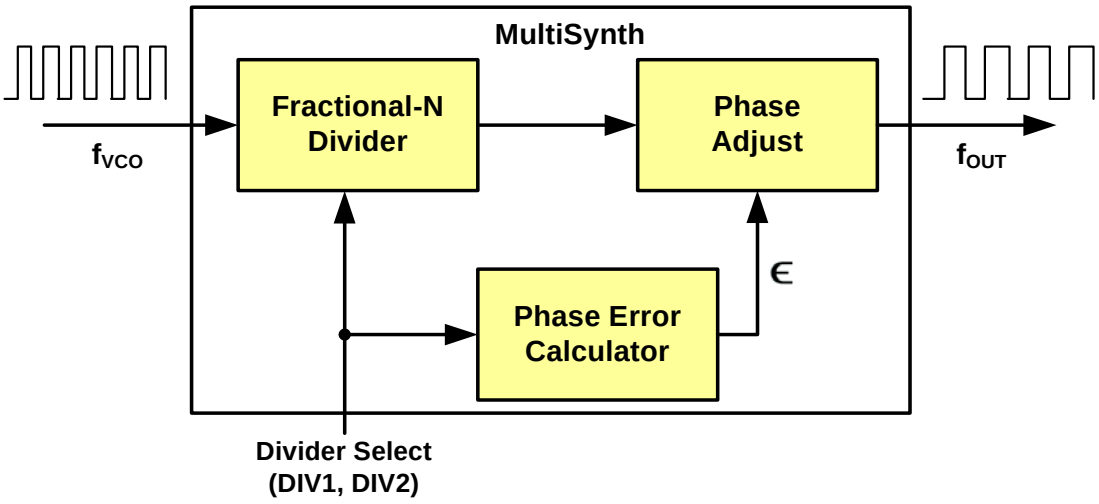


Figure 6. Silicon Labs' MultiSynth Technology

3.4. Output Stage

The output stage consists of output selectors, output dividers, and programmable output drivers as shown in Figure 7.

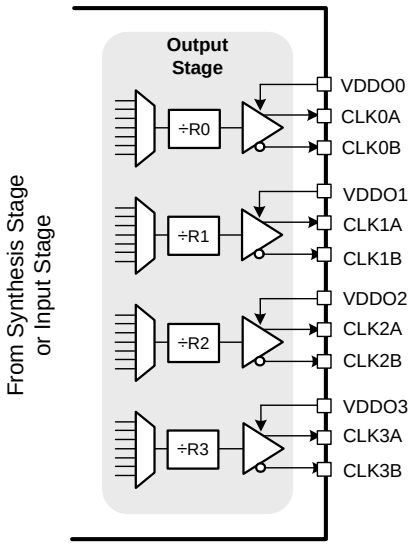


Figure 7. Output Stage

The output selectors select the clock source for the output drivers. By default, each output driver is connected to its own MultiSynth block (e.g. M0 to CLK0, M1 to CLK1, etc), but other combinations are possible by reconfiguring the device. The PLL can be bypassed by connected the input stage signals (osc, ref, refdiv, fb, or fbdiv) directly to the output divider. Bypassing an input directly to an output will not allow phase alignment of that output to other outputs. Each of the output drivers can also connect to the first MultiSynth block (M0) enabling a fan-out function. This allows the Si5338 to act as a clock generator, a fanout buffer, or a combination of both in the same package.

The output dividers (R0, R1, R2, R3) allow another stage of clock division.These dividers are configurable as divide by 1 (default), 2, 4, 8, 16, or 32. When an Rn does not equal 1, the phase alignment function for that output will not work.

The output drivers are configurable to support common signal formats, such as LVPECL, LVDS, HCSL, CMOS, HSTL, and SSTL. Separate output supply pins ($VDDO_n$) are provided for each output buffer.

The voltage on these supply pins can be 3.3, 2.5, 1.8, or 1.5 V as needed for the possible output formats. Additionally, the outputs can be configured to stop high, low, or tri-state when the PLL has lost lock. If the Si5338 is used in a zero delay mode, the output that is fed back must be set for always on, which will override any output disable signal.

Each of the outputs can also be enabled or disabled through the I^2C port. A single pin to enable/disable all outputs is available in the Si5338K/L/M.

3.5. Configuring the Si5338

The Si5338 is a highly-flexible clock generator that is entirely configurable through its I^2C interface. The device's default configuration is stored in non-volatile memory (NVM) as shown in Figure 8. The NVM is a one-time programmable memory (OTP), which can store a custom user configuration at power-up. This is a useful feature for applications that need a clock present at power-up (e.g., for providing a clock to a processor).

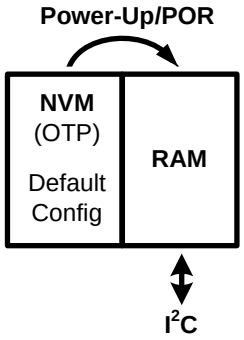


Figure 8. Si5338 Memory Configuration

During a power cycle or a power-on reset (POR), the contents of the NVM are copied into random access memory (RAM), which sets the device configuration that will be used during operation. Any changes to the device configuration after power-up are made by reading and writing to registers in the RAM space through the I^2C interface. ClockBuilder Desktop (see "3.1.1. ClockBuilder™ Desktop Software" on page 16) can be used to easily configure register map files that can be written into RAM (see "3.5.2. Creating a New Configuration for RAM" for details). Alternatively, the register map file can be created manually with the help of the equations in AN411.

Two versions of the Si5338 are available. First, standard, non-customized Si5338 devices are available in which the RAM can be configured in-circuit via I^2C (example part number Si5338C-A-GM). Alternatively, standard Si5338 devices can be field-programmed using the Si5338-PROG-EVB field programmer. Second, custom factory-programmed Si5338 devices are available that include a user-specified startup frequency configuration (example part number Si5338C-Axxxxx-GM).

3.5.1. Ordering a Custom NVM Configuration

The Si5338 is orderable with a factory-programmed custom NVM configuration. This is the simplest way of using the Si5338 since it generates the desired output frequencies at power-up or after a power-on reset (POR). This default configuration can be reconfigured in RAM through the I^2C interface after power-up (see “3.5.2. Creating a New Configuration for RAM”).

The first step in ordering a custom device is generating an NVM file which defines the input and output clock frequencies and signal formats. This is easily done using the ClockBuilder Desktop software (see "3.1.1. ClockBuilder™ Desktop Software" on page 16). This GUI based software generates an NVM file, which is used by the factory to manufacture custom parts. Each custom part is marked with a unique part number identifying the specific configuration (e.g., Si5338C-A00100-GM). Consult your local sales representative for more details on ordering a custom Si5338.

3.5.2. Creating a New Configuration for RAM

Any Si5338 device can be configured by writing to registers in RAM through the I^2C interface. A non-factory programmed device must be configured in this manner.

When writing a configuration to RAM, use the following procedure:

1. Create a device configuration (register map) using ClockBuilder Desktop (v2.7 or later; see "3.1.1. ClockBuilder™ Desktop Software" on page 16) or manually using the equations in “AN411: Configuring the Si5338”.
    a. Configure the frequency plan.
    b. Configure the output driver format and supply voltage.
    c. Configure frequency and/or phase inc/dec (if desired).
    d. Configure spread spectrum (if desired).
    e. Configure for zero-delay mode (if desired, see "3.9.5. Zero-Delay Mode" on page 24).
    f. If needed go to the Advanced tab and make additional configurations.
2. Save the configuration using the Options > Save Register Map File or Options > Save C code Header File, or create the register contents by the conversions listed in AN411.

3.5.3. Writing a Custom Configuration to RAM

Writing a new configuration (register map) to the RAM consists of pausing the LOL state-machine, writing new values to the IC accounting for the write-allowed mask given in "6.1. Register Write-Allowed Mask" on page 28, validating the input clock or crystal, locking the PLL to the input with the new configuration, restarting the LOL state-machine, and calibrating the VCO for robust operation across temperature. The flow chart in Figure 9 on page 21 enumerates the details:

Note: The write-allowed mask specifies which bits must be read and modified before writing the entire register byte (a.k.a. read-modify-write). “AN428: Jump Start: In-System, Flash-Based Programming for Silicon Labs’ Timing Products” illustrates the procedure defined in Section 3.5.2 with ANSI C code.

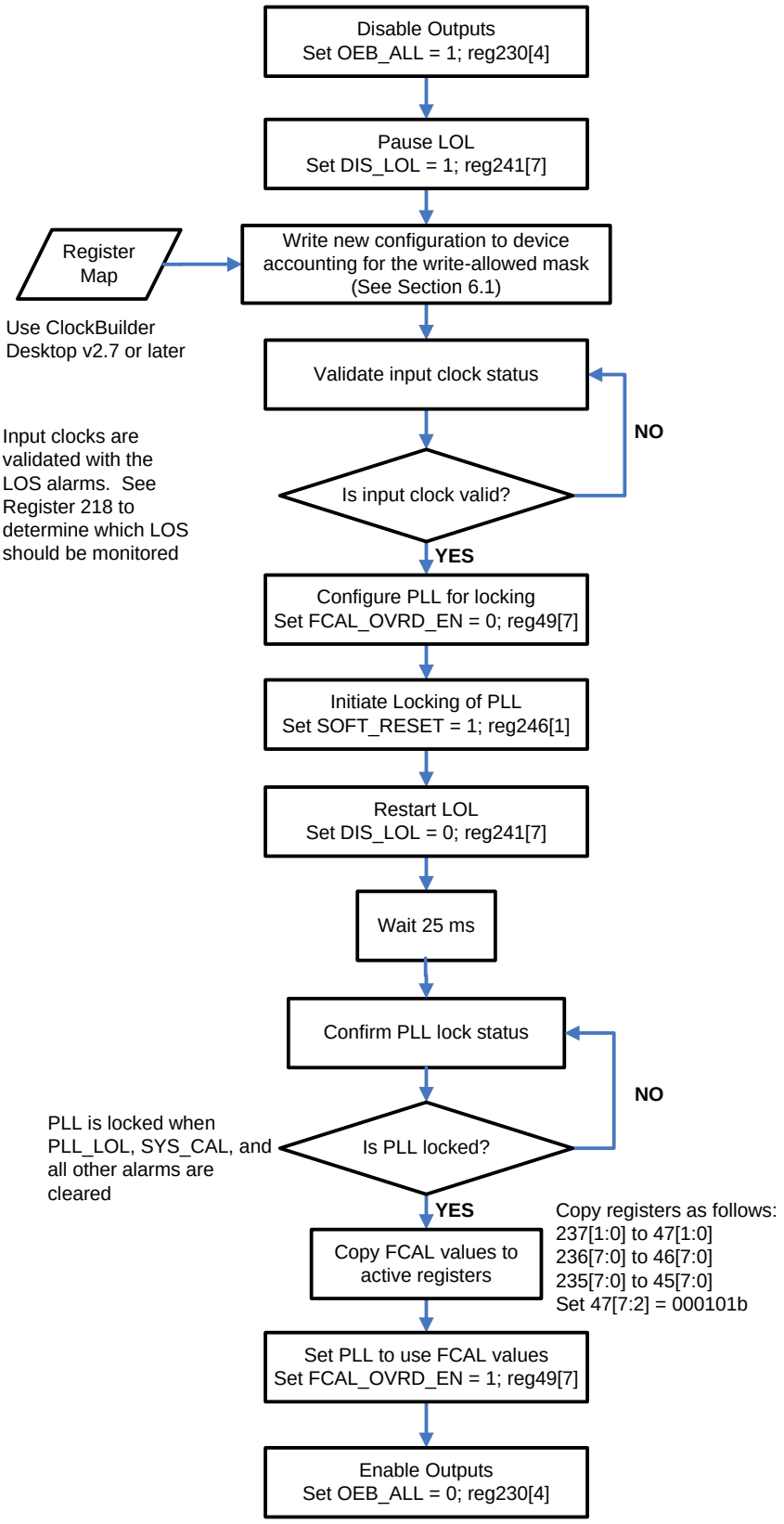


Figure 9. I²C Programming Procedure

3.5.4. Modifying a MultiSynth Output Divider Ratio/ Frequency Configuration

The output MultiSynth dividers of a configured and phase-locked Si5338 can be modified without relocking the PLL (i.e. without following section 3.5.3). This feature allows any of the four output frequencies to be modified without disturbing the others.

In this case, only write the set of registers associated with the output MultiSynth divider (MultiSynth Frequency Configuration; see Section 6.2). The feedback MultiSynth must not be modified unless following the procedure in Section 3.5.3.

To avoid intermediate frequencies, it is recommended that the output be disabled before changing the divider ratio (see Register 230).

Any output MultiSynth that is reconfigured will lose its phase alignment with the other outputs. SOFT_RESET can be used to resynchronize the outputs (see "3.8. Reset Options" on page 23).

3.5.5. Writing a Custom Configuration to NVM

An alternative to ordering an Si5338 with a custom NVM configuration is to use the field programming kit (Si5338-PROG-EVB) to write directly to the NVM of a "blank" Si5338. Since NVM is an OTP memory, it can only be written once. The default configuration can be reconfigured by writing to RAM through the I^2C interface (see “3.5.2. Creating a New Configuration for RAM”).

3.6. Status Indicators

A logic-high interrupt pin (INTR) is available to indicate a loss of signal (LOS) condition, a PLL loss of lock (PLL_LOL) condition, or that the PLL is in process of acquiring lock (SYS_CAL). PLL_LOL is held high when the input frequency drifts beyond the PLL lock range. It is held low during all other times and during a POR or soft reset. SYS_CAL is held high during a POR or SOFT reset so that no chattering occurs during the locking process. As shown in Figure 10, a status register at address 218 is available to help identify the exact event that caused the interrupt pin to become active.

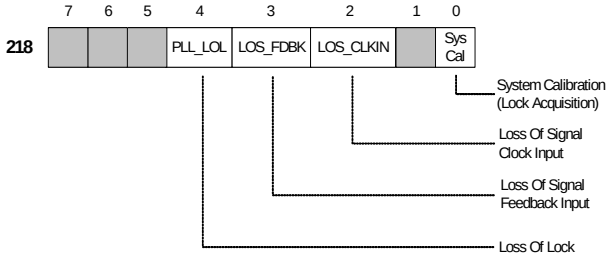


Figure 10. Status Register

Figure 11 shows a typical connection with the required pull-up resistor to VDD.

3.6.1. Using the INTR Pin in Systems with I^2C

The INTR output pin is not latched and thus it should not be a polled input to an MCU but an edge-triggered interrupt. An MCU can process an interrupt event by reading the sticky register 247 to see what event caused the interrupt. The same register can be cleared by writing zeros to the bits that were set. Individual interrupt bits can be masked by register 6[4:0].

3.6.2. Using the INTR Pin in Systems without I^2C

The INTR pin also provides a useful function in systems that require a pin-controlled fault indicator. Pre-setting the interrupt mask register allows the INTR pin to become an indicator for a specific event, such as LOS and/or LOL. Therefore, the INTR pin can be used to indicate a single fault event or even multiple events.

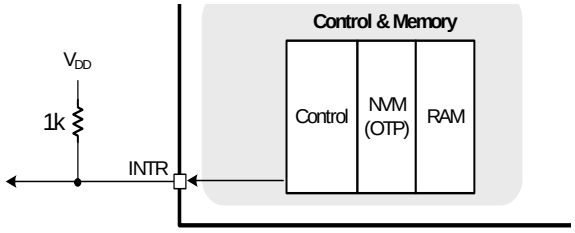


Figure 11. INTR Pin with Required Pull-Up

3.7. Output Enable

There are two methods of enabling and disabling the output drivers: Pin control, and I^2C control.

3.7.1. Enabling Outputs Using Pin Control

The Si5338K/L/M devices provide an Output Enable pin (OEB) as shown in Figure 12. Pulling this pin high will turn all outputs off. The state of the individual drivers when turned off is controllable. If an individual output is set to always on, then the OEB pin will not have an effect on that driver. Drive state options and always on are explained in “3.7.2. Enabling Outputs through the I^2C Interface”.

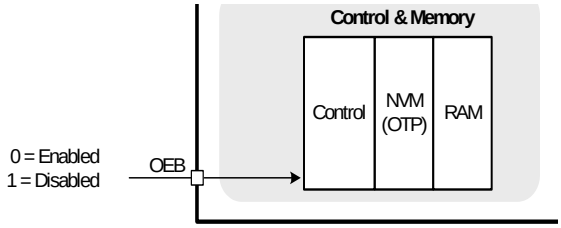


Figure 12. Output Enable Pin (Si5338K/L/M)

3.7.2. Enabling Outputs through the I²C Interface

Output enable can be controlled through the I²C interface. As shown in Figure 13, register 230[3:0] allows control of each individual output driver. Register 230[4] controls all drivers at once. When register 230[4] is set to disable all outputs, the individual output enables will have no effect. Registers 110[7:6], 114[7:6], 118[7:6], and 112[7:6] control the output disabled state as tri-state, low, high, or always on. If always on is set, that output will always be on regardless of any other register or chip state. In addition, the always on mode must be selected for an output that is fed back in a Zero Delay application.

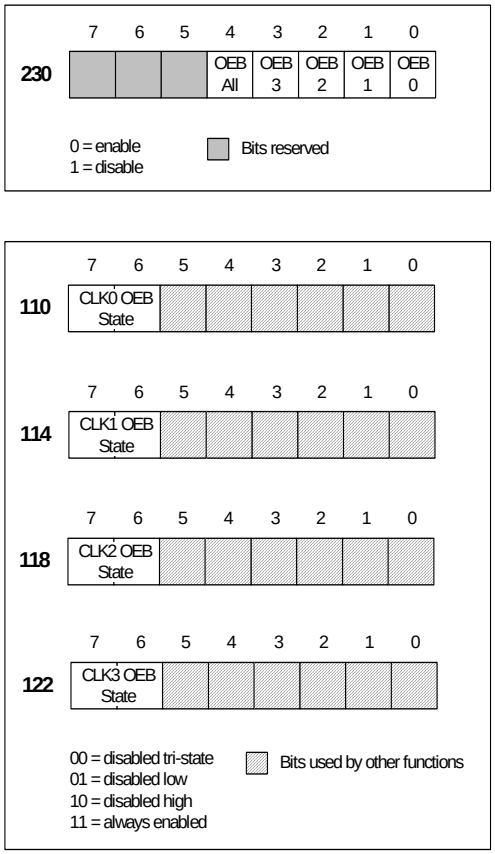


Figure 13. Output Enable Control Registers

3.8. Reset Options

There are two types of resets on the Si5338, POR and soft reset. A POR reset automatically occurs whenever the supply voltage on the VDD is applied.

The soft reset is forced by writing 0x02 to register 246. This bit is not self-clearing, and thus it may read back as a 1 or a 0. A soft reset will not download any pre-programmed NVM and will not change any register values in RAM.

The soft reset performs the following sequence:

1. All outputs turn off except if programmed to be always on.
2. Internal calibrations are done and MultiSynths are initialized.
   a. Outputs that are synchronous are phase aligned (if Rn = 1).
3. 25 ms is allowed for the PLL to lock (no delay occurs when FCAL_OVRD_EN = 1).
4. Turn on all outputs that were turned off in step 1.

3.9. Features of the Si5338

The Si5338 offers several features and functions that are useful in many timing applications. The following paragraphs describe in detail the main features and typical applications. All of these features can be easily configured using the ClockBuilder Desktop. See "3.1.1. ClockBuilder™ Desktop Software" on page 16.

3.9.1. Frequency Increment/Decrement

Each of the output clock frequencies can be independently stepped up or down in predefined steps as low as 1 ppm per step and with a resolution of 1 ppm. Setting of the step size and control of the frequency increment or decrement is accomplished through the I²C interface. Alternatively, the Si5338 can be ordered with optional frequency increment (FINC) and frequency decrement (FDEC) pins for pin-controlled applications. See Table 18 for ordering information of pin-controlled devices.

The frequency increment and decrement feature is useful in applications requiring a variable clock frequency (e.g., CPU speed control, FIFO overflow management, etc.) or in applications where frequency margining (e.g., f_{out} ±5%) is necessary for design verification and manufacturing test. Frequency increment or decrement can be applied as fast as 1.5 MHz when it is done by pin control. When under I²C control, the frequency increment and decrement update rate is limited by the I²C bus speed. The magnitude of the frequency step has 0 ppm error. Frequency steps are seamless and glitchless.

3.9.2. Output Phase Increment/Decrement

The Si5338 has a digitally-controlled glitchless phase increment and decrement feature that allows adjusting the phase of each output clock in relation to the other output clocks. The phase of each output clock can be adjusted with an accuracy of 20 ps over a range of ±45 ns. Setting of the step size and control of the phase increment or decrement is accomplished through the I^2C interface. Alternatively, the Si5338 can be ordered with optional phase increment (PINC) and phase decrement (PDEC) pins for pin-controlled applications. In pin controlled applications the phase increment and decrement update rate is as fast as 1.5 MHz. In I^2C applications, the maximum update rate is limited by the speed of the I^2C. See Table 18 for ordering information of pin-controlled devices.

The phase increment and decrement feature provides a useful method for fine tuning setup and hold timing margins or adjusting for mismatched PCB trace lengths.

3.9.3. Initial Phase Offset

Each output clock can be set for its initial phase offset up to ±45 ns. In order for the initial phase offset to be applied correctly at power up, the VDDOx output supply voltage must cross 1.2 V before the VDD (pins 7,24) core power supply voltage crosses 1.45 V. This applies to the each driver output individually. A soft_reset will also guarantee that the programmed Initial Phase Offset is applied correctly. The initial phase offset only works on outputs that have their R divider set to 1.

3.9.4. Output R Divider

When the requested output frequency of a channel is below 5 MHz, the Rn (n = 0,1,2,3) divider needs to be set and enabled. This is automatically done in register maps generated by the ClockBuilder Desktop. When the Rn divider is active the step size range of the frequency increment and decrement function will decrease by the Rn divide ratio. The Rn divider can be set to {1, 2, 4, 8, 16, 32}.

Non-unity settings of R0 will affect the Finc/Fdec step size at the MultiSynth0 output. For example, if the MultiSynth0 output step size is 2.56 MHz and R0 = 8, the step size at the output of R0 will be 2.56 MHz divided by 8 = .32 MHz. When the Rn divider is set to non-unity, the initial phase of the CLKn output with respect to other CLKn outputs is not guaranteed.

3.9.5. Zero-Delay Mode

The Si5338 supports an optional zero delay mode of operation for applications that require minimal input-to-output delay. In this mode, one of the device output clocks is fed back to the feedback input pin (IN4 or IN5/IN6) to implement an external feedback path essentially nullifying the delay between the reference input and the output clocks. Figure 14 shows the Si5338 in a typical zero-delay configuration. It is generally recommended that Clk3 be LVDS and that the feedback input be pins 5 and 6. For the differential input configuration to pins 5 and 6, see Figure 3 on page 17. The zero-delay mode combined with the phase increment/decrement feature allows unprecedented flexibility in generating clocks with precise edge alignment.

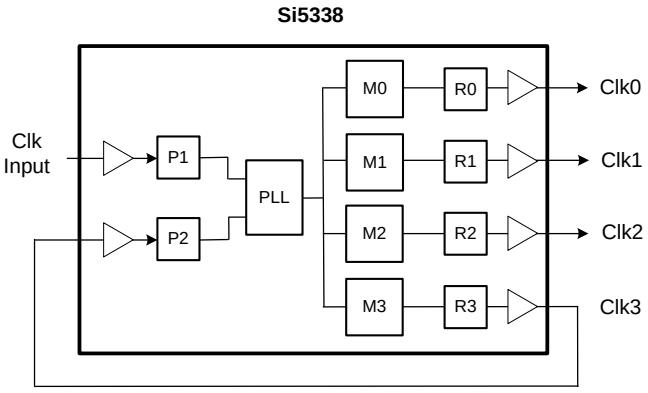


Figure 14. Si5338 in Zero Delay Clock Generator Mode

3.9.6. Spread Spectrum

To help reduce electromagnetic interference (EMI), the Si5338 supports spread spectrum modulation. The output clock frequencies can be modulated to spread energy across a broader range of frequencies, lowering system EMI. The Si5338 implements spread spectrum using its patented MultiSynth technology to achieve previously unattainable precision in both modulation rate and spreading magnitude as shown in Figure 15. Spread spectrum can be applied to any output clock, any clock frequency, and any spread amount. The device supports center spread (±0.1% to ±5%) and down spread (–0.1% to –5%). In addition, the device has extensive on-chip voltage regulation so that power supply variations do not influence the device's spread-spectrum clock waveforms.

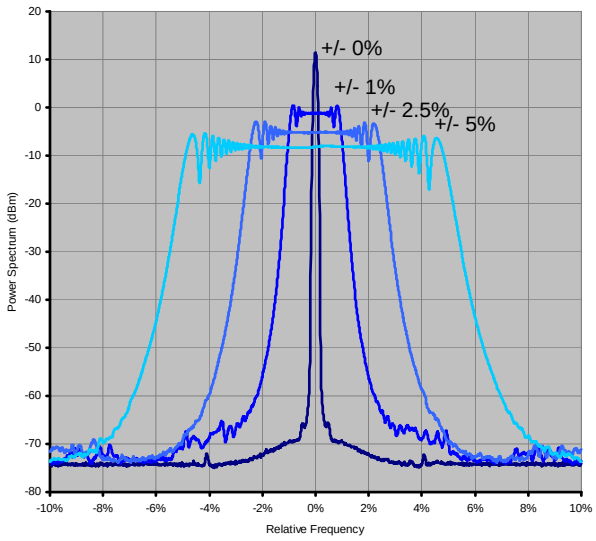


Figure 15. Configurable Spread Spectrum

4. Applications of the Si5338

Because of its flexible architecture, the Si5338 can be configured to serve several functions in the timing path. The following sections describe some common applications.

4.1. Free-Running Clock Generator

Using the internal oscillator (Osc) and an inexpensive external crystal (XTAL), the Si5338 can be configured as a free-running clock generator for replacing high-end and long-lead-time crystal oscillators found on many printed circuit boards (PCBs). Replacing several crystal oscillators with a single IC solution helps consolidate the bill of materials (BOM), reduces the number of suppliers, and reduces the number of long-lead-time components on the PCB. In addition, since crystal oscillators tend to be the least reliable aspect of many systems, the overall FIT rate improves with the elimination of each oscillator.

Up to four independent clock frequencies can be generated at any rate within its supported frequency range and with any of supported output types. Features, such as frequency increment and decrement and phase adjustments on a per-output basis, provide unprecedented flexibility for PCB designs. Figure 16 shows the Si5338 configured as a free-running clock generator.

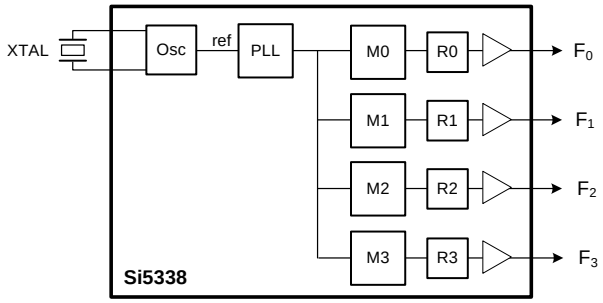


Figure 16. Si5338 as a Free-Running Clock Generator

4.2. Synchronous Frequency Translation

In other cases, it is useful to generate an output frequency that is synchronous (or phase-locked) to another clock frequency. The Si5338 is the ideal choice for generating up to four clocks with different frequencies with a fixed phase relationship to an input reference. Because of its highly precise frequency synthesis, the Si5338 can generate all four output frequencies with 0 ppm error to the input reference. The Si5338 is an ideal choice for applications that have traditionally required multiple stages of frequency synthesis to achieve complex frequency translations. Examples are in broadcast video (e.g., 148.5 MHz to 148.351648351648 MHz), WAN/LAN applications (e.g. 155.52 MHz to 156.25 MHz), and Forward Error Correction (FEC) applications (e.g., 156.25 MHz to 161.1328125 MHz). Using the input reference selectors, the Si5338 can select from one of four inputs (IN1/IN2, IN3, IN4, and IN5/IN6). Figure 17 shows the Si5338 configured as a synchronous clock generator. Frequencies and multiplication ratios may be entered into ClockBuilder Desktop using fractional notation to ensure that the exact scaling ratios can be achieved.

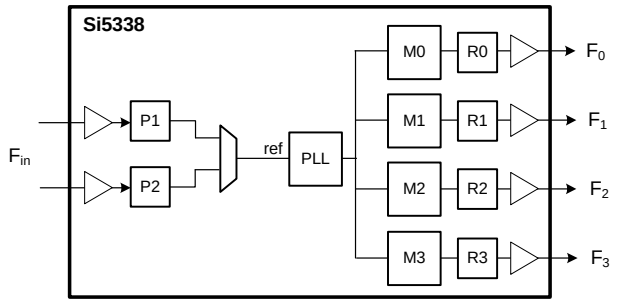


Figure 17. Si5338 as a Synchronous Clock Generator or Frequency Translator

4.3. Configurable Buffer and Level Translator

Using the output selectors, the synthesis stage can be entirely bypassed allowing the Si5338 to act as a configurable clock buffer/divider with level translation and selectable inputs. Because of its highly selectable configuration, virtually any combination is possible. The configurable output drivers allow four differential outputs, eight single-ended outputs, or a combination of both. Figure 18 shows the Si5338 configured as a flexible clock buffer.

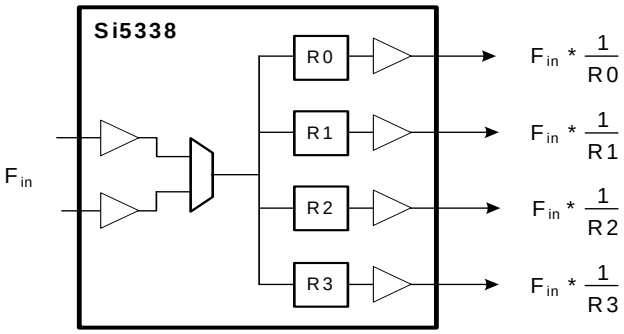


Figure 18. Si5338 as a Configurable Clock Buffer/Divider with Level Translation

4.3.1. Combination Free-Running and Synchronous Clock Generator

Another application of the Si5338 is in generating both free-running and synchronous clocks in one device. This is accomplished by configuring the input and output selectors for the desired split configuration. An example of such an application is shown in Figure 19.

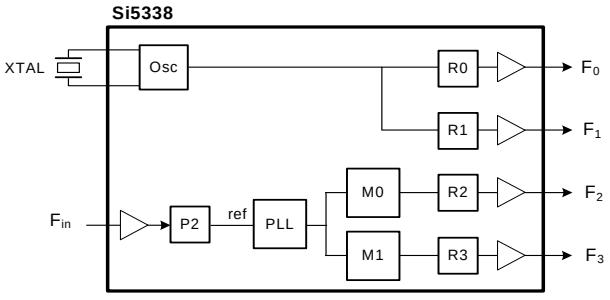


Figure 19. Si5338 In a Free-Running and Synchronous Clock Generator Application

5. I²C Interface

Configuration and operation of the Si5338 is controlled by reading and writing to the RAM space using the I²C interface. The device operates in slave mode with 7-bit addressing and can operate in Standard-Mode (100 kbps) or Fast-Mode (400 kbps) and supports burst data transfer with auto address increments.

The I²C bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL) as shown in Figure 20. Both the SDA and SCL pins must be connected to the VDD supply via an external pull-up as recommended by the I²C specification.

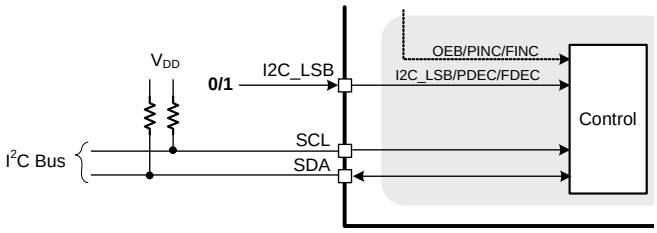


Figure 20. I²C and Control Signals

The 7-bit device (slave) address of the Si5338 consists of a 6-bit fixed address plus a user-selectable LSB bit as shown in Figure 21. The LSB bit is selectable using the optional I2C_LSB pin which is available as an ordering option for applications that require more than one Si5338 on a single I²C bus. Devices without the I2C_LSB pin option have a fixed 7-bit address of 70h (111 0000) as shown in Figure 21. Other custom I²C addresses are also possible. See Table 18 for details on device ordering information with the optional I2C_LSB pin.

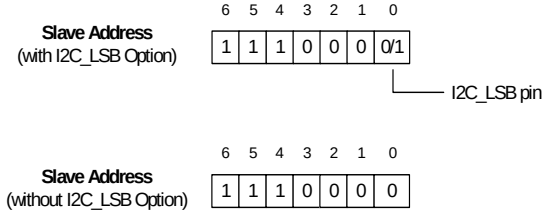


Figure 21. Si5338 I²C Slave Address

Data is transferred MSB first in 8-bit words as specified by the I²C specification. A write command consists of a 7-bit device (slave) address + a write bit, an 8-bit register address, and 8 bits of data as shown in Figure 22. A write burst operation is also shown where every additional data word is written using an auto-incremented address.

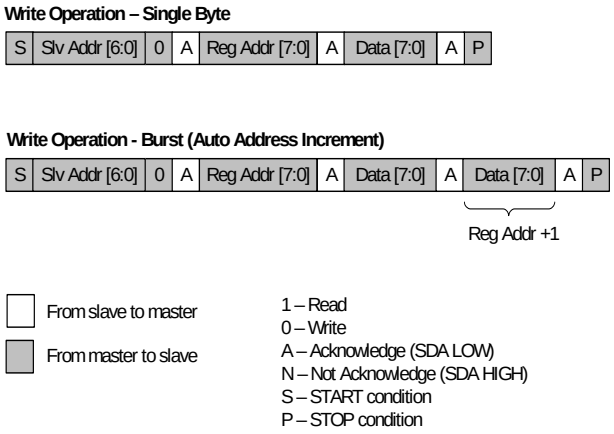


Figure 22. I²C Write Operation

A read operation is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. A read burst operation is also supported. This is shown in Figure 23.

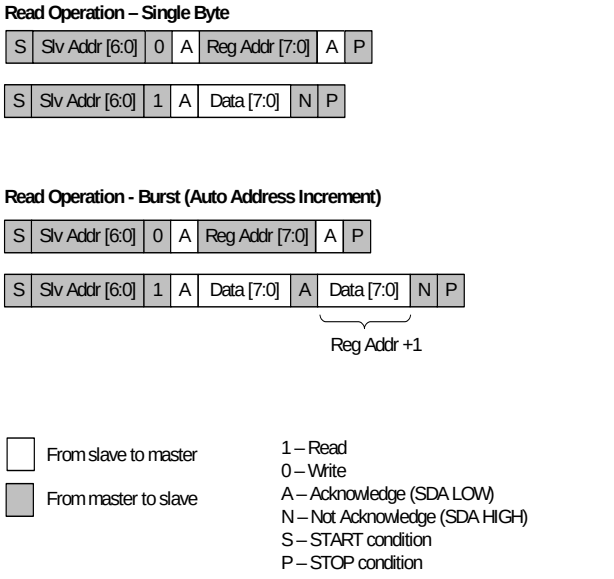


Figure 23. I²C Read Operation

AC and DC electrical specifications for the SCL and SDA pins are shown in Table 14. The timing specifications and timing diagram for the I²C bus are compatible with the I²C-Bus Standard. SDA timeout is supported for compatibility with SMBus interfaces.

The I²C bus can be operated at a bus voltage of 1.71 to 3.63 V and is 3.3 V tolerant. If a bus voltage of less than 2.5 V is used, register 27[7] = 1 must be written to maintain compatibility with the I²C bus standard.

6. Si5338 Registers

This section describes the registers and their usage in detail. These values are easily configured using ClockBuilder Desktop (see "3.1.1. ClockBuilder™ Desktop Software" on page 16). See AN428 for a working example using Silicon Labs' F301 MCU.

6.1. Register Write-Allowed Mask

The masks listed in Table 15 indicate which bits in each register of the Si5338 can be modified and which bits cannot. Therefore, these masks are write-allowed or write-enabled bits. These masks must be used to perform a read-modify-write on each register.

If a mask is 0x00, all bits in the associated register are reserved and must remain unchanged. If the mask is 0xFF, all the bits in the register can be changed. All other registers require a read-modify-write procedure to write to the registers. ClockBuilder Desktop can be used to create ANSI C code (Options → Save C code header file) with the register contents and mask values. AN428 demonstrates the usage of this header file and the read-modify-write procedure.

The following code demonstrates the application of the above write allowed mask.

- Let addr be the address of the register to access.
- Let data be the data or value to write to the register located at addr.
- Let mask be the write-allowed bits defined for the corresponding register.

```
// ignore registers with masks of 0x00
if(mask != 0x00){

        if(mask == 0xFF){
                // do a regular I2C write to the register
                // at addr with the desired data value
                write_Si5338(addr, data);

        } else {
                // do a read-modify-write using I2C and
                // bit-wise operations

                // get the current value from the device at the
                // register located at addr
                curr_val = read_Si5338(addr);

                // clear the bits that are allowed to be
                // accessed in the current value of the register
                clear_curr_val = curr_val AND (NOT mask);

                // clear the bits in the desired data that
                // are not allowed to be accessed
                clear_new_val = data AND mask;

                // combine the cleared values to get the new
                // value to write to the desired register
                combined = clear_curr_val OR clear_new_val;

                write_Si5338(addr, combined);
        }

}
```

Table 15. Register Write-Allowed Masks

Address (Decimal)	Mask (Hex)
0	0x00
1	0x00
2	0x00
3	0x00
4	0x00
5	0x00
6	0x1D
7	0x00
8	0x00
9	0x00
10	0x00
11	0x00
12	0x00
13	0x00
14	0x00
15	0x00
16	0x00
17	0x00
18	0x00
19	0x00
20	0x00
21	0x00
22	0x00
23	0x00
24	0x00
25	0x00
26	0x00
27	0x80
28	0xFF

***Note:** See Figure 9, “I2C Programming Procedure,” on page 21 for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).

Table 15. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
29	0xFF
30	0xFF
31	0xFF
32	0xFF
33	0xFF
34	0xFF
35	0xFF
36	0x1F
37	0x1F
38	0x1F
39	0x1F
40	0xFF
41	0x7F
42	0x3F
43	0x00
44	0x00
45	0xFF
46	0xFF
47	0x3F
48	0xFF
49	0xFF
50	0xFF
51	0xFF
52	0x7F
53	0xFF
54	0xFF
55	0xFF
56	0xFF
57	0xFF
***Note:** See Figure 9, “I2C Programming Procedure,” on page 21 for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).	

Table 15. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
58	0xFF
59	0xFF
60	0xFF
61	0xFF
62	0x3F
63	0x7F
64	0xFF
65	0xFF
66	0xFF
67	0xFF
68	0xFF
69	0xFF
70	0xFF
71	0xFF
72	0xFF
73	0x3F
74	0x7F
75	0xFF
76	0xFF
77	0xFF
78	0xFF
79	0xFF
80	0xFF
81	0xFF
82	0xFF
83	0xFF
84	0x3F
85	0x7F
86	0xFF

***Note:** See Figure 9, “I2C Programming Procedure,” on page 21 for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).

Table 15. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
87	0xFF
88	0xFF
89	0xFF
90	0xFF
91	0xFF
92	0xFF
93	0xFF
94	0xFF
95	0x3F
96	0x00
97	0xFF
98	0xFF
99	0xFF
100	0xFF
101	0xFF
102	0xFF
103	0xFF
104	0xFF
105	0xFF
106	0xBF
107	0xFF
108	0x7F
109	0xFF
110	0xFF
111	0xFF
112	0x7F
113	0xFF
114	0xFF
115	0xFF
***Note:** See Figure 9, “I2C Programming Procedure,” on page 21 for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).	

Table 15. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
116	0xFF
117	0xFF
118	0xFF
119	0xFF
120	0xFF
121	0xFF
122	0xFF
123	0xFF
124	0xFF
125	0xFF
126	0xFF
127	0xFF
128	0xFF
129	0x0F
130	0x0F
131	0xFF
132	0xFF
133	0xFF
134	0xFF
135	0xFF
136	0xFF
137	0xFF
138	0xFF
139	0xFF
140	0xFF
141	0xFF
142	0xFF
143	0xFF
144	0xFF
***Note:** See Figure 9, "I2C Programming Procedure," on page 21 for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).	

Table 15. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
145	0x00
146	0x00
147	0x00
148	0x00
149	0x00
150	0x00
151	0x00
152	0xFF
153	0xFF
154	0xFF
155	0xFF
156	0xFF
157	0xFF
158	0x0F
159	0x0F
160	0xFF
161	0xFF
162	0xFF
163	0xFF
164	0xFF
165	0xFF
166	0xFF
167	0xFF
168	0xFF
169	0xFF
170	0xFF
171	0xFF
172	0xFF
173	0xFF
***Note:** See Figure 9, "I2C Programming Procedure," on page 21 for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).	

Table 15. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
174	0xFF
175	0xFF
176	0xFF
177	0xFF
178	0xFF
179	0xFF
180	0xFF
181	0x0F
182	0xFF
183	0xFF
184	0xFF
185	0xFF
186	0xFF
187	0xFF
188	0xFF
189	0xFF
190	0xFF
191	0xFF
192	0xFF
193	0xFF
194	0xFF
195	0xFF
196	0xFF
197	0xFF
198	0xFF
199	0xFF
200	0xFF
201	0xFF
202	0xFF
***Note:** See Figure 9, "I2C Programming Procedure," on page 21 for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).	

Table 15. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
203	0x0F
204	0xFF
205	0xFF
206	0xFF
207	0xFF
208	0xFF
209	0xFF
210	0xFF
211	0xFF
212	0xFF
213	0xFF
214	0xFF
215	0xFF
216	0xFF
217	0xFF
218	0x00
219	0x00
220	0x00
221	0x00
222	0x00
223	0x00
224	0x00
225	0x00
226	0x04
227	0x00
228	0x00
229	0x00
230*	0xFF
231	0x00
***Note:** See Figure 9, "I2C Programming Procedure," on page 21 for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).	

Table 15. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
232	0x00
233	0x00
234	0x00
235	0x00
236	0x00
237	0x00
238	0x00
239	0x00
240	0x00
241*	0xFF
242	0x02
243	0x00
244	0x00
245	0x00
246*	0xFF
247	0x00
248	0x00
249	0x00
250	0x00
251	0x00
252	0x00
253	0x00
254	0x00
255	0xFF
256	0x00
257	0x00
258	0x00
259	0x00
260	0x00

***Note:** See Figure 9, “I2C Programming Procedure,” on page 21 for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).

Table 15. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
261	0x00
262	0x00
263	0x00
264	0x00
265	0x00
266	0x00
267	0x00
268	0x00
269	0x00
270	0x00
271	0x00
272	0x00
273	0x00
274	0x00
275	0x00
276	0x00
277	0x00
278	0x00
279	0x00
280	0x00
281	0x00
282	0x00
283	0x00
284	0x00
285	0x00
286	0x00
287	0xFF
288	0xFF
289	0xFF
***Note:** See Figure 9, "I2C Programming Procedure," on page 21 for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).	

Table 15. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
290	0xFF
291	0xFF
292	0xFF
293	0xFF
294	0xFF
295	0xFF
296	0xFF
297	0xFF
298	0xFF
299	0x0F
300	0x00
301	0x00
302	0x00
303	0xFF
304	0xFF
305	0xFF
306	0xFF
307	0xFF
308	0xFF
309	0xFF
310	0xFF
311	0xFF
312	0xFF
313	0xFF
314	0xFF
315	0x0F
316	0x00
317	0x00
318	0x00

***Note:** See Figure 9, “I2C Programming Procedure,” on page 21 for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).

Table 15. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
319	0xFF
320	0xFF
321	0xFF
322	0xFF
323	0xFF
324	0xFF
325	0xFF
326	0xFF
327	0xFF
328	0xFF
329	0xFF
330	0xFF
331	0x0F
332	0x00
333	0x00
334	0x00
335	0xFF
336	0xFF
337	0xFF
338	0xFF
339	0xFF
340	0xFF
341	0xFF
342	0xFF
343	0xFF
344	0xFF
345	0xFF
346	0xFF
347	0x0F
***Note:** See Figure 9, "I2C Programming Procedure," on page 21 for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).	

Table 15. Register Write-Allowed Masks (Continued)

Address (Decimal)	Mask (Hex)
348	0x00
349	0x00
350	0x00
***Note:** See Figure 9, "I2C Programming Procedure," on page 21 for the correct usage of registers 230, 241, and 246. These registers are not saved in the register map or C code header file from ClockBuilder Desktop (v2.7 or later).	

6.2. Register Categories

This is a list of registers needed to define the Configuration of a device. Set the PAGEBIT to access registers with addresses greater than 255.

Address (Decimal)	Bits	Function
6	4:0	Mask bits for LOS_CLKIN,LOS_FB, LOL, SYS_CAL
27	7:6	I^2C Configuration
27	7	
28 - 30	7:0	Input Mux Configuration
31 - 39	7:0	Output Configuration
40	7:0	Output Driver Trim Bits
41	6:0	
42	4:0	
47	5:2	Input Configuration
48	7:0	PLL Configuration
49	6:0	
50	7:0	
51	7:4, 2:0	
52	6:0	MultiSynth0 Freq inc/dec, SS, Phase inc/dec Configuration
53-61	7:0	MultiSynth0 frequency Configuration
62	5:0	
63	6:0	MultiSynth1 frequency Configuration
64-72	7:0	
73	5:0	
74	6:0	MultiSynth2 frequency Configuration
75-83	7:0	
84	5:0	
85	6:0	MultiSynth3 frequency Configuration
86-94	7:0	
95	5:0	
97-105	7:0	MultiSynthN Feedback divider Configuration
106	5:0	
107 - 110	7:0	MultiSynth0 Phase inc/dec, SS Configuration, drive state
111 - 114	7:0	MultiSynth1 Phase inc/dec, SS Configuration, drive state
115 - 118	7:0	MultiSynth2 Phase inc/dec, SS Configuration, drive state

Address (Decimal)	Bits	Function
119	7:0	MultiSynth3 Phase inc/dec, SS Configuration, drive state
120	6:0	
121 - 122	7:0	
123-128	7:0	MultiSynth0 freq inc/dec Configuration, ID config
129	3:0	
130	6:0	
131 - 144	7:0	
152 - 173	7:0	MultiSynth1 freq inc/dec Configuration
174 - 195	7:0	MultiSynth2 freq inc/dec Configuration
196 - 216	7:0	MultiSynth3 freq inc/dec Configuration
217	6:0	
241	7:0	Reserved - set to 0x65 if not factory-programmed.
287	7:0	MultiSynth0 spread spectrum Configuration
288	6:0	
289	7:0	
290	6:0	
291	7:0	
292	7:0	
293	7:0	
294	7:0	
295	6:0	
296	7:0	
297	6:0	
298	7:0	
299	7:0	

Address (Decimal)	Bits	Function
303	7:0	MultiSynth1 spread spectrum Configuration
304	6:0	
305	7:0	
306	6:0	
307	7:0	
308	7:0	
309	7:0	
310	7:0	
311	6:0	
312	7:0	
313	6:0	
314	7:0	
315	7:0	
319	7:0	MultiSynth2 spread spectrum Configuration
320	6:0	
321	7:0	
322	6:0	
323	7:0	
324	7:0	
325	7:0	
326	7:0	
327	6:0	
328	7:0	
329	6:0	
330	7:0	
331	7:0	

Address (Decimal)	Bits	Function
335	7:0	MultiSynth3 spread spectrum Configuration
336	6:0	
337	7:0	
338	6:0	
339	7:0	
340	7:0	
341	7:0	
342	7:0	
343	6:0	
344	7:0	
345	6:0	
346	7:0	
347	7:0	

6.3. Register Summary

Table 16. Register Summary

Register	7	6	5	4	3	2	1	0
0						REVID[2:0]		
6				PLL_LOL_ MASK	LOS_FDBK_ MASK	LOS_CLKIN_ MASK		SYS_CAL_ MASK
27	I2C_1P8_SEL	I2C_ADDR[6:0]						
28	FDBK_PDN		P2DIV_IN[0]	P1DIV_IN[2:0]			XTAL_FREQ[1:0]	
29	PFD_IN_REF[2:0]			P1DIV_IN[4:3]		P1DIV[2:0]		
30	PFD_IN_FB[2:0]			P2DIV_IN[2:1]		P2DIV[2:0]		
31	R0DIV_IN[2:0]			R0DIV[2:0]			MS0_PDN	DRV0_PDN
32	R1DIV_IN[2:0]			R1DIV[2:0]			MS1_PDN	DRV1_PDN
33	R2DIV_IN[2:0]			R2DIV[2:0]			MS2_PDN	DRV2_PDN
34	R3DIV_IN[2:0]			R3DIV[2:0]			MS3_PDN	DRV3_PDN
35	DRV3_VDDO[1:0]		DRV2_VDDO[1:0]		DRV1_VDDO[1:0]		DRV0_VDDO[1:0]	
36				DRV0_INV[1:0]		DRV0_FMT[2:0]		
37				DRV1_INV[1:0]		DRV1_FMT[2:0]		
38				DRV2_INV[1:0]		DRV2_FMT[2:0]		
39				DRV3_INV[1:0]		DRV3_FMT[2:0]		
40	DRV1_TRIM[2:0]			DRV0_TRIM[4:0]				
41		DRV2_TRIM[4:0]					DRV1_TRIM[4:3]	
42				DRV3_TRIM[4:0]				
45	FCAL_OVRD[7:0]							
46	FCAL_OVRD[15:8]							
47							FCAL_OVRD[17:16]	
48	PFD_EXTFB	PLL_KPHI[6:0]						
49	FCAL_OVRD_EN	VCO_GAIN[2:0]			RSEL[1:0]		BWSEL[1:0]	
50	PLL_ENABLE[1:0]		MSCAL[5:0]					
51	MS3_HS	MS2_HS	MS1_HS	MS0_HS		MS_PEC[2:0]		
52		MS0_FIDCT[1:0]		MS0_FIDDIS	MS0_SSMODE[1:0]		MS0_PHIDCT[1:0]	
53	MS0_P1[7:0]							
54	MS0_P1[15:8]							
55	MS0_P2[5:0]						MS0_P1[17:16]	
56	MS0_P2[13:6]							
57	MS0_P2[21:14]							
58	MS0_P2[29:22]							
59	MS0_P3[7:0]							

Table 16. Register Summary (Continued)

Register	7	6	5	4	3	2	1	0
60	MS0_P3[15:8]							
61	MS0_P3[23:16]							
62			MS0_P3[29:24]					
63		MS1_FIDCT[1:0]		MS1_FIDDIS	MS1_SSMODE[1:0]		MS1_PHIDCT[1:0]	
64	MS1_P1[7:0]							
65	MS1_P1[15:8]							
66	MS1_P2[5:0]						MS1_P1[17:16]	
67	MS1_P2[13:6]							
68	MS1_P2[21:14]							
69	MS1_P2[29:22]							
70	MS1_P3[7:0]							
71	MS1_P3[15:8]							
72	MS1_P3[23:16]							
73			MS1_P3[29:24]					
74		MS2_FRCTL[1:0]		MS2_FIDDIS	MS2_SSMODE[1:0]		MS2_PHIDCT[1:0]	
75	MS2_P1[7:0]							
76	MS2_P1[15:8]							
77	MS2_P2[5:0]						MS2_P1[17:16]	
78	MS2_P2[13:6]							
79	MS2_P2[21:14]							
80	MS2_P2[29:22]							
81	MS2_P3[7:0]							
82	MS2_P3[15:8]							
83	MS2_P3[23:16]							
84			MS2_P3[29:24]					
85		MS3_FIDCTL[1:0]		MS3_FIDDIS	MS3_SSMODE[1:0]		MS3_PHIDCTL[1:0]	
86	MS3_P1[7:0]							
87	MS3_P1[15:8]							
88	MS3_P2[5:0]						MS3_P1DIV[17:16]	
89	MS3_P2[13:6]							
90	MS3_P2[21:14]							
91	MS3_P2[29:22]							
92	MS3_P3[7:0]							
93	MS3_P3[15:8]							
94	MS3_P3[23:16]							
95			MS3_P3[29:24]					

Table 16. Register Summary (Continued)

Register	7	6	5	4	3	2	1	0
97	MSN_P1[7:0]							
98	MSN_P1[15:8]							
99	MSN_P2[5:0]						MSN_P1[17:16]	
100	MSN_P2[13:6]							
101	MSN_P2[21:14]							
102	MSN_P2[29:22]							
103	MSN_P3[7:0]							
104	MSN_P3[15:8]							
105	MSN_P3[23:16]							
106			MSN_P3[29:24]					
107	MS0_PHOFF[7:0]							
108		MS0_PHOFF[14:8]						
109	MS0_PHSTEP[7:0]							
110	CLK0_DISST[1:0]		MS0_PHSTEP[13:8]					
111	MS1_PHOFF[7:0]							
112		MS1_PHOFF[14:8]						
113	MS1_PHSTEP[7:0]							
114	CLK1_DISST[1:0]		MS1_PHSTEP[13:8]					
115	MS2_PHOFF[7:0]							
116		MS2_PHOFF[14:8]						
117	MS2_PHSTEP[7:0]							
118	CLK2_DISST[1:0]		MS2_PHSTEP[13:8]					
119	MS3_PHOFF[7:0]							
120		MS3_PHOFF[14:8]						
121	MS3_PHSTEP[7:0]							
122	CLK3_DISST[1:0]		MS3_PHSTEP[13:8]					
123	MS0_FIDP1[7:0]							
124	MS0_FIDP1[15:8]							
125	MS0_FIDP1[23:16]							
126	MS0_FIDP1[31:24]							
127	MS0_FIDP1[39:32]							
128	MS0_FIDP1[47:40]							
129					MS0_FIDP1[51:48]			
130					MS0_FIDP2[51:48]			
131	MS0_FIDP2[47:40]							
132	MS0_FIDP2[39:32]							

Table 16. Register Summary (Continued)

Register	7	6	5	4	3	2	1	0
133	MS0_FIDP2[31:24]							
134	MS0_FIDP2[23:16]							
135	MS0_FIDP2[15:8]							
136	MS0_FIDP2[7:0]							
137	MS0_FIDP3[7:0]							
138	MS0_FIDP3[15:8]							
139	MS0_FIDP3[23:16]							
140	MS0_FIDP3[31:24]							
141	MS0_FIDP3[39:32]							
142	MS0_FIDP3[47:40]							
143	MS0_FIDP3[51:48]							
144	MS0_ALL	MS0_FIDP3[62:56]						
152	MS1_FIDP1[7:0]							
153	MS1_FIDP1[15:8]							
154	MS1_FIDP1[23:16]							
155	MS1_FIDP1[31:24]							
156	MS1_FIDP1[39:32]							
157	MS1_FIDP1[47:40]							
158					MS1_FIDP1[51:48]			
159					MS1_FIDP2[51:48]			
160	MS1_FIDP2[47:40]							
161	MS1_FIDP2[39:32]							
162	MS1_FIDP2[31:24]							
163	MS1_FIDP2[23:16]							
164	MS1_FIDP2[15:8]							
165	MS1_FIDP2[7:0]							
166	MS1_FIDP3[7:0]							
167	MS1_FIDP3[15:8]							
168	MS1_FIDP3[23:16]							
169	MS1_FIDP3[31:24]							
170	MS1_FIDP3[39:32]							
171	MS1_FIDP3[47:40]							
172	MS1_FIDP3[51:48]							
173		MS1_FIDP3[62:56]						
174	MS2_FIDP1[7:0]							
175	MS2_FIDP1[15:8]							

Table 16. Register Summary (Continued)

Register	7	6	5	4	3	2	1	0
176	MS2_FIDP1[23:16]							
177	MS2_FIDP1[31:24]							
178	MS2_FIDP1[39:32]							
179	MS2_FIDP1[47:40]							
180					MS2_FIDP1[51:48]			
181					MS2_FIDP2[51:48]			
182	MS2_FIDP2[47:40]							
183	MS2_FIDP2[39:32]							
184	MS2_FIDP2[31:24]							
185	MS2_FIDP2[23:16]							
186	MS2_FIDP2[15:8]							
187	MS2_FIDP2[7:0]							
188	MS2_FIDP3[7:0]							
189	MS2_FIDP3[15:8]							
190	MS2_FIDP3[23:16]							
191	MS2_FIDP3[31:24]							
192	MS2_FIDP3[39:32]							
193	MS2_FIDP3[47:40]							
194	MS2_FIDP3[51:48]							
195		MS2_FIDP3[62:56]						
196	MS3_FIDP1[7:0]							
197	MS3_FIDP1[15:8]							
198	MS3_FIDP1[23:16]							
199	MS3_FIDP1[31:24]							
200	MS3_FIDP1[39:32]							
201	MS3_FIDP1[47:40]							
202					MS3_FIDP1[51:48]			
203					MS3_FIDP2[51:48]			
204	MS3_FIDP2[47:40]							
205	MS3_FIDP2[39:32]							
206	MS3_FIDP2[31:24]							
207	MS3_FIDP2[23:16]							
208	MS3_FIDP2[15:8]							
209	MS3_FIDP2[7:0]							
210	MS3_FIDP3[7:0]							
211	MS3_FIDP3[15:8]							

Table 16. Register Summary (Continued)

Register	7	6	5	4	3	2	1	0
212	MS3_FIDP3[23:16]							
213	MS3_FIDP3[31:24]							
214	MS3_FIDP3[39:32]							
215	MS3_FIDP3[47:40]							
216	MS3_FIDP3[51:48]							
217		MS3_FIDP3[62:56]						
218				PLL_LOL	LOS_FDBK	LOS_CLKIN		SYS_CAL
230				OEB_ALL	OEB_3	OEB_2	OEB_1	OEB_0
235	FCAL[7:0]							
236	FCAL[15:8]							
237						FCAL[17:16]		
241	DIS_LOL							
242							DCLK_DIS	
246							SOFT_RESET	
247				PLL_LOL_STK	LOS_FDBK_STK	LOS_CLKIN_STK		SYS_CAL_STK
255								PAGE_SEL
287	MS0_SSUPP2[7:0]							
288		MS0_SSUPP2[14:8]						
289		MS0_SSUPP3[7:0]						
290		MS0_SSUPP3[14:8]						
291	MS0_SSUPP1[7:0]							
292	MS0_SSUDP1[3:0]				MS0_SSUPP1[11:8]			
293	MS0_SSUDP1[11:4]							
294	MS0_SSDNP2[7:0]							
295		MS0_SSDNP2[14:8]						
296	MS0_SSDNP3[7:0]							
297		MS0_SSDNP3[14:8]						
298	MS0_SSDNP1[7:0]							
299					MS0_SSDNP1[11:8]			
303	MS1_SSUPP2[7:0]							
304		MS1_SSUPP2[14:8]						
305	MS1_SSUPP3[7:0]							
306		MS1_SSUPP3[14:8]						
307	MS1_SSUPP1[7:0]							
308	MS1_SSUDP1[3:0]				MS1_SSUPP1[11:8]			

Table 16. Register Summary (Continued)

Register	7	6	5	4	3	2	1	0
309	MS1_SSUDP1[11:4]							
310	MS1_SSDNP2[7:0]							
311		MS1_SSDNP2[14:8]						
312	MS1_SSDNP3[7:0]							
313		MS1_SSDNP3[14:8]						
314	MS1_SSDNP1[7:0]							
315					MS1_SSDNP1[11:8]			
319	MS2_SSUPP2[7:0]							
320		MS2_SSUPP2[14:8]						
321	MS2_SSUPP3[7:0]							
322		MS2_SSUPP3[14:8]						
323	MS2_SSUPP1[7:0]							
324	MS2_SSUDP1[3:0]				MS2_SSUPP1[11:8]			
325	MS2_SSUDP1[11:4]							
326	MS2_SSDNP2[7:0]							
327		MS2_SSDNP2[14:8]						
328	MS2_SSDNP3[7:0]							
329		MS2_SSDNP3[14:8]						
330	MS2_SSDNP1[7:0]							
331					MS2_SSDNP1[11:8]			
335	MS3_SSUPP2[7:0]							
336		MS3_SSUPP2[14:8]						
337	MS3_SSUPP3[7:0]							
338		MS3_SSUPP3[14:8]						
339	MS3_SSUPP1[7:0]							
340	MS3_SSUDP1[3:0]				MS3_SSUPP1[11:8]			
341	MS3_SSUDP1[11:4]							
342	MS3_SSDNP2[7:0]							
343		MS3_SSDNP2[14:8]						
344	MS3_SSDNP3[7:0]							
345		MS3_SSDNP3[14:8]						
346	MS3_SSDNP1[7:0]							
347					MS3_SSDNP1[11:8]			

6.4. Register Descriptions

In many registers, the byte reset value contains one or more “x”s because a factory-programmed device can have multiple values for these bits.

Register 0.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						REVID[2:0]		
Type	R							

Reset value = xxxx xxxx

Bit	Name	Function
7:3	Reserved	**Reserved.**
2:0	REVID[2:0]	Device Revision ID.

Register 6.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				PLL_LOL_MASK	LOS_FDBK_MASK	LOS_CLKIN_MASK	Reserved	SYS_CAL_MASK
Type				R/W	R/W	R/W		R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	Reserved. Must only write 000b to these bits.
4	PLL_LOL_MASK	**Mask Bit for PLL_LOL.** When true, the PLL_LOL bit (Register 218) will not cause an interrupt. See also Register 247. 0: PLL Loss of Lock (LOL) triggers active interrupt on INTR output pin. 1: PLL Loss of Lock (LOL) ignored in generating interrupt output.
3	LOS_FDBK_MASK	**Mask Bit for Loss of Signal on IN4 or IN5,6.** When true, the LOS_FDBK bit (Register 218) will not cause an interrupt. See also Register 247. 0: FDBK LOS triggers active interrupt on INTR output pin. 1: FDBK LOS ignored in generating interrupt output.
2	LOS_CLKIN_MASK	**Mask Bit for Loss of Signal on IN1,2 or IN3.** When true, the LOS_CLKIN bit (Register 218) will not cause an interrupt. See also Register 247. 0: CLKIN LOS triggers active interrupt on INTR output pin. 1: CLKIN LOS ignored in generating interrupt output.
1	Reserved	Reserved. Must only write 0 to this bit.
0	SYS_CAL_MASK	**Chip Calibration Mask Bit.** When true, the SYS_CAL bit (Register 218) will not cause an interrupt. See also Register 247. 0:PLL self-calibration triggers active interrupt on INTR output pin. 1:PLL self-calibration ignored in generating interrupt output.

Register 27.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	I2C_1P8_SEL	I2C_ADDR[6:0]						
Type	R/W	R/W*						

Reset value = xxxx xxxx

Bit	Name	Function
7	I2C_1P8_SEL	**I^2C Reference V_{DD}.** External I2C VDD 0 = 3.3 V/2.5 V, 1 = 1.8 V. 0: 3.3 V/2.5 V (default) 1: 1.8 V
6:0*	I2C_ADDR[6:0]	**7-Bit I^2C Address.** If and only if there is an I2C_LSB pin, the actual I^2C LSB address is the logical “or” of the bit in position 0 with the state of the I2C_LSB pin. Otherwise, the actual I2C_LSB is the LSB of this 7-bit address. Custom 7-bit I^2C addresses may be requested but must be even numbers if pin control of the I^2C address is to be implemented. For example, if the I^2C address = 70h, the I2C_LSB pin can change the LSB from 0 to 1. However, if the I^2C address = 71h, the I2C_LSB pin will have no effect upon the I^2C address.
***Note:** Although these bits are R/W, writing them is not supported. Custom I^2C addresses can be set at the factory. Contact your local sales office for details.		

Register 28.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			P2DIV_IN[0]	P1DIV_IN[2:0]			XTAL_FREQ[1:0]	
Type	R/W		R/W	R/W			R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	Reserved. Must only write a 00 to these bits.
5	P2DIV_IN[0]	This bit and Register 30[4:3] create a 3-bit field that selects the input to the P2 divider [reg30[4:3] reg28[5]] = P2DIV_IN[2:0]. 000b: Clock from IN5,IN6 is input to P2 divider 011b: Clock from IN4 is input to P2 100b: No clock is input to P2 All other bit values are reserved.
4:2	P1DIV_IN[2:0]	These three bits are combined with Register 29[4:3] and create a 5-bit field that selects the input to the P1 divider [reg29[4:3] reg28[4:2]] = P1DIV_IN[4:0]. 00000b: Clock from IN1,IN2 selected 01010b: Clock from IN3 selected 10101b: Crystal oscillator selected All other bit values are reserved and should not be written.
1:0	XTAL_FREQ[1:0]	**Crystal Frequency Range.** Select Xtal Frequency that you are using. For more information on using crystals, see “AN360: Crystal Selection Guide for Si533x/5x Devices”. 0: 8–11 MHz 1: 11–19 MHz 2: 19–26 MHz 3: 26–30 MHz

Register 29.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PFD_IN_REF[2:0]			P1DIV_IN[4:3]		P1DIV[2:0]		
Type	R/W			R/W		R/W		

Reset value = xxxx xxxx

Bit	Name	Function
7:5	PFD_IN_REF[2:0]	Selects the input clock to be provided to the reference input of PLL Phase Frequency Detector (PFD). 0: P1DIV_IN selected 1: P2DIV_IN selected 2: P1DIV_OUT (P1 divider output) selected 3: P2DIV_OUT (P2 divider output) selected 4: XOCLK selected 5: No Clock selected 6: Reserved 7: Reserved
4:3	P1DIV_IN[4:3]	These two bits along with reg28[4:2] create a 5-bit field that selects the input to the P1 divider [reg29[4:3] reg28[4:2]] = P1DIV_IN[4:0]. 00000b: Clock from IN,2 selected 01010b: Clock from IN3 selected 10101b: Crystal oscillator selected All other bit values are reserved
2:0	P1DIV[2:0]	Sets the value of the P1 divider. 0: Divide by 1 1: Divide by 2 2: Divide by 4 3: Divide by 8 4: Divide by 16 5: Divide by 32

Register 30.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PFD_IN_FB[2:0]			P2DIV_IN[2:1]		P2DIV[2:0]		
Type	R/W			R/W		R/W		

Reset value = xxxx xxxx

Bit	Name	Function
7:5	PFD_IN_FB[2:0]	Selects the external input applied to the PFD feedback input. See also Register 48[7]. 0: P2DIV_IN (fbclk) 1: P1DIV_IN (refclk) 2: P2DIV_OUT (P2 divider output) selected 3: P1DIV_OUT (P1 divider output) selected 4: Reserved 5: No Clock selected 6: Reserved 7: Reserved
4:3	P2DIV_IN[2:1]	These two bits and Register 28[5] create a 3-Bit field that selects the input to the P2 divider [reg30[4:3] reg28[5]] = P2DIV_IN[2:0]. 000b: Clock from IN5,IN6 is input to P2 divider 011b: Clock from IN4 is input to P2 100b: No clock is input to P2 All other bit values are reserved.
2:0	P2DIV[2:0]	Sets the value of the P2 the divider. 0: Divide by 1 1: Divide by 2 2: Divide by 4 3: Divide by 8 4: Divide by 16 5: Divide by 32

Register 31.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	R0DIV_IN[2:0]			R0DIV[2:0]			MS0_PDN	DRV0_PDN
Type	R/W			R/W			R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	R0DIV_IN[2:0]	Selects the input to the R0 divider. R0 divider output goes to CLK0. 0: P2DIV_IN (fbclk) selected 1: P1DIV_IN (refclk) selected 2: P2DIV_OUT (P2 divider output) selected 3: P1DIV_OUT (P1 divider output) selected 4: XOCLK selected 5: MultiSynth0 output selected 6: MultiSynth0 output selected 7: No Clock selected
4:2	R0DIV[2:0]	**CLK0 R0 Output Divider.** 0: Divide by 1 1: Divide by 2 2: Divide by 4 3: Divide by 8 4: Divide by 16 5: Divide by 32
1	MS0_PDN	**MultiSynth0 Power Down.** 0: MS0 MultiSynth powered up 1: MS0 MultiSynth powered down
0	DRV0_PDN	**R0 and CLK0 Power Down.** 0: R0 output divider and CLK0 driver powered up 1: R0 output divider and CLK0 driver powered down

Register 32.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	R1DIV_IN[2:0]			R1DIV[2:0]			MS1_PDN	DRV1_PDN
Type	R/W			R/W			R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	R1DIV_IN[2:0]	Selects the input to the R1 divider. R1 divider output goes to CLK1. 0: P2DIV_IN (fbclk) selected 1: P1DIV_IN (refclk) selected 2: P2DIV_OUT (P2 divider output) selected 3: P1DIV_OUT (P1 divider output) selected 4: XOCLK selected 5: MultiSynth0 output selected 6: MultiSynth1 output selected 7: No Clock selected
4:2	R1DIV[2:0]	**CLK1 R1 Output Divider.** 0: Divide by 1 1: Divide by 2 2: Divide by 4 3: Divide by 8 4: Divide by 16 5: Divide by 32
1	MS1_PDN	**MultiSynth1 Power Down.** 0: MultiSynth1 is powered up 1: MultiSynth1 is powered down
0	DRV1_PDN	**R1 and CLK1 Power Down.** 0: R1 output divider and CLK1 driver powered up 1: R1 output divider and CLK1 driver powered down

Register 33.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	R2DIV_IN[2:0]			R2DIV[2:0]			MS2_PDN	DRV2_PDN
Type	R/W			R/W			R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	R2DIV_IN[2:0]	Selects the input to the R2 divider. R2 divider output goes to CLK2. 0: P2DIV_IN (fbclk) selected 1: P1DIV_IN (refclk) selected 2: P2DIV_OUT (P2 divider output) selected 3: P1DIV_OUT (P1 divider output) selected 4: XOCLK selected 5: MultiSynth0 output selected 6: MultiSynth2 output selected 7: No Clock selected
4:2	R2DIV[2:0]	**CLK2 R2 Output Divider.** 0: Divide by 1 1: Divide by 2 2: Divide by 4 3: Divide by 8 4: Divide by 16 5: Divide by 32
1	MS2_PDN	**MultiSynth2 Power Down.** 0: MultiSynth2 powered up 1: MultiSynth2 powered down
0	DRV2_PDN	**R2 and CLK2 Power Down.** 0: R2 output divider and CLK2 driver powered up 1: R2 output divider and CLK2 driver powered down

Register 34.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	R3DIV_IN[2:0]			R3DIV[2:0]			MS3_PDN	DRV3_PDN
Type	R/W			R/W			R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	R3DIV_IN[2:0]	Selects the input to the R3 divider. R3 divider output goes to CLK3. 0: P2DIV_IN (fbclk) selected 1: P1DIV_IN (refclk) selected 2: P2DIV_OUT (P2 divider output) selected 3: P1DIV_OUT (P1 divider output) selected 4: XOCLK selected 5: MultiSynth0 output selected 6: MultiSynth3 output selected 7: No Clock selected
4:2	R3DIV[2:0]	**CLK3 R3 Output Divider.** 0: Divide by 1 1: Divide by 2 2: Divide by 4 3: Divide by 8 4: Divide by 16 5: Divide by 32
1	MS3_PDN	**MultiSynth3 Power Down.** 0: MultiSynth3 is power up 1: MultiSynth3 powered down
0	DRV3_PDN	**R3 and CLK3 Powerdown.** 0: R3 output divider and CLK3 driver powered up 1: R3 output divider and CLK3 driver powered down

Register 35.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DRV3_VDDO[1:0]		DRV2_VDDO[1:0]		DRV1_VDDO[1:0]		DRV0_VDDO[1:0]	
Type	R/W		R/W		R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:6	DRV3_VDDO[1:0]	**VDDO Setting for CLK3.** 0: VDDO3 = 3.3 V (not for HSTL) 1: VDDO3 = 2.5 V (not for HSTL) 2: VDDO3 = 1.8 V (not for HSTL or LVPECL) 3: VDDO3 = 1.5 V (HSTL only)
5:4	DRV2_VDDO[1:0]	**VDDO Setting for CLK2.** 0: VDDO2 = 3.3 V (not for HSTL) 1: VDDO2 = 2.5 V (not for HSTL) 2: VDDO2 = 1.8 V (not for HSTL or LVPECL) 3: VDDO2 = 1.5 V (HSTL only)
3:2	DRV1_VDDO[1:0]	**VDDO Setting for CLK1.** 0: VDDO1 = 3.3 V (not for HSTL) 1: VDDO1 = 2.5 V (not for HSTL) 2: VDDO1 = 1.8 V (not for HSTL or LVPECL) 3: VDDO1 = 1.5 V (HSTL only)
1:0	DRV0_VDDO[1:0]	**VDDO Setting for CLK0.** 0: VDDO0 = 3.3 V (not for HSTL) 1: VDDO0 = 2.5 V (not for HSTL) 2: VDDO0 = 1.8 V (not for HSTL or LVPECL) 3: VDDO0 = 1.5 V (HSTL only)
Note: If the VDDOx voltage is below the minimum allowed voltage of the programmed voltage setting in Register 35, the output driver may not turn on.		

Register 36.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DRV0_INV[1:0]		DRV0_FMT[2:0]		
Type	R/W					R/W		

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	**Reserved.**
4:3	DRV0_INV[1:0]	**Invert Driver for CLK0 for CMOS/SSTL/HSTL Outputs.** 0: Both outputs are in phase 1: CLK0A inverted 2: CLK0B inverted 3: CLK0A/B inverted and in phase
2:0	DRV0_FMT[2:0]	**CLK0 Signal Format.** 0: Reserved 1: CLK0A = (CMOS/SSTL/HSTL), CLK0B = off 2: CLK0B = (CMOS/SSTL/HSTL), CLK0A = off 3: CLK0A,B = (CMOS/SSTL/HSTL) 4: LVPECL 5: Reserved 6: LVDS 7: HCSL

Register 37.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DRV1_INV[1:0]		DRV1_FMT[2:0]		
Type	R/W					R/W		

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	**Reserved.**
4:3	DRV1_INV[1:0]	**Invert Driver for CLK1 for CMOS/SSTL/HSTL Outputs.** 0: Both outputs are in phase 1: CLK1A invert 2: CLK1B invert 3: CLK1A/B invert and in phase
2:0	DRV1_FMT[2:0]	**CLK1 Signal Format.** 0: Reserved 1: CLK1A = (CMOS/SSTL/HSTL), CLK1B = off 2: CLK1B = (CMOS/SSTL/HSTL), CLK1A = off 3: CLK1A,B = (CMOS/SSTL/HSTL) 4: LVPECL 5: Reserved 6: LVDS 7: HCSL

Register 38.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DRV2_INV[1:0]		DRV2_FMT[2:0]		
Type	R/W					R/W		

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	**Reserved.**
4:3	DRV2_INV[1:0]	**Invert Driver for CLK2 for CMOS/SSTL/HSTL Outputs.** 0: Both outputs are in phase 1: CLK2A inverted 2: CLK2B inverted 3: CLK2A/B inverted and in phase
2:0	DRV2_FMT[2:0]	**CLK2 Signal Format.** 0: Reserved 1: CLK2A = (CMOS/SSTL/HSTL), CLK2B = off 2: CLK2B = (CMOS/SSTL/HSTL), CLK2A = off 3: CLK2A,B = (CMOS/SSTL/HSTL) 4: LVPECL 5: Reserved 6: LVDS 7: HCSL

Register 39.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DRV3_INV[1:0]		DRV3_FMT[2:0]		
Type	R/W					R/W		

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	**Reserved.**
4:3	DRV3_INV[1:0]	**Invert Driver for CLK3 for CMOS/SSTL/HSTL Outputs.** 0: Both outputs are in phase 1: CLK3A inverted 2: CLK3B inverted 3: CLK3A/B inverted and in phase
2:0	DRV3_FMT[2:0]	**CLK3 Signal Format.** 0: Reserved 1: CLK3A = (CMOS/SSTL/HSTL), CLK3B = off 2: CLK3B = (CMOS/SSTL/HSTL), CLK3A = off 3: CLK3A,B = (CMOS/SSTL/HSTL) 4: LVPECL 5: Reserved 6: LVDS 7: HCSL

Register 40.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DRV1_TRIM [2:0]			DRV0_TRIM [4:0]				
Type	R/W			R/W				

Reset value = xxxx xxxx

Bit	Name	Function
7:5	DRV1_TRIM [2:0]	**Trim Bits for CLK1 Driver.** Clockbuilder Desktop sets these values automatically. See AN411 for required manual settings information
4:3	DRV0_TRIM [4:0]	**Trim Bits for CLK0 Driver.** Clockbuilder Desktop sets these values automatically. See AN411 for required manual settings information

Register 41.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		DRV2_TRIM [4:0]					DRV1_TRIM [4:3]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	**Reserved.**
6:2	DRV2_TRIM [4:0]	**Trim Bits for CLK2 Driver.** Clockbuilder Desktop sets these values automatically. See AN411 for required manual settings information.
1:0	DRV1_TRIM [4:3]	**Trim Bits for CLK1 Driver.** Clockbuilder Desktop sets these values automatically. See AN411 for required settings information.

Register 42.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DRV3_TRIM [4:0]				
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	**Reserved.**
5	Reserved	Must write 1b to this bit.
4:0	DRV3_TRIM [4:0]	**Trim Bits for CLK3.** Clockbuilder Desktop sets these values automatically. See AN411 for required manual settings information.

Register 45.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FCAL_OVRD[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	FCAL_OVRD[7:0]	Bits 7:0 of the Override Frequency Calibration for the VCO.

Register 46.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FCAL_OVRD[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	FCAL_OVRD[15:8]	Bits 15:8 of the Override Frequency Calibration for the VCO

Register 47.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved						FCAL_OVRD[17:16]	
Type	R						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	Reserved	**Reserved.** Must write 000101b to these bits if the device is not factory programmed.
1:0	FCAL_OVRD[17:16]	Bits 17:16 of the Override Frequency Calibration for the VCO.

Register 48.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PFD_EXTFB	PLL_KPHI[6:0]						
Type	R/W	R/W						

Reset value = xxxx xxxx

Bit	Name	Function
7	PFD_EXTFB	Selects PFD feedback input from internal (see Register 30[7:5]) or external source. 0: Internal feedback path 1: External feedback path (zero delay mode)
6:0	PLL_KPHI[6:0]	Sets the charge pump current for the PFD. Clockbuilder Desktop sets these values automatically. See AN411 for manual setting.

Register 49.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FCAL_OVRD_EN	VCO_GAIN[2:0]			RSEL[1:0]		BWSEL[1:0]	
Type	R/W	R/W			R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7	FCAL_OVRD_EN	**FCAL Override Enable.** 0: Do not use FCAL value in registers 45,46,47 1: Use FCAL value in registers 45,46,47
6:4	VCO_GAIN[2:0]	**Sets the VCO Gain.** Clockbuilder Desktop sets these values automatically. See AN411 for manual setting.
3:2	RSEL[1:0]	**Loop Filter Resistor Select.** Clockbuilder Desktop sets these values automatically. See AN411 for manual setting.
1:0	BWSEL[1:0]	**Select the PLL Loopfilter.** Clockbuilder Desktop sets these values automatically. See AN411 for manual setting.

Register 50.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PLL_ENABLE[1:0]		MSCAL[5:0]					
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	PLL_ENABLE[1:0]	00: Disable PLL 11: Enable PLL It is expected that all Si5338 applications will need to have the PLL enabled; however, the PLL may be disabled when the Si5338 is set up in buffer mode.
5:0	MSCAL[5:0]	**MultiSynth Calibration Value for Optimum Performance.** Clockbuilder Desktop sets these values automatically. See AN411 for manual setting.

Register 51.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_HS	MS2_HS	MS1_HS	MS0_HS		MS_PEC[2:0]		
Type	R/W	R/W	R/W	R/W				

Reset value = xxxx x111

Bit	Name	Function
7	MS3_HS	**MultiSynth3 High Speed Mode.** When this bit is asserted, MultiSynth3 will only accept divide ratios of 4.0 or 6.0. Increment/decrement, SSC, and all phase functions are not available when this bit is set. 0: MultiSynth3 implements fractional divide ratios between 8 and 1023 1: MultiSynth3 can only implement 4.0 or 6.0 divide ratio.
6	MS2_HS	**MultiSynth2 High Speed Mode.** When this bit is asserted, MultiSynth2 will only accept divide ratios of 4.0 or 6.0. Increment/decrement, SSC, and all phase functions are not available when this bit is set. 0: MultiSynth2 implements fractional divide ratios between 8 and 1023. 1: MultiSynth2 can only implement 4.0 or 6.0 divide ratio.
5	MS1_HS	**MultiSynth1 High Speed Mode.** When this bit is asserted, MultiSynth1 will only accept divide ratios of 4.0 or 6.0. Increment/decrement, SSC, and all phase functions are not available when this bit is set. 0: MultiSynth1 implements fractional divide ratios between 8 and 1023. 1: MultiSynth1 can only implement 4.0 or 6.0 divide ratio.
4	MS0_HS	**MultiSynth0 High Speed Mode.** When this bit is asserted, MultiSynth0 will only accept divide ratios of 4.0 or 6.0. Increment/decrement, SSC, and all phase functions are not available when this bit is set. 0: MultiSynth0 implements fractional divide ratios between 8 and 1023. 1: MultiSynth0 can only implement 4.0 or 6.0 divide ratio.
3	Unused	**Unused.**
2:0	MS_PEC[2:0]	**MultiSynth Phase Error Correction.** All non-factory programmed devices must have 111b written to these bits.

Register 52.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS0_FIDCT[1:0]		MS0_FIDDIS	MS0_SSMODE[1:0]		MS0_PHIDCT[1:0]	
Type	R/W			R/W	R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	**Reserved.**
6:5	MS0_FIDCT[1:0]	**MultiSynth0 Frequency Increment/Decrement Control.** Bit 4 (disable) must be 0 before writing an increment or decrement to these bits. Only MS0 can have pin control of Frequency Increment/Decrement. 0: No frequency inc/dec on MS0 1: Enable pin control of frequency inc/dec 2: Frequency increment on MS0, self-clearing 3: Frequency decrement on MS0, self-clearing
4	MS0_FIDDIS	**MultiSynth0 Frequency Increment/Decrement Disable (see also Register 242[1]).** 0: Frequency inc/dec enabled on MS0 1: Frequency inc/dec disabled on MS0
3:2	MS0_SSMODE[1:0]	**MultiSynth0 Spread Spectrum Mode Select.** 0: No SSC on MS0 1: Center spread on MS0 2: Reserved 3: Down spread MS0
1:0	MS0_PHIDCT[1:0]	**MultiSynth0 Phase Increment/Decrement Control.** 0: No phase inc/dec on MS0 1: Enable pin control of phase inc/dec 2: Phase increment on MS0, self clearing 3: Phase decrement on MS0, self clearing

Register 53.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P1[7:0]	**MultiSynth0 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth0 divider.

Register 54.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
15:8	MS0_P1[15:8]	**MultiSynth0 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth0 divider.

Register 55.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P2[5:0]						MS0_P1[17:16]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	MS0_P2[5:0]	**MultiSynth0 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth0 Divider.
1:0	MS0_P1[17:16]	MultiSynth0 Parameter 1. This 18-bit number is an encoded representation of the integer part of the MultiSynth0 divider.

Register 56.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P2[13:6]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P2[13:6]	**MultiSynth0 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth0 Divider.

Register 57.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P2[21:14]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P2[21:14]	**MultiSynth0 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth0 Divider.

Register 58.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P2[29:22]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P2[29:22]	**MultiSynth0 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth0 Divider.

Register 59.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P3[7:0]	**MultiSynth0 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth0 divider.

Register 60.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P3[15:8]	**MultiSynth0 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth0 divider.

Register 61.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P3[23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P3[23:16]	**MultiSynth0 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth0 divider.

Register 62.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			MS0_P3[29:24]					
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	**Reserved.**
5:0	MS0_P3[29:24]	**MultiSynth0 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth0 divider.

Register 63.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS1_FIDCT[1:0]		MS1_FIDDIS	MS1_SSMODE[1:0]		MS1_PHIDCT[1:0]	
Type	R/W			R/W	R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	**Reserved.**
6:5	MS1_FIDCT[1:0]	**MultiSynth1 Frequency Increment/Decrement Control.** Bit 4 (disable) must be 0 before writing an increment or decrement to these bits. 0: No frequency inc/dec on MS1 1: Reserved 2: Frequency increment on MS1, self-clearing 3: Frequency decrement on MS1, self-clearing
4	MS1_FIDDIS	**MultiSynth1 Frequency Increment/Decrement Disable.** See also Register 242[1]. 0: Frequency inc/dec enabled on MS1 1: Frequency inc/dec disabled on MS1
3:2	MS1_SSMODE[1:0]	**MultiSynth1 Spread Spectrum Mode Select.** 0: No SSC on MS1 1: Center spread on MS1 2: Reserved 3: Downspread MS1
1:0	MS1_PHIDCT[1:0]	**MultiSynth1 Phase Increment/Decrement Control.** Writing a 10 or 11 will self clear back to 0. 0: No phase inc/dec on MS1 1: Enable pin control of phase inc/dec 2: Phase increment on MS1, self clearing 3: Phase decrement on MS1, self clearing

Register 64.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P1[7:0]	**MultiSynth1 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth1 divider.

Register 65.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P1[15:8]	**MultiSynth1 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth1 divider.

Register 66.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P2[5:0]						MS1_P1[17:16]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	MS1_P2[5:0]	**MultiSynth1 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth1 Divider.
1:0	MS1_P1[17:16]	**MultiSynth1 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth1 divider.

Register 67.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P2[13:6]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P2[13:6]	**MultiSynth1 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth1 Divider.

Register 68.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P2[21:14]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P2[21:14]	**MultiSynth1 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth1 Divider.

Register 69.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P2[29:22]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P2[29:22]	**MultiSynth1 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth1 Divider.

Register 70.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P3[7:0]	**MultiSynth1 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth1 Divider.

Register 71.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P3[15:8]	**MultiSynth1 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth1 Divider.

Register 72.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P3[23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P3[23:16]	**MultiSynth1 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth1 Divider.

Register 73.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			MS1_P3[29:24]					
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	**Reserved**
5:0	MS1_P3[29:24]	**MultiSynth1 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth1 Divider.

Register 74.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS2_FIDCT[1:0]		MS2_FIDDIS	MS2_SSMODE[1:0]		MS2_PHIDCT[1:0]	
Type	R/W			R/W	R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	**Reserved.**
6:5	MS2_FIDCT[1:0]	**MultiSynth2 Frequency Increment/Decrement Control.** Bit 4 (disable) must be 0 before writing an increment or decrement to these bits. 0: No frequency inc/dec on MS2 1: Reserved 2: Frequency increment on MS2, self-clearing 3: Frequency decrement on MS2, self-clearing
4	MS2_FIDDIS	**MultiSynth2 Frequency Increment/Decrement Disable (see also Register 242[1]).** 0: Frequency inc/dec enabled on MS2 1: Frequency inc/dec disabled on MS2
3:2	MS2_SSMODE[1:0]	**MultiSynth2 Spread Spectrum Mode Select.** 0: No SSC on MS2 1: Center spread on MS2 2: Reserved 3: Down spread MS2
1:0	MS2_PHIDCT[1:0]	**MultiSynth2 Phase Increment/Decrement Control.** 0: No phase inc/dec on MS2 1: Enable pin control of phase inc/dec 2: Phase increment on MS2, self clearing 3: Phase decrement on MS2, self clearing

Register 75.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P1[7:0]	**MultiSynth2 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth2 divider.

Register 76.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P1[15:8]	**MultiSynth2 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth2 divider.

Register 77.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P2[5:0]						MS2_P1[17:16]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	MS2_P2[5:0]	**MultiSynth2 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth2 Divider.
1:0	MS2_P1[17:16]	**MultiSynth2 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth2 divider.

Register 78.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P2[13:6]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P2[13:6]	**MultiSynth2 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth2 Divider.

Register 79.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P2[21:14]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P2[21:14]	**MultiSynth2 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth2 Divider.

Register 80.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P2[29:22]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P2[29:22]	**MultiSynth2 Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth2 Divider.

Register 81.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
	MS2_P3[7:0]	**MultiSynth2 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth2 Divider.

Register 82.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P3[15:8]	**MultiSynth2 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth2 Divider.

Register 83.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P3[23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P3[23:16]	**MultiSynth2 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth2 Divider.

Register 84.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			MS2_P3[29:24]					
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	**Reserved.**
	MS2_P3[29:24]	**MultiSynth2 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth2 Divider.

Register 85.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS3_FIDCT[1:0]		MS3_FIDDIS	MS3_SSMODE[1:0]		MS3_PHIDCT[1:0]	
Type	R/W			R/W	R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	**Reserved.**
6:5	MS3_FIDCT[1:0]	**MultiSynth3 Frequency Increment/Decrement Control.** Bit 4 (disable) must be 3 before writing an increment or decrement to these bits. 0: No frequency inc/dec on MS3 1: Reserved 2: Frequency increment on MS3, self-clearing 3: Frequency decrement on MS3, self-clearing
4	MS3_FIDDIS	**MultiSynth3 Frequency Increment/Decrement Disable (see also Register 242[1]).** 0: Frequency inc/dec enabled on MS3 1: Frequency inc/dec disabled on MS3
3:2	MS3_SSMODE[1:0]	**MultiSynth3 Spread Spectrum Mode Select.** 0: No SSC on MS3 1: Center spread on MS3 2: Reserved 3: Down spread MS3
1:0	MS3_PHIDCT[1:0]	**MultiSynth3 Phase Increment/Decrement Control.** 0: No phase inc/dec on MS3 1: Enable pin control of phase inc/dec 2: Phase increment on MS3 3: Phase decrement on MS3

Register 86.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_P1[7:0]	**MultiSynth3 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth3 divider.

Register 87.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_P1[15:8]	**MultiSynth3 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth3 divider

Register 88.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P2[5:0]						MS3_P1[17:16]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	MS3_P2[5:0]	**MultiSynth3 Parameter 2.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth3 Divider.
1:0	MS3_P1[17:16]	**MultiSynth3 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth3 divider.

Register 89.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P2[13:6]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_P2[13:6]	**MultiSynth3 Parameter 2.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth3 Divider.

Register 90.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P2[21:14]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_P2[21:14]	**MultiSynth3 Parameter 2.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth3 Divider.

Register 91.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P2[29:22]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_P2[29:22]	**MultiSynth3 Parameter 2.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth3 Divider.

Register 92.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_P3[7:0]	**MultiSynth3 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth3 Divider.

Register 93.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_P3[15:8]	**MultiSynth3 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth3 Divider

Register 94.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P3[23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_P3[23:16]	**MultiSynth3 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth3 Divider

Register 95.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			MS3_P3[29:24]					
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	**Reserved.**
5:0	MS3_P3[29:24]	**MultiSynth3 Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth3 Divider.

Register 97.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P1[7:0]	**Feedback MultiSynthN Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth Feedback divider.

Register 98.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P1[15:8]	**Feedback MultiSynthN Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth Feedback divider.

Register 99.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P2[5:0]						MSN_P1[17:16]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	MSN_P2[5:0]	**Feedback MultiSynthN Parameter 2.** This 18-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth Feedback divider.
1:0	MSN_P1[17:16]	**Feedback MultiSynthN Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth Feedback divider.

Register 100.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P2[13:6]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P2[13:6]	**Feedback MultiSynthN Parameter 2.** This 18-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth Feedback divider.

Register 101.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P2[21:14]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P2[21:14]	**Feedback MultiSynthN Parameter 2.** This 18-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth Feedback divider.

Register 102.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P2[29:22]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P2[29:22]	**Feedback MultiSynthN Parameter 2.** This 18-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth Feedback divider.

Register 103.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P3[7:0]	**Feedback MultiSynthN Parameter 3.** This 18-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth Feedback divider.

Register 104.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P3[15:8]	**Feedback MultiSynthN Parameter 3.** This 18-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth Feedback divider

Register 105.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P3[23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P3[23:16]	**Feedback MultiSynthN Parameter 3.** This 18-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth Feedback divider.

Register 106.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NOTERM_FB		MSN_P3[29:24]					
Type	R/W		R/W					

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	**Reserved.** Must write 1b to this bit.
6	Reserved	**Reserved.**
5:0	MSN_P3[29:24]	**Feedback MultiSynthN Parameter 3.** This 18-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth Feedback divider.

Register 107.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_PHOFF[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_PHOFF[7:0]	**MultiSynth0 Initial Phase Offset.** MultiSynth0_PHOFF[14:0] is a 2s complement number. The initial phase offset is MultiSynth0_PHOFF[14:0]*Tvco/128 where Tvco is the period of the VCO.

Register 108.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS0_PHOFF[14:8]						
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	**Reserved.**
6:0	MS0_PHOFF[14:8]	**MultiSynth0 Initial Phase Offset.** MultiSynth0_PHOFF[14:0] is a 2s complement number. The initial phase offset is MultiSynth0_PHOFF[14:0]*Tvco/128 where Tvco is the period of the VCO.

Register 109.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_PHSTEP[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_PHSTEP[7:0]	**MultiSynth0 Phase Step Size.** The phase step size is MultiSynth0_PHSTEP[13:0]*Tvco/128 where Tvco is the period of the VCO. Either the phase inc/dec pins (if available) or register 52[1:0] will control the stepping of phase. A phase increment will delay the clock edge.

Register 110.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK0_DISST[1:0]		MS0_PHSTEP[13:8]					
Type	R/W		R/W					

Reset value = xxxx xxxx

Bit	Name	Function
7:6	CLK0_DISST[1:0	**CLK0 Output Driver State When Disabled.** 00: High impedance 01: Logic low 10: Logic high 11: Always on even if disabled
5:0	MS0_PHSTEP[13:8]	**MS0 Phase Step Size.** The phase step size is MS0_PHSTEP[13:0]*Tvco/128 where Tvco is the period of the VCO. Either the phase inc/dec pins (if available) or register 52[1:0] will control the stepping of phase. A phase increment will delay the clock edge.

Register 111.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_PHOFF[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_PHOFF[7:0]	**MultiSynth1 Initial Phase Offset.** MultiSynth1_PHOFF[14:0] is a 2s complement number. The initial phase offset is MultiSynth1_PHOFF[14:0]*Tvco/128 where Tvco is the period of the VCO.

Register 112.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS1_PHOFF[14:8]						
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	**Reserved**
6:0	MS1_PHOFF[14:8]	**MultiSynth1 Initial Phase Offset.** MultiSynth1_PHOFF[14:0] is a 2s complement number. The initial phase offset is MultiSynth1_PHOFF[14:0] x Tvco/128 where Tvco is the period of the VCO.

Register 113.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_PHSTEP[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_PHSTEP[7:0]	**MultiSynth1 Phase Step Size.** The phase step size is MultiSynth1_PHSTEP[13:0] x Tvco/128 where Tvco is the period of the VCO. Either the phase inc/dec pins (if available) or register 63[1:0] will control the stepping of phase. A phase increment will delay the clock edge.

Register 114.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK1_DISST[1:0]		MS1_PHSTEP[13:8]					
Type	R/W		R/W					

Reset value = xxxx xxxx

Bit	Name	Function
7:6	CLK1_DISST[1:0]	**MultiSynth1 Output Driver State When Disabled.** 00: High impedance 01: Logic low 10: Logic high 11: Always on even if disabled
5:0	MS1_PHSTEP[13:8]	**MultiSynth1 Phase Step Size.** The phase step size is MS1_PHSTEP[13:0]*Tvco/128 where Tvco is the period of the VCO. Either the phase inc/dec pins (if available) or register 63[1:0] will control the stepping of phase. A phase increment will delay the clock edge.

Register 115.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_PHOFF[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_PHOFF[7:0]	**MultiSynth2 Initial Phase Offset.** MultiSynth2_PHOFF[14:0] is a 2s complement number. The initial phase offset is MultiSynth2_PHOFF[14:0] x Tvco/128 where Tvco is the period of the VCO.

Register 116.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS2_PHOFF[14:8]						
Type	R/W	R/W						

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	**Reserved.** Must write 1b to this bit.
6:0	MS2_PHOFF[14:8]	**MultiSynth2 Initial Phase Offset.** MultiSynth2_PHOFF[14:0] is a 2s complement number. The initial phase offset is MultiSynth2_PHOFF[14:0] x Tvco/128 where Tvco is the period of the VCO.

Register 117.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_PHSTEP[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_PHSTEP[7:0]	**MultiSynth2 Phase Step Size.** The phase step size is MultiSynth2_PHSTEP[13:0] x Tvco/128 where Tvco is the period of the VCO. Either the phase inc/dec pins (if available) or register 74[1:0] will control the stepping of phase. A phase increment will delay the clock edge.

Register 118.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK2_DISST[1:0]		MS2_PHSTEP[13:8]					
Type	R/W		R/W					

Reset value = xxxx xxxx

Bit	Name	Function
7:6	CLK2_DISST[1:0]	**MultiSynth2 Output Driver State When Disabled.** 00: High impedance 01: Logic low 10: Logic high 11: Always on even if disabled
5:0	MS2_PHSTEP[13:8]	**MultiSynth2 Phase Step Size.** The phase step size is MS2_PHSTEP[13:0]*Tvco/128 where Tvco is the period of the VCO. Either the phase inc/dec pins (if available) or register 74[1:0] will control the stepping of phase. A phase increment will delay the clock edge.

Register 119.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_PHOFF[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_PHOFF[7:0]	**MultiSynth3 Initial Phase Offset.** MultiSynth3_PHOFF[14:0] is a 2s complement number. The initial phase offset is MultiSynth3_PHOFF[14:0] x Tvco/128 where Tvco is the period of the VCO.

Register 120.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS3_PHOFF[14:8]						
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7	Unused	**Unused.**
6:0	MS3_PHOFF[14:8]	**MultiSynth3 Initial Phase Offset.** MultiSynth3_PHOFF[14:0] is a 2s complement number. The initial phase offset is MultiSynth3_PHOFF[14:0] x Tvco/128 where Tvco is the period of the VCO.

Register 121.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_PHSTEP[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_PHSTEP[7:0]	**MultiSynth3 Phase Step Size.** The phase step size is MultiSynth3_PHSTEP[13:0] x Tvco/128 where Tvco is the period of the VCO. Either the phase inc/dec pins (if available) or register 85[1:0] will control the stepping of phase. A phase increment will delay the clock edge.

Register 122.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK3_DISST[1:0]		MS3_PHSTEP[13:8]					
Type	R/W		R/W					

Reset value = xxxx xxxx

Bit	Name	Function
7:6	CLK3_DISST[1:0]	**MultiSynth3 Output Driver State When Disabled.** 00: High impedance 01: Logic low 10: Logic high 11: Always on even if disabled
5:0	MS3_PHSTEP[13:8]	**MultiSynth3 Phase Step Size.** The phase step size is MultiSynth3_PHSTEP[13:0] x Tvco/128 where Tvco is the period of the VCO. Either the phase inc/dec pins (if available) or register 85[1:0] will control the stepping of phase. A phase increment will delay the clock edge.

Register 123.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP1[7:0]	**MultiSynth0 Frequency Increment/Decrement Parameter 1.**

Register 124.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP1 [15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP1 [15:8]	**MultiSynth0 Frequency Increment/Decrement Parameter 1.**

Register 125.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP1 [23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP1 [23:16]	**MultiSynth0 Frequency Increment/Decrement Parameter 1.**

Register 126.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP1 [31:24]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP1 [31:24]	**MultiSynth0 Frequency Increment/Decrement Parameter 1.**

Register 127.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP1 [39:32]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP1 [39:32]	**MultiSynth0 Frequency Increment/Decrement Parameter 1.**

Register 128.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP1 [47:40]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP1 [47:40]	**MultiSynth0 Frequency Increment/Decrement Parameter 1.**

Register 129.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS0_FIDP1 [51:48]			
Type	R/W							

Reset value = 001x xxxx

Bit	Name	Function
7:4	Reserved	Reserved.
3:0	MS0_FIDP1[51:48]	**MultiSynth0 Frequency Increment/Decrement Parameter 1.**

Register 130.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS0_FIDP2 [51:48]			
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:4	Reserved	Reserved
3:0	MS0_FIDP2[51:48]	**MultiSynth0 Frequency Increment/Decrement Parameter 2.**

Register 131.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP2 [47:40]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP2 [47:40]	**MultiSynth0 Frequency Increment/Decrement Parameter 2.**

Register 132.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP2 [39:32]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP2 [39:32]	**MultiSynth0 Frequency Increment/Decrement Parameter 2.**

Register 133.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP2 [31:24]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP2 [31:24]	**MultiSynth0 Frequency Increment/Decrement Parameter 2.**

Register 134.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP2 [23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP2 [23:16]	**MultiSynth0 Frequency Increment/Decrement Parameter 2.**

Register 135.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP2 [15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP2 [15:8]	**MultiSynth0 Frequency Increment/Decrement Parameter 2.**

Register 136.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP2 [7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP2 [7:0]	**MultiSynth0 Frequency Increment/Decrement Parameter 2.**

Register 137.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP3 [7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP3 [7:0]	**MultiSynth0 Frequency Increment/Decrement Parameter 3.**

Register 138.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP3 [15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP3 [15:8]	**MultiSynth0 Frequency Increment/Decrement Parameter 3.**

Register 139.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP3 [23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP3 [23:16]	**MultiSynth0 Frequency Increment/Decrement Parameter 3.**

Register 140.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP3 [31:24]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP3 [31:24]	**MultiSynth0 Frequency Increment/Decrement Parameter 3.**

Register 141.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP3 [39:32]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP3 [39:32]	**MultiSynth0 Frequency Increment/Decrement Parameter 3.**

Register 142.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP3 [47:40]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP3 [47:40]	**MultiSynth0 Frequency Increment/Decrement Parameter 3.**

Register 143.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_FIDP3 [55:48]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_FIDP3 [55:48]	**MultiSynth0 Frequency Increment/Decrement Parameter 3.**

Register 144.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_ALL	MS0_FIDP3[62:56]						
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7	MS0_ALL	**Use MultiSynth0 for All Outputs.** If set, the MultiSynth0 output is routed to the mux at the input of each R divider. Unused MultiSynths should be powered down to save power.
6:0	MS0_FIDP3[62:56]	**MultiSynth0 Frequency Increment/Decrement Parameter 3.**

Register 152.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP1[7:0]	**MultiSynth1 Frequency Increment/Decrement Parameter 1.**

Register 153.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP1[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP1[15:8]	**MultiSynth1 Frequency Increment/Decrement Parameter 1.**

Register 154.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP1[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP1[23:16]	**MultiSynth1 Frequency Increment/Decrement Parameter 1.**

Register 155.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP1[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP1[31:24]	**MultiSynth1 Frequency Increment/Decrement Parameter 1.**

Register 156.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP1[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP1[39:32]	**MultiSynth1 Frequency Increment/Decrement Parameter 1.**

Register 157.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP1[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP1[47:40]	**MultiSynth1 Frequency Increment/Decrement Parameter 1.**

Register 158.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS1_FIDP1[51:48]			
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	Reserved.
3:0	MS1_FIDP1[51:48]	**MultiSynth1 Frequency Increment/Decrement Parameter 1.**

Register 159.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS1_FIDP2[51:48]			
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	Reserved
3:0	MS1_FIDP2[51:48]	**MultiSynth1 Frequency Increment/Decrement Parameter 2.**

Register 160.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP2[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP2[47:40]	**MultiSynth1 Frequency Increment/Decrement Parameter 2.**

Register 161.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP2[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP2[39:32]	**MultiSynth1 Frequency Increment/Decrement Parameter 2.**

Register 162.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP2[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP2[31:24]	**MultiSynth1 Frequency Increment/Decrement Parameter 2.**

Register 163.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP2[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP2[23:16]	**MultiSynth1 Frequency Increment/Decrement Parameter 2.**

Register 164.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP2[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP2[15:8]	**MultiSynth1 Frequency Increment/Decrement Parameter 2.**

Register 165.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP2[7:0]	**MultiSynth1 Frequency Increment/Decrement Parameter 2.**

Register 166.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP3[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP3[7:0]	**MultiSynth1 Frequency Increment/Decrement Parameter 3.**

Register 167.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP3[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP3[15:8]	**MultiSynth1 Frequency Increment/Decrement Parameter 3.**

Register 168.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP3[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP3[23:16]	**MultiSynth1 Frequency Increment/Decrement Parameter 3.**

Register 169.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP3[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP3[31:24]	**MultiSynth1 Frequency Increment/Decrement Parameter 3.**

Register 170.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP3[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP3[39:32]	**MultiSynth1 Frequency Increment/Decrement Parameter 3.**

Register 171.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP3[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP3[47:40]	**MultiSynth1 Frequency Increment/Decrement Parameter 3.**

Register 172.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_FIDP3[55:48]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_FIDP3[55:48]	**MultiSynth1 Frequency Increment/Decrement Parameter 3.**

Register 173.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS1_FIDP3[62:56]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	Unused.
6:0	MS1_FIDP3[62:56]	**MultiSynth1 Frequency Increment/Decrement Parameter 3.**

Register 174.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP1[7:0]	**MultiSynth2 Frequency Increment/Decrement Parameter 1.**

Register 175.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP1[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP1[15:8]	**MultiSynth2 Frequency Increment/Decrement Parameter 1.**

Register 176.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP1[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP1[23:16]	**MultiSynth2 Frequency Increment/Decrement Parameter 1.**

Register 177.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP1[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP1[31:24]	**MultiSynth2 Frequency Increment/Decrement Parameter 1.**

Register 178.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP1[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP1[39:32]	**MultiSynth2 Frequency Increment/Decrement Parameter 1.**

Register 179.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP1[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP1[47:40]	**MultiSynth2 Frequency Increment/Decrement Parameter 1.**

Register 180.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS2_FIDP1[51:48]			
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:4	Unused	Unused.
3:0	MS2_FIDP1[51:48]	**MultiSynth2 Frequency Increment/Decrement Parameter 1.**

Register 181.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS2_FIDP2[51:48]			
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	Reserved.
3:0	MS2_FIDP2[51:48]	**MultiSynth2 Frequency Increment/Decrement Parameter 2.**

Register 182.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP2[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP2[47:40]	**MultiSynth2 Frequency Increment/Decrement Parameter 2.**

Register 183.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP2[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP2[39:32]	**MultiSynth2 Frequency Increment/Decrement Parameter 2.**

Register 184.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP2[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP2[31:24]	**MultiSynth2 Frequency Increment/Decrement Parameter 2.**

Register 185.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP2[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP2[23:16]	**MultiSynth2 Frequency Increment/Decrement Parameter 2.**

Register 186.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP2[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP2[15:8]	**MultiSynth2 Frequency Increment/Decrement Parameter 2.**

Register 187.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP2[7:0]	**MultiSynth2 Frequency Increment/Decrement Parameter 2.**

Register 188.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP3[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP3[7:0]	**MultiSynth2 Frequency Increment/Decrement Parameter 3.**

Register 189.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP3[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP3[15:8]	**MultiSynth2 Frequency Increment/Decrement Parameter 3.**

Register 190.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP3[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP3[23:16]	**MultiSynth2 Frequency Increment/Decrement Parameter 3.**

Register 191.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP3[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP3[31:24]	**MultiSynth2 Frequency Increment/Decrement Parameter 3.**

Register 192.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP3[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP3[39:32]	**MultiSynth2 Frequency Increment/Decrement Parameter 3.**

Register 193.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP3[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP3[47:40]	**MultiSynth2 Frequency Increment/Decrement Parameter 3.**

Register 194.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_FIDP3[55:48]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_FIDP3[55:48]	**MultiSynth2 Frequency Increment/Decrement Parameter 3.**

Register 195.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS2_FIDP3[62:56]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	Unused.
6:0	MS2_FIDP3[62:56]	**MultiSynth2 Frequency Increment/Decrement Parameter 3.**

Register 196.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP1[7:0]	**MultiSynth3 Frequency Increment/Decrement Parameter 1.**

Register 197.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP1[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP1[15:8]	**MultiSynth3 Frequency Increment/Decrement Parameter 1.**

Register 198.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP1[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP1[23:16]	**MultiSynth3 Frequency Increment/Decrement Parameter 1.**

Register 199.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP1[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP1[31:24]	**MultiSynth3 Frequency Increment/Decrement Parameter 1.**

Register 200.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP1[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP1[39:32]	**MultiSynth3 Frequency Increment/Decrement Parameter 1.**

Register 201.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP1[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP1[47:40]	**MultiSynth3 Frequency Increment/Decrement Parameter 1.**

Register 202.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS3_FIDP1 [51:48]			
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:4	Unused	Unused.
3:0	MS3_FIDP1 [51:48]	**MultiSynth3 Frequency Increment/Decrement Parameter 1.**

Register 203.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS3_FIDP2[51:48]			
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	Reserved
3:0	MS3_FIDP2[51:48]	**MultiSynth3 Frequency Increment/Decrement Parameter 2.**

Register 204.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP2[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP2[47:40]	**MultiSynth3 Frequency Increment/Decrement Parameter 2.**

Register 205.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP2[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP2[39:32]	**MultiSynth3 Frequency Increment/Decrement Parameter 2.**

Register 206.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP2[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP2[31:24]	**MultiSynth3 Frequency Increment/Decrement Parameter 2.**

Register 207.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP2[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP2[23:16]	**MultiSynth3 Frequency Increment/Decrement Parameter 2.**

Register 208.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP2[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP2[15:8]	**MultiSynth3 Frequency Increment/Decrement Parameter 2.**

Register 209.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP2[7:0]	**MultiSynth3 Frequency Increment/Decrement Parameter 2.**

Register 210.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP3[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP3[7:0]	**MultiSynth3 Frequency Increment/Decrement Parameter 3.**

Register 211.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP3[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP3[15:8]	**MultiSynth3 Frequency Increment/Decrement Parameter 3.**

Register 212.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP3[23:16]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP3[23:16]	**MultiSynth3 Frequency Increment/Decrement Parameter 3.**

Register 213.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP3[31:24]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP3[31:24]	**MultiSynth3 Frequency Increment/Decrement Parameter 3.**

Register 214.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP3[39:32]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP3[39:32]	**MultiSynth3 Frequency Increment/Decrement Parameter 3.**

Register 215.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP3[47:40]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP3[47:40]	**MultiSynth3 Frequency Increment/Decrement Parameter 3.**

Register 216.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_FIDP3[55:48]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_FIDP3[55:48]	**MultiSynth3 Frequency Increment/Decrement Parameter 3.**

Register 217.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS3_FIDP3[62:56]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	Unused
6:0	MS3_FIDP3[62:56]	**MultiSynth3 Frequency Increment/Decrement Parameter 3.**

Register 218.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				PLL_LOL	LOS_FDBK	LOS_CLKIN		SYS_CAL
Type				R	R	R		R

Reset value = 0000 0000

Bit	Name	Function
7:5	Reserved	**Reserved**
4	PLL_LOL	**PLL Loss of Lock (LOL).** Asserts when the two PFD inputs have a frequency difference > 1000 ppm. This bit is held high during a POR_reset until the PLL has locked. This bit will not chatter while the PLL is locking. PLL_LOL does not assert when the input from IN1,IN2 or IN3 is lost. When PLL_LOL asserts, the part will automatically try to re-acquire to the input clock. See Register 241[7].
3	LOS_FDBK	**Loss of Signal on Feedback Clock from IN5,6 or IN4.**
2	LOS_CLKIN	**Loss of Signal on Input Clock from IN1,2 or IN3.**
1	Reserved	**Reserved**
0	SYS_CAL	**Device Calibration in Process.**

Register 230.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				OEB_ALL	OEB_3	OEB_2	OEB_1	OEB_0
Type				R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7:5	Unused	**Unused.**
4	OEB_ALL	**Disable All Clock Outputs.** 0: All output clocks are disabled 1: Output clocks are not disabled
3	OEB_3	**CLK3 Disable.** 0: CLK1 output is disabled 1: CLK1 output is not disabled
2	OEB_2	**CLK2 Disable.** 0: CLK2 output is disabled 1: CLK2 output is not disabled
1	OEB_1	**CLK1 Disable.** 0: CLK2 output is disabled 1: CLK2 output is not disabled
0	OEB_0	**CLK0 Disable.** 0: CLK0 output is disabled 1: CLK0 output is not disabled

Register 235.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FCAL[7:0]							
Type	R							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	FCAL[7:0]	**Bits 7:0 of the Frequency Calibration for the VCO.**

Register 236.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FCAL[15:8]							
Type	R							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	FCAL[15:8]	**Bits 15:8 of the Frequency Calibration for the VCO.**

Register 237.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved						FCAL[17:16]	
Type	R						R	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	Reserved	**Reserved.**
1:0	FCAL[17:16]	**Bits 17:16 of the Frequency Calibration for the VCO.**

Register 241.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIS_LOL	Reserved. Write to 0x65.						
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7	DIS_LOL	When asserted, the PLL_LOL status in register 218 is prevented from asserting.
6:0	Reserved	On a non-factory-programmed device this register must be set to 0x65. On a factory programmed device, this register must stay 0x65.

Register 242.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							DCLK_DIS	
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:2	Reserved	**Reserved.**
1	DCLK_DIS	**Disable Clock to INC/DEC State Machine.** When true, the frequency inc/dec logic is disabled, which saves about 2 mA of current. See also Registers 52[4], 63[4], 74[4], 85[4].
0	Reserved	**Reserved.**

Register 246.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							SOFT_RESET	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	Reserved	**Reserved.**
1	SOFT_RESET	**Soft Reset.** This reset will disable all clock outputs, then re-acquire the PLL to the input clock and the enable all the clock outputs. Retains device configuration stored in RAM. Do not use read-modify-write procedure to perform soft reset. Instead, write reg246=0x02, regardless of the current value of this bit. Reading this bit after a soft reset will return a 1.
0	Reserved	**Reserved.**

Register 247.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				PLL_LOL_STK	LOS_FDBK_STK	LOS_CLKIN_STK		SYS_CAL_STK
Type				R/W	R/W	R/W		R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	**Reserved.**
4	PLL_LOL_STK	**PLL Loss of Lock Sticky Bit.** Sticky version of PLL_LOL. See also Registers 6 and 218. Only a soft or POR reset or writing a “0” to this bit will clear it.
3	LOS_FDBK_STK	**Feedback Clock Loss of Signal Sticky Bit.** Sticky version of LOS_FDBK. See also Registers 6 and 218. Only a soft or POR reset or writing a “0” to this bit will clear it.
2	LOS_CLKIN_STK	**Input Clock Loss of Signal Sticky Bit.** Sticky version of LOS_CLKIN_STK. See also Registers 6 and 218. Only a soft or POR reset or writing a “0” to this bit will clear it.
1	Reserved	**Reserved.**
0	SYS_CAL_STK	**System Calibration in Process Sticky Bit.** Sticky version of SYS_CAL. See also Registers 6 and 218. Only a soft or POR reset or writing a “0” to this bit will clear it.

Register 255.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								PAGE_SEL
Type								R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:1	Unused	**Unused.**
0	PAGE_SEL	Set to 0 to access registers 0–254, set to 1 to access register 256 to 347.

Register 287.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_SSUPP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS0_SSUPP2[7:0]	**MultiSynth0 Spread Spectrum Up Parameter 2.**

Register 288.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS0_SSUPP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MS0_SSUPP2[14:8]	**MultiSynth0 Spread Spectrum Up Parameter 2.**

Register 289.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_SSUPP3[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS0_SSUPP3[7:0]	**MultiSynth0 Spread Spectrum Up Parameter 3.**

Register 290.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS0_SSUPP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	Unused
6:0	MS0_SSUPP3[14:8]	**MultiSynth0 Spread Spectrum Up Parameter 3.**

Register 291.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_SSUPP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS0_SSUPP1[7:0]	**MultiSynth0 Spread Spectrum Up Parameter 1.**

Register 292.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_SSUDP1[3:0]				MS0_SSUPP1[11:8]			
Type	R/W				R/W			

Reset value = 0011 0001

Bit	Name	Function
7:4	MS0_SSUDP1[3:0]	**MultiSynth0 Spread Spectrum Up/Down Parameter 1.**
3:0	MS0_SSUPP1[11:8]	**MultiSynth0 Spread Spectrum Up Parameter 1.**

Register 293.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_SSUDP1[11:4]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	MS0_SSUDP1[11:4]	**MultiSynth0 Spread Spectrum Up Parameter 1.**

Register 294.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_SSDNP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS0_SSDNP2[7:0]	**MultiSynth0 Spread Spectrum Down Parameter 2.**

Register 295.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS0_SSDNP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	Unused.
6:0	MS0_SSDNP2[14:8]	**MultiSynth0 Spread Spectrum Down Parameter 2.**

Register 296.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_SSDNP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MS0_SSDNP3[7:0]	**MultiSynth0 Spread Spectrum Down Parameter 3.**

Register 297.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS0_SSDNP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	Unused.
6:0	MS0_SSDNP3[14:8]	**MultiSynth0 Spread Spectrum Down Parameter 3.**

Register 298.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_SSDNP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS0_SSDNP1[7:0]	**MultiSynth0 Spread Spectrum Down Parameter 1.**

Register 299.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS0_SSDNP1[11:8]			
Type	R/W				R/W			

Reset value = 0011 0001

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:0	MS0_SSDNP1[11:8]	**MultiSynth0 Spread Spectrum Down Parameter 1.**

Register 303.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_SSUPP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_SSUPP2[7:0]	**MultiSynth1 Spread Spectrum Up Parameter 2.**

Register 304.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS1_SSUPP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MS1_SSUPP2[14:8]	**MultiSynth1 Spread Spectrum Up Parameter 2.**

Register 305.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_SSUPP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MS1_SSUPP3[7:0]	**MultiSynth1 Spread Spectrum Up Parameter 3.**

Register 306.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS1_SSUPP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MS1_SSUPP3[14:8]	**MultiSynth1 Spread Spectrum Up Parameter 3.**

Register 307.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_SSUPP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_SSUPP1[7:0]	**MultiSynth1 Spread Spectrum Up Parameter 1.**

Register 308.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_SSUDP1[3:0]				MS1_SSUPP1[11:8]			
Type	R/W				R/W			

Reset value = 1001 0000

Bit	Name	Function
7:4	MS1_SSUDP1[3:0]	**MultiSynth1 Spread Spectrum Up/Down Parameter 1.**
3:0	MS1_SSUPP1[11:8]	**MultiSynth1 Spread Spectrum Up Parameter 1.**

Register 309.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_SSUDP1[11:4]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	MS1_SSUDP1[11:4]	**MultiSynth1 Spread Spectrum Up Parameter 1.**

Register 310.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_SSDNP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_SSDNP2[7:0]	**MultiSynth1 Spread Spectrum Down Parameter 2.**

Register 311.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS1_SSDNP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MS1_SSDNP2[14:8]	**MultiSynth1 Spread Spectrum Down Parameter 2.**

Register 312.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_SSDNP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MS1_SSDNP3[7:0]	**MultiSynth1 Spread Spectrum Down Parameter 3.**

Register 313.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS1_SSDNP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MS1_SSDNP3[14:8]	**MultiSynth1 Spread Spectrum Down Parameter 3.**

Register 314.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_SSDNP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS1_SSDNP1[7:0]	**MultiSynth1 Spread Spectrum Down Parameter 1.**

Register 315.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS1_SSDNP1[11:8]			
Type	R/W				R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:0	MS1_SSDNP1[11:8]	**MultiSynth1 Spread Spectrum Down Parameter 1.**

Register 319.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_SSUPP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_SSUPP2[7:0]	**MultiSynth2 Spread Spectrum Up Parameter 2.**

Register 320.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS2_SSUPP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MS2_SSUPP2[14:8]	**MultiSynth2 Spread Spectrum Up Parameter 2.**

Register 321.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_SSUPP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MS2_SSUPP3[7:0]	**MultiSynth2 Spread Spectrum Up Parameter 3.**

Register 322.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS2_SSUPP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MS2_SSUPP3[14:8]	**MultiSynth2 Spread Spectrum Up Parameter 3.**

Register 323.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_SSUPP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_SSUPP1[7:0]	**MultiSynth2 Spread Spectrum Up Parameter 1.**

Register 324.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_SSUDP1[3:0]				MS2_SSUPP1[11:8]			
Type	R/W				R/W			

Reset value = 1001 0000

Bit	Name	Function
7:4	MS2_SSUDP1[3:0]	**MultiSynth2 Spread Spectrum Up/Down Parameter 1.**
3:0	MS2_SSUPP1[11:8]	**MultiSynth2 Spread Spectrum Up Parameter 1.**

Register 325.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_SSUDP1[11:4]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	MS2_SSUDP1[11:4]	**MultiSynth2 Spread Spectrum Up/Down Parameter 1.**

Register 326.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_SSDNP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_SSDNP2[7:0]	**MultiSynth2 Spread Spectrum Down Parameter 2.**

Register 327.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS2_SSDNP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MS2_SSDNP2[14:8]	**MultiSynth2 Spread Spectrum Down Parameter 2.**

Register 328.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_SSDNP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MS2_SSDNP3[7:0]	**MultiSynth2 Spread Spectrum Down Parameter 3.**

Register 329.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS2_SSDNP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MS2_SSDNP3[14:8]	**MultiSynth2 Spread Spectrum Down Parameter 3.**

Register 330.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_SSDNP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS2_SSDNP1[7:0]	**MultiSynth2 Spread Spectrum Down Parameter 1.**

Register 331.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS2_SSDNP1[11:8]			
Type	R/W				R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:0	MS2_SSDNP1[11:8]	**MultiSynth2 Spread Spectrum Down Parameter 1.**

Register 335.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_SSUPP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_SSUPP2[7:0]	**MultiSynth3 Spread Spectrum Up Parameter 2.**

Register 336.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS3_SSUPP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MS3_SSUPP2[14:8]	**MultiSynth3 Spread Spectrum Up Parameter 2.**

Register 337.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_SSUPP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MS3_SSUPP3[7:0]	**MultiSynth3 Spread Spectrum Up Parameter 3.**

Register 338.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS3_SSUPP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MS3_SSUPP3[14:8]	**MultiSynth3 Spread Spectrum Up Parameter 3.**

Register 339.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_SSUPP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_SSUPP1[7:0]	**MultiSynth3 Spread Spectrum Up Parameter 1.**

Register 340.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_SSUDP1[3:0]				MS3_SSUPP1[11:8]			
Type	R/W				R/W			

Reset value = 1001 0000

Bit	Name	Function
7:4	MS3_SSUDP1[3:0]	**MultiSynth3 Spread Spectrum Up/Down Parameter 1.**
3:0	MS3_SSUPP1[11:8]	**MultiSynth3 Spread Spectrum Up Parameter 1.**

Register 341.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_SSUDP1[11:4]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	MS3_SSUDP1[11:4]	**MultiSynth3 Spread Spectrum Up Parameter 2.**

Register 342.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_SSDNP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_SSDNP2[7:0]	**MultiSynth3 Spread Spectrum Down Parameter 2.**

Register 343.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS3_SSDNP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MS3_SSDNP2[14:8]	**MultiSynth3 Spread Spectrum Down Parameter 2.**

Register 344.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_SSDNP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MS3_SSDNP3[7:0]	**MultiSynth3 Spread Spectrum Down Parameter 3.**

Register 345.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MS3_SSDNP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MS3_SSDNP3[14:8]	**MultiSynth3 Spread Spectrum Down Parameter 3.**

Register 346.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_SSDNP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MS3_SSDNP1[7:0]	**MultiSynth3 Spread Spectrum Down Parameter 1.**

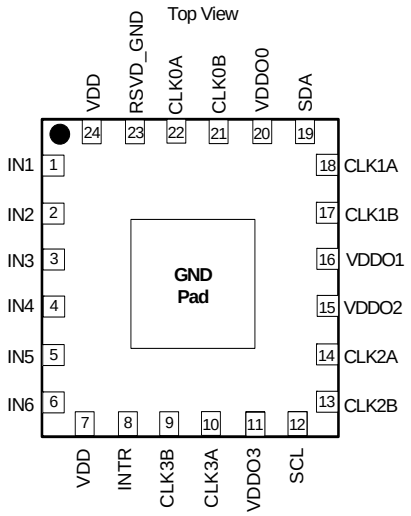
Register 347.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MS3_SSDNP1[11:8]			
Type	R/W				R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:0	MS3_SSDNP1[11:8]	**MultiSynth3 Spread Spectrum Down Parameter 1.**

7. Pin Descriptions



Note: Center pad must be tied to GND for normal operation.

Table 17. Si5338 Pin Descriptions

Pin #	Pin Name	I/O	Signal Type	Description
1,2	IN1/IN2	I	Multi	**CLKIN/CLKINB.** These pins are used as the main differential clock input or as the XTAL input. See "3.2. Input Stage" on page 17, Figure 3 and Figure 4, for connection details. Clock inputs to these pins must be ac-coupled. Keep the traces from pins 1,2 to the crystal as short as possible and keep other signals and radiating sources away from the crystal. When not in use, leave IN1 unconnected and IN2 connected to GND.

Table 17. Si5338 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
3	IN3	I	Multi	This pin can have one of the following functions depending on the part number: **CLKIN** (for Si5338A/B/C and Si5338N/P/Q devices only) Provides a high-impedance clock input for single ended clock signals. This input should be dc-coupled as shown in “3.2. Input Stage”, Figure 3. If this pin is not used, it should be connected to ground. **PINC** (for Si5338D/E/F devices only) Used as the phase increment pin. See "3.9.2. Output Phase Increment/Decrement" on page 24 for more details. Minimum pulse width of 100 ns is required for proper operation. If this pin is not used, it should be connected to ground. **FINC** (for Si5338G/H/J devices only) Used as the frequency increment pin. See "3.9.1. Frequency Increment/Decrement" on page 23 for more details. Minimum pulse width of 100 ns is required for proper operation. If this pin is not used, it should be connected to ground. **OEB** (for Si5338K/L/M devices only) Used as an output enable pin. 0 = All outputs enabled; 1 = All outputs disabled. By default, outputs are tri-stated when disabled.
4	IN4	I	Multi	This pin can have one of the following functions depending on the part number **I^2C_LSB** (for Si5338A/B/C and Si5338K/L/M devices only) This is the LSB of the Si5338 I^2C address. 0 = I^2C address 70h (111 0000), 1 = I^2C address 71h (111 0001). **FDBK** (for Si5338N/P/Q devices only) Provides a high-impedance feedback input for single-ended clock signals. This input should be dc-coupled as shown in “3.2. Input Stage”, Figure 3. If this pin is not used, it should be connected to ground. **PDEC** (for Si5338D/E/F) devices only) Used as the phase decrement pin. See “3.9.2. Output Phase Increment/Decrement” for more details. Minimum pulse width of 100 ns is required for proper operation. If this pin is not used, it should be connected to ground. **FDEC** (for Si5338G/H/J devices only) Used as the frequency decrement pin. See “3.9.1. Frequency Increment/Decrement” for more details. Minimum pulse width of 100 ns is required for proper operation. If this pin is not used, it should be connected to ground.

Table 17. Si5338 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
5,6	IN5/IN6	I	Multi	**FDBK/FDBKB.** These pins can be used as a differential feedback input in zero delay mode or as a secondary clock input. See section 3.2, Figure 3, for termination details. See "3.9.5. Zero-Delay Mode" on page 24 for zero delay mode set-up. Inputs to these pins must be ac-coupled. When not in use, leave IN5 unconnected and IN6 connected to GND.
7	VDD	VDD	Supply	**Core Supply Voltage.** This is the core supply voltage, which can operate from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.
8	INTR	O	Open Drain	**Interrupt.** A typical pullup resistor of 1–4 kΩ is used on this pin. This pin can be pulled up to a supply voltage as high as 3.6 V regardless of the other supply voltages on pins 7, 11, 15, 16, 20, and 24. The interrupt condition allows the pull up resistor to pull the output up to the supply voltage.
9	CLK3B	O	Multi	**Output Clock B for Channel 3.** May be a single-ended output or half of a differential output with CLK3A being the other differential half. If unused, leave this pin floating.
10	CLK3A	O	Multi	**Output Clock A for Channel 3.** May be a single-ended output or half of a differential output with CLK3B being the other differential half. If unused, leave this pin floating.
11	VDDO3	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage (3.3, 2.5, 1.8, or 1.5 V) for CLK3A,B. A 0.1 µF capacitor must be located very close to this pin. If CLK3 is not used, this pin must be tied to VDD (pin 7, 24).
12	SCL	I	LVCMOS	**I^2C Serial Clock Input.** This is the serial clock input for the I^2C bus. A pullup resistor at this pin is required. Typical values would be 1–4 kΩ. See the I^2C bus spec for more information. This pin is 3.3 V tolerant regardless of the other supply voltages on pins 7, 11, 15, 16, 20, 24.
13	CLK2B	O	Multi	**Output Clock B for Channel 2.** May be a single-ended output or half of a differential output with CLK2A being the other differential half. If unused, leave this pin floating.
14	CLK2A	O	Multi	**Output Clock A for Channel 2.** May be a single-ended output or half of a differential output with CLK2B being the other differential half. If unused, leave this pin floating.

Table 17. Si5338 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
15	VDDO2	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage (3.3, 2.5, 1.8, or 1.5 V) for CLK2A,B. A 0.1 µF capacitor must be located very close to this pin. If CLK2 is not used, this pin must be tied to VDD (pin 7, 24).
16	VDDO1	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage (3.3, 2.5, 1.8, or 1.5 V) for CLK1A,B. A 0.1 µF capacitor must be located very close to this pin. If CLK1 is not used, this pin must be tied to VDD (pin 7, 24).
17	CLK1B	O	Multi	**Output Clock B for Channel 1.** May be a single-ended output or half of a differential output with CLK1A being the other differential half. If unused, leave this pin floating.
18	CLK1A	O	Multi	**Output Clock A for Channel 1.** May be a single-ended output or half of a differential output with CLK1B being the other differential half. If unused, leave this pin floating.
19	SDA	I/O	LVCMOS	**I^2C Serial Data.** This is the serial data for the I^2C bus. A pullup resistor at this pin is required. Typical values would be 1–4 kΩ. See the I^2C bus spec for more information. This pin is 3.3 V tolerant regardless of the other supply voltages on pins 7, 11, 15, 16, 20, 24.
20	VDDO0	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage (3.3, 2.5, 1.8, or 1.5 V) for CLK0A,B. A 0.1 µF capacitor must be located very close to this pin. If CLK0 is not used, this pin must be tied to VDD (pin 7, 24).
21	CLK0B	O	Multi	**Output Clock B for Channel 0.** May be a single-ended output or half of a differential output with CLK0A being the other differential half. If unused, leave this pin floating.
22	CLK0A	O	Multi	**Output Clock A for Channel 0.** May be a single-ended output or half of a differential output with CLK0B being the other differential half. If unused, leave this pin floating.
23	GND	GND	GND	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device.
24	VDD	VDD	Supply	**Core Supply Voltage.** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.
GND PAD	GND	GND	GND	**Ground Pad.** This is the large pad in the center of the package. Device specifications cannot be guaranteed unless the ground pad is properly connected to a ground plane on the PCB. See Table 20, “PCB Land Pattern,” on page 167 for ground via requirements.

8. Device Pinout by Part Number

The Si5338 is orderable in three different speed grades: Si5338A/D/G/K/N have a maximum output clock frequency limit of 710 MHz. Si5338B/E/H/L/P have a maximum output clock frequency of 350 MHz. Si5338C/F/J/M/Q have a maximum output clock frequency of 200 MHz.

Devices are also orderable according to the pin control functions available on Pins 3 and 4:

- **CLKIN**—single-ended clock input
- **I2C_LSB**—determines the LSB bit of the 7-bit I^2C address
- **FINC**—frequency increment pin
- **FDEC**—frequency decrement pin
- **PINC**—phase increment pin
- **PDEC**—phase decrement pin
- **FDBK**—single-ended feedback input
- **OEB**—output enable

Table 18. Pin Function by Part Number

Pin #	Si5338A: 710 MHz Si5338B: 350 MHz Si5338C: 200 MHz	Si5338D: 710 MHz Si5338E: 350 MHz Si5338F: 200 MHz	Si5338G: 710 MHz Si5338H: 350 MHz Si5338J: 200 MHz	Si5338K: 710 MHz Si5338L: 350 MHz Si5338M: 200 MHz	Si5338N: 710 MHz Si5338P: 350 MHz Si5338Q: 200 MHz
1	CLKIN[1]	CLKIN[1]	CLKIN[1]	CLKIN[1]	CLKIN[1]
2	CLKINB[1]	CLKINB[1]	CLKINB[1]	CLKINB[1]	CLKINB[1]
3	CLKIN[2]	PINC	FINC	OEB	CLKIN[2]
4	I2C_LSB	PDEC	FDEC	I2C_LSB	FDBK[3]
5	FDBK[4]	FDBK[4]	FDBK[4]	FDBK[4]	FDBK[4]
6	FDBKB[4]	FDBKB[4]	FDBKB[4]	FDBKB[4]	FDBKB[4]
7	VDD	VDD	VDD	VDD	VDD
8	INTR	INTR	INTR	INTR	INTR
9	CLK3B	CLK3B	CLK3B	CLK3B	CLK3B
10	CLK3A	CLK3A	CLK3A	CLK3A	CLK3A
11	VDDO3	VDDO3	VDDO3	VDDO3	VDDO3
12	SCL	SCL	SCL	SCL	SCL
13	CLK2B	CLK2B	CLK2B	CLK2B	CLK2B
14	CLK2A	CLK2A	CLK2A	CLK2A	CLK2A
15	VDDO2	VDDO2	VDDO2	VDDO2	VDDO2
16	VDDO1	VDDO1	VDDO1	VDDO1	VDDO1

Notes:
1. CLKIN/CLKINB on pins 1 and 2 are differential clock inputs or XTAL inputs.
2. CLKIN on pin 3 is a single-ended clock input.
3. FDBK on pin 4 is a single-ended feedback input.
4. FDBK/FDBKB on pins 5 and 6 are differential feedback inputs.

Table 18. Pin Function by Part Number (Continued)

Pin #	Si5338A: 710 MHz Si5338B: 350 MHz Si5338C: 200 MHz	Si5338D: 710 MHz Si5338E: 350 MHz Si5338F: 200 MHz	Si5338G: 710 MHz Si5338H: 350 MHz Si5338J: 200 MHz	Si5338K: 710 MHz Si5338L: 350 MHz Si5338M: 200 MHz	Si5338N: 710 MHz Si5338P: 350 MHz Si5338Q: 200 MHz
17	CLK1B	CLK1B	CLK1B	CLK1B	CLK1B
18	CLK1A	CLK1A	CLK1A	CLK1A	CLK1A
19	SDA	SDA	SDA	SDA	SDA
20	VDDO0	VDDO0	VDDO0	VDDO0	VDDO0
21	CLK0B	CLK0B	CLK0B	CLK0B	CLK0B
22	CLK0A	CLK0A	CLK0A	CLK0A	CLK0A
23	GND	GND	GND	GND	GND
24	VDD	VDD	VDD	VDD	VDD

Notes:
1. CLKIN/CLKINB on pins 1 and 2 are differential clock inputs or XTAL inputs.
2. CLKIN on pin 3 is a single-ended clock input.
3. FDBK on pin 4 is a single-ended feedback input.
4. FDBK/FDBKB on pins 5 and 6 are differential feedback inputs.

9. Package Outline: 24-Lead QFN

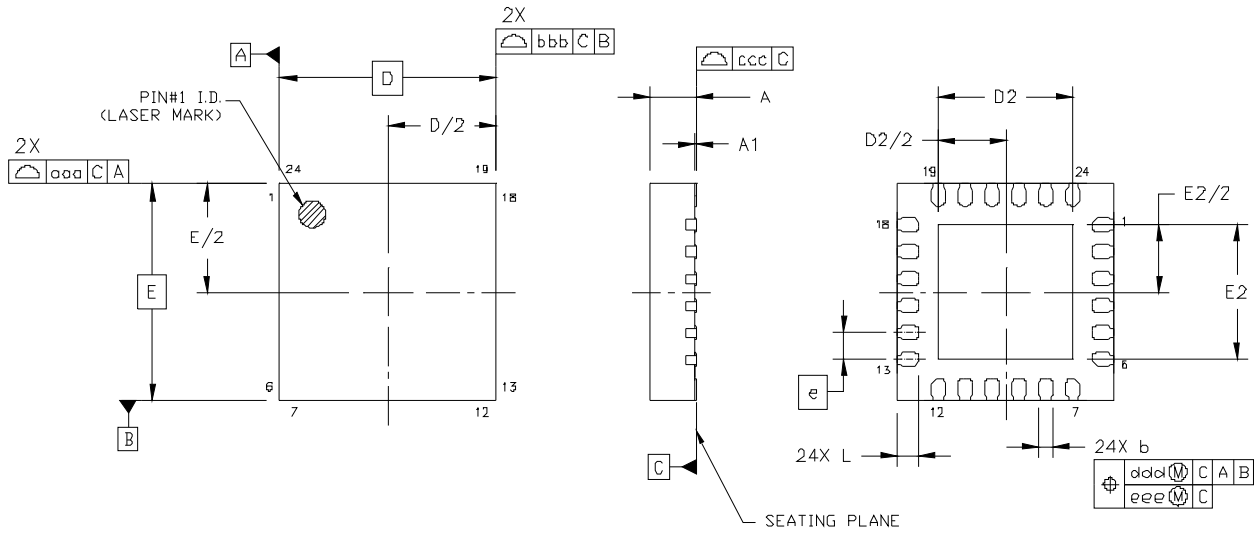


Figure 24. 24-Lead Quad Flat No-lead (QFN)

Table 19. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC.	
D2	2.35	2.50	2.65
e		0.50 BSC.	
E		4.00 BSC.	
E2	2.35	2.50	2.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10. Recommended PCB Layout

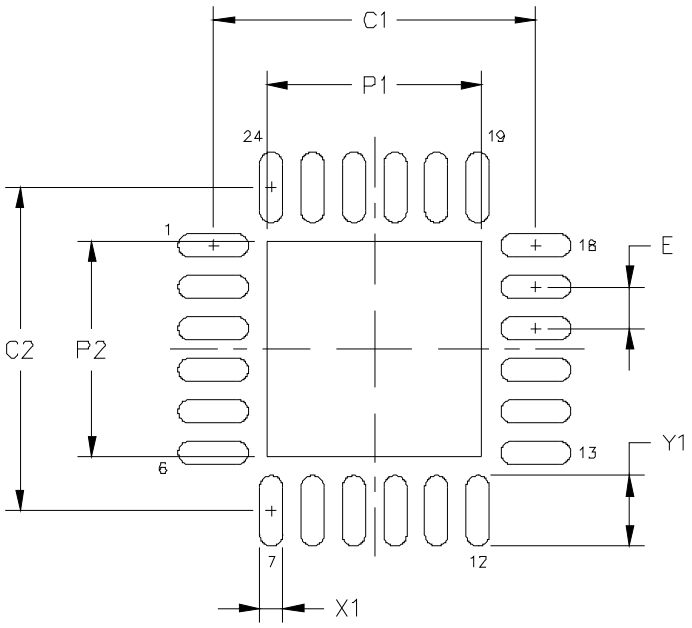


Table 20. PCB Land Pattern

Dimension	Min	Nom	Max
P1	2.50	2.55	2.60
P2	2.50	2.55	2.60
X1	0.20	0.25	0.30
Y1	0.75	0.80	0.85
C1	3.90		
C2	3.90		
E	0.50		

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. Center pad should be connected to the nearest GND plane.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

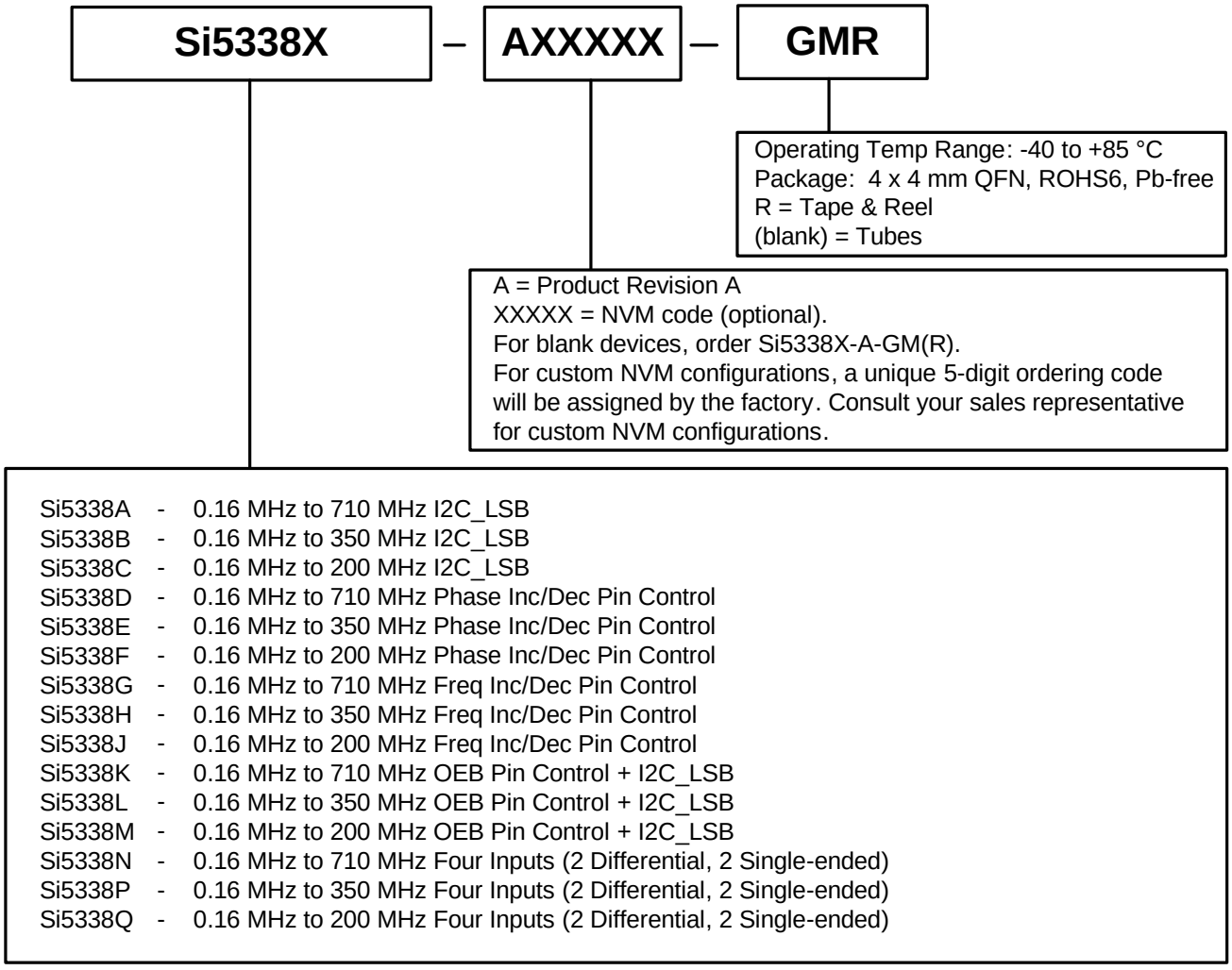
Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
9. A 2x2 array of 1.0 mm square openings on 1.25 mm pitch should be used for the center ground pad.

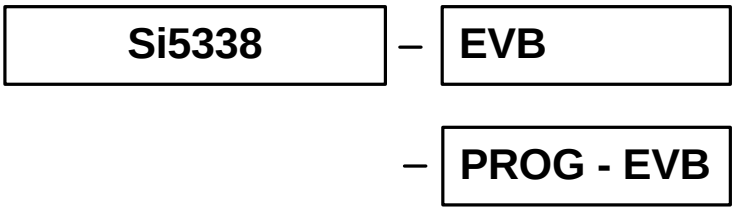
Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

11. Ordering Information



Evaluation Boards



Si5338 Evaluation Board

Si5338 Field Programmer

DOCUMENT CHANGE LIST

Revision 0.1 to 0.2

- Updated block diagram to show Rn output divider and PLL bypass mode
- Updated pin description to include FDBK±
- Updated Table 3. DC Characteristics
- Updated Table 12. Jitter Specifications
- Added Supply Current vs. Output Frequency
- Updated package outline specification
- Clarified input clock configuration register settings
- Updated DRV_INVERTn[1:0] settings
- Added PLL bypass mode
- Added LOS_FDBK description
- Added additional detail to phase increment/ decrement and frequency increment/decrement descriptions
- Clarified output driver powerdown options
- Clarified entry to self-calibration mode
- Updated ordering guide

Revision 0.2 to 0.3

- Changed minimum output clock frequency from 5 MHz to 1 MHz.
- Updated slew rates.
- Updated " Features" on page 1.
- Updated Table 6, “Input and Output Clock Characteristics,” on page 7.
- Deleted Table 12, “Output Driver Slew Rate Control”.

Revision 0.3 to 0.5

- Major editorial changes to all sections to improve clarity
- Completed electrical specification tables with final characterization results
- Revised the maximum input and output frequencies from 700 MHz to 710 MHz
- Improved jitter specifications to reflect updated characterization results
- Added new Si5338N/P/Q ordering codes
- Added typical application diagrams
- Added an application section to highlight the flexibility of the Si5338 in various timing functions
- Added a configuration section to clarify configuration options

Revision 0.5 to 0.55

- Editorial changes to section 3.5 “Configuring the Si5338” to improve clarity on ordering custom Si5338 and on configuring "blank" Si5338.
- Added pin numbers to device package drawings.
- Updated ordering information to include evaluation boards.
- Updated first page description and applications
- Added θ_{JC} to specification tables.
- Added GbE RM jitter specification with 1.875–20 MHz integration band.

Revision 0.55 to 0.6

- Changed output duty cycle to 45–55%.
- All I^2C address now in binary.
- Changed ordering information to reflect 710 MHz limit.
- Info on POR and soft reset added.
- Updated Figure 14 on page 24.
- Added register section.
- Update programming procedure in “3.5. Configuring the Si5338” to improve robustness.
- Updated Figure 9 to include the entire programming procedure.
- Added "3.2.1. Loss-of-Signal (LOS) Alarm Detectors" on page 17 to show the location of the LOS detector circuits.
- Updated input circuit diagrams in "3.2. Input Stage" on page 17.
- Update block diagrams with new input circuit diagrams.

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