

HALOGEN

FREE

50 m Ω , Slew Rate Controlled Load Switch in WCSP

DESCRIPTION

The SiP32460, SiP32461, and SiP32462 are slew rate controlled integrated high side load switches that operate in the input voltage range from 1.2 V to 5.5 V.

This series of design feature slew rate control, reverse blocking, output discharge, and control logic pull down. The devices are logic high enabled.

The SiP32460, SIP32461, and SiP32462 are available in compact wafer level WCSP package, WCSP4 $0.76~\text{mm} \times 0.76~\text{mm}$ with 0.4~mm pitch.

FEATURES

- Low input voltage, 1.2 V to 5.5 V
- Low Ron, 54 mΩ/typ. at 3 V
- Slew rate control
- · Low logic control
- 7.5 µs turn-on time at 5 V (SiP32462)
- · Reverse current blocking when disabled
- Integrated output discharge switch (SiP32461)
- Integrated pull down resistor at "EN"
- 4-bump WCSP package
- Material categorization: For definitions of compliance please see www.vishav.com/doc?99912

APPLICATIONS

- · Smart phones
- · GPS and portable media players
- Tablet computer
- Medical and healthcare equipment
- Industrial and instrument
- Game console

DEVICE OPTIONS										
PART NUMBER	R _{on} (mΩ)	t _{on} (μs)	t _{d(off)}	REVERSE BLOCKING	R _{DISCHARGE}	EN _{LOGIC}	EN/PULL DOWN RESISTOR (Ω)			
SiP32460DB-T2-GE1	54	200	2	Y	N	High enable	2 M			
SiP32461DB-T2-GE1	54	200	2	Υ	Y	High enable	2 M			
SiP32462DB-T2-GE1	54	7.5	2	Υ	N	High enable	2 M			

TYPICAL APPLICATION CIRCUIT

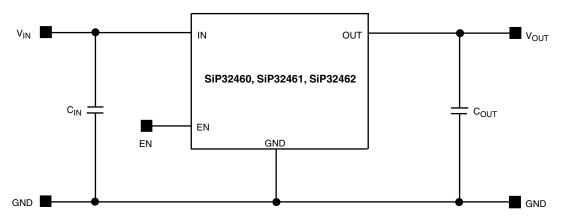


Fig. 1 - Typical Application Circuit

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ABSOLUTE MAXIMUM RATINGS						
PARAMETER	CONDITIONS	LIMIT	UNIT			
Supply Input Voltage V _{IN}	Reference to GND	- 0.3 to 6.5				
Output Voltage V _{OUT}	Reference to GND	- 0.3 to 6.5	V			
Output Voltage V _{OUT}	Pulse at 1 ms reference to GND (1)	- 1.6	v			
Enable Input Voltage EN	Reference to GND	- 0.3 to 6.5				
Maximum Continuous Switch Current		1.2	^			
Maximum Pulse Switch Current	Pulse at 1 ms, 10 % duty cycle	2	A			
ESD Rating (HBM)		4000	V			
Thermal Resistance		280	°C/W			
TEMPERATURE						
Operating Temperature		- 40 to 85				
Operating Junction Temperature		125	°C			
Storage Temperature		- 65 to 150				

Note

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE							
ELECTRICAL PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT			
Input Voltage (V _{IN})	1.2	-	5.5	V			

SPECIFICATIONS								
24244555	0)/14701	TEST CONDITION UNLESS SPECIFIED	LIMITS					
PARAMETER	SYMBOL	V_{IN} = 1.2 V to 5.5 V, T_{A} = - 40 °C to 85 °C (Typical values are at 25 °C)	MIN.	TYP.	MAX.	UNIT		
POWER SUPPLY	•			•				
Quiescent Current	IQ	$V_{IN} = 3.3 \text{ V}, I_{OUT} = 0 \text{ mA}$	-	4.5	7			
Shutdown Current	I _{SD}	OUT = GND	-	0.01	2			
Off Switch Current	I _{DS(off)}	EN = GND, OUT = GND	-	0.01	2	μA		
Devenue Blacking Ownerst		Out = 5 V, IN = 1.2 V, EN = 0 V, (Measured at IN pin)	-	0.01	1			
Reverse Blocking Current	I _{(in)RB}	Out = 5 V, IN = 0 V, EN = 0 V, (Measured at IN pin)	ı	0.01	1			
SWITCH RESISTANCE								
	R _{DS(on)}	I _{OUT} = 500 mA, V _{IN} = 1.2 V, T _A = 25 °C	-	95	150	mΩ		
		I _{OUT} = 500 mA, V _{IN} = 1.5 V, T _A = 25 °C	-	80	120			
On Resistance		I _{OUT} = 500 mA, V _{IN} = 1.8 V, T _A = 25 °C	-	70	100			
		I _{OUT} = 500 mA, V _{IN} = 3 V, T _A = 25 °C	-	54	65			
		I _{OUT} = 500 mA, V _{IN} = 5 V, T _A = 25 °C	-	52	65			
Discharge Switch On	Б	When V _{IN} = 3 V at 25 °C	-	80	-			
Resistance	R_{PD}	When V _{IN} = 1.8 V at 25 °C	-	< 200	-	Ω		
EN Pin Pull Down Resistor	R _{EN}	EN = 1.2 V	1	2.6	5	ΜΩ		
On Resistance Temperature Coefficient	TC _{RDS}		-	2800		ppm/°C		
ON/OFF LOGIC								
EN Input Low Voltage	V _{IL}	V _{IN} = 1.5 V	0.4	-	-	V		
EN Input High Voltage	V _{IH}	V _{IN} = 5.5 V	-	-	1	v		

⁽¹⁾ Negative current injection up to 300 mA

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SPECIFICATIONS									
DADAMETED	SYMBOL	TEST CONDITION UNLESS SPECIFIED	LIMITS			LINUT			
PARAMETER	STMBOL	MBOL V _{IN} = 1.2 V to 5.5 V, T _A = - 40 °C to 85 °C (Typical values are at 25 °C)		TYP.	MAX.	UNIT			
SWITCHING SPEED									
Switch Turn-ON Delay Time (SiP32461)	t _{on_DLY}	R_{LOAD} = 500 Ω , C_L = 0.1 μF V_{IN} = 5 V	-	130	-				
Switch Turn-ON Rise Time (SiP32461)	t _r	R_{LOAD} = 500 Ω , C_L = 0.1 μF V_{IN} = 5 V	-	170	-				
Switch Turn-ON Time (including Turn-ON Delay and Rise Time (SiP32462, fast switching)	t _{on}	R_{LOAD} = 500 Ω , C_L = 0.1 μF V_{IN} = 5 V	ı	7.5	20	μs			
Switch Turn-OFF Delay Time	t _{off}	$R_{LOAD} = 500 \Omega$, $C_L = 0.1 \mu F$, (50 % V_{IN} to 90 % V_{OUT})	-	2	-				

PIN CONFIGURATION

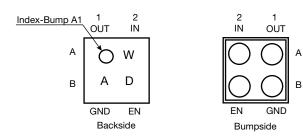


Fig. 2 - WCSP 2 x 2 Package

PIN DESCRIPTION (WSCP PACKAGE)						
PIN#	NAME	FUNCTION				
A1	OUT	Switch output				
A2	IN	Switch input				
B1	GND	Ground connection				
B2	EN	Switch on/off control. A pull down resistor is integrated				

DEVICE MARKING	;		
Row 1	Dot + W	: Dot is A1 locator plus week coc	
Row 2	АВ	: Mark code for part number	
SiP32460 = AF			
SiP32461 = AG			
SiP32462 = AH			

TRUTH TABLE						
EN	SWITCH					
1	ON					
0	OFF					

BLOCK DIAGRAM

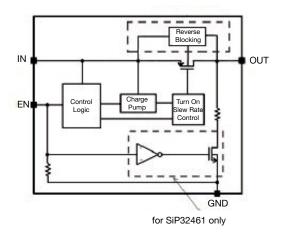


Fig. 3 - Functional Block Diagram

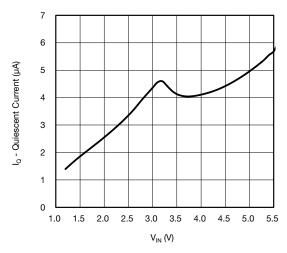


Fig. 4 - Quiescent Current vs. Input Voltage

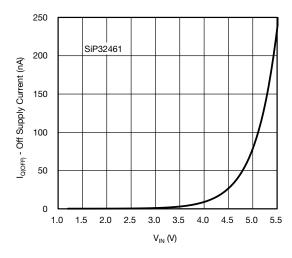


Fig. 5 - Off Supply Current vs. Input Voltage

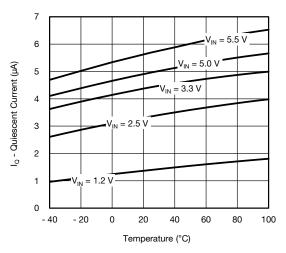


Fig. 6 - Quiescent Current vs. Temperature

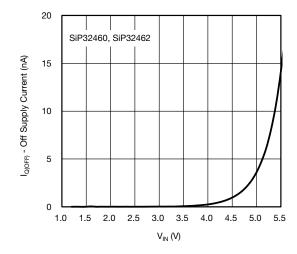


Fig. 7 - Off Supply Current vs. Input Voltage

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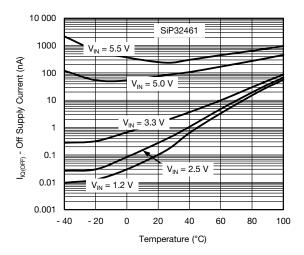


Fig. 8 - Off Supply Current vs. Temperature

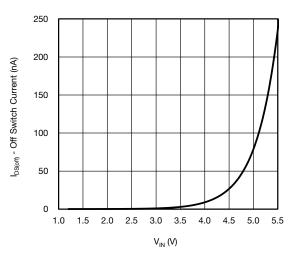


Fig. 9 - Off Switch Current vs. Input Voltage

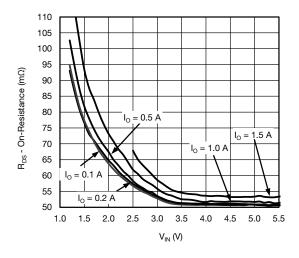


Fig. 10 - R_{DS(on)} vs. Input Voltage

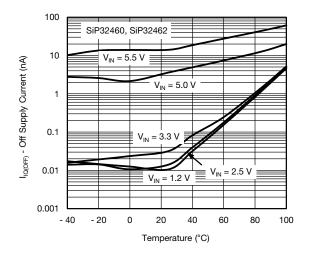


Fig. 11 - Off Supply Current vs. Temperature

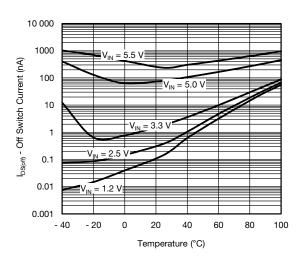


Fig. 12 - Off Switch Current vs. Temperature

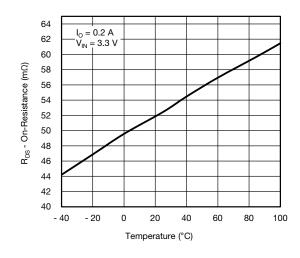


Fig. 13 - R_{DS(on)} vs. Temperature

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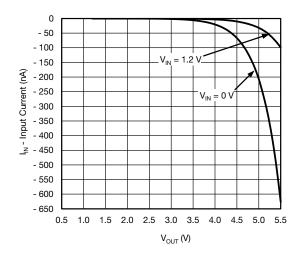


Fig. 14 - Reverse Blocking Current vs. Output Voltage

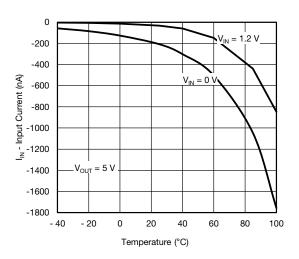


Fig. 15 - Reverse Blocking Current vs. Temperature

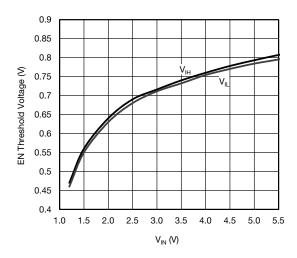


Fig. 16 - EN Threshold Voltage vs. Input Voltage

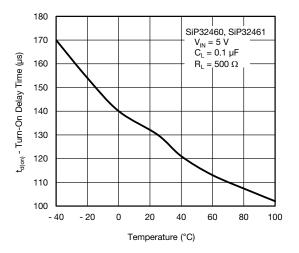


Fig. 17 - Turn-on Delay Time vs. Temperature

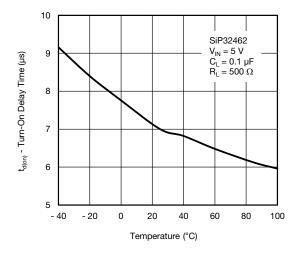


Fig. 18 - Turn-on Delay Time vs. Temperature

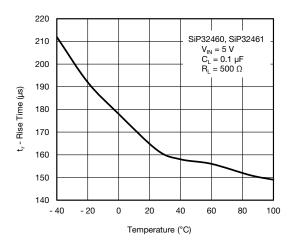


Fig. 19 - Rise Time vs. Temperature

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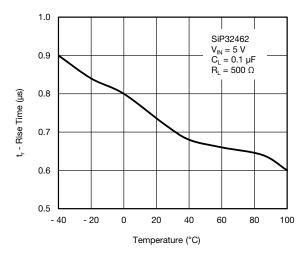


Fig. 20 - Rise Time vs. Temperature

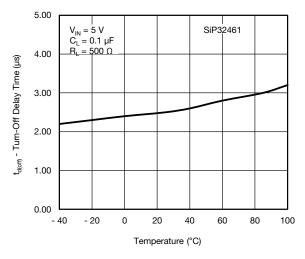


Fig. 21 - Turn-off Delay Time vs. Temperature

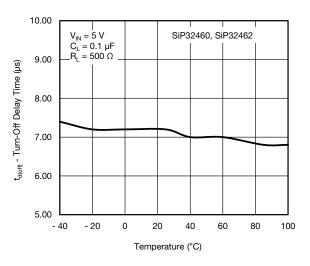


Fig. 22 - Turn-off Delay Time vs. Temperature

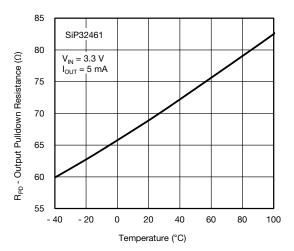
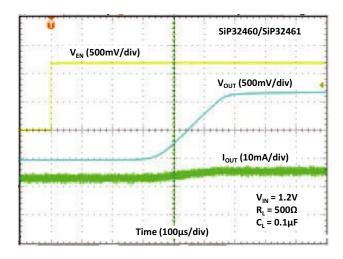
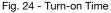


Fig. 23 - Output Pulldown Resistance vs. Temperature





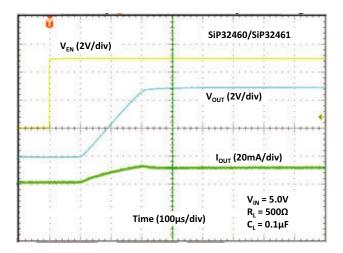


Fig. 27 - Turn-on Time

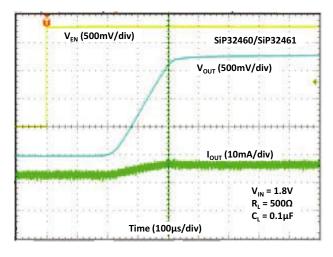


Fig. 25 - Turn-on Time

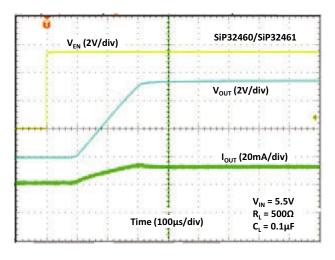


Fig. 28 - Turn-on Time

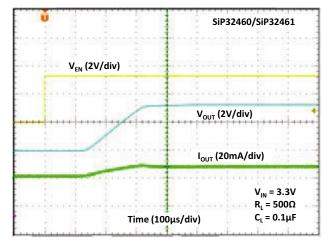


Fig. 26 - Turn-on Time

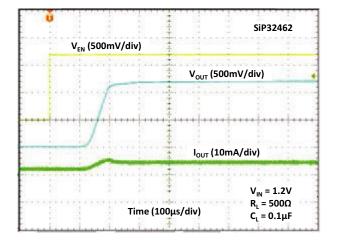


Fig. 29 - Turn-on Time

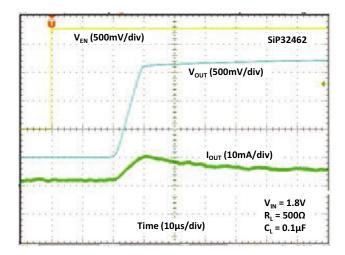


Fig. 30 - Turn-on Time

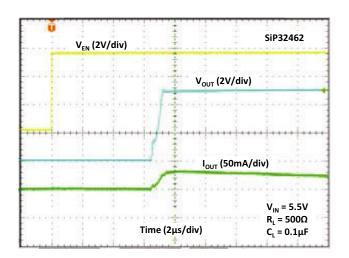


Fig. 33 - Turn-on Time

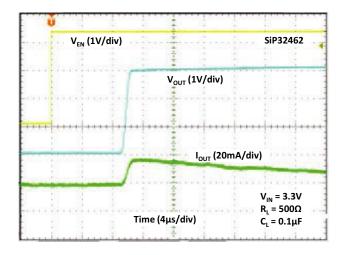


Fig. 31 - Turn-on Time

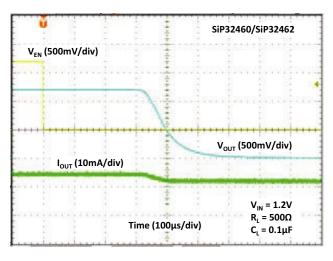


Fig. 34 - Turn-off Time

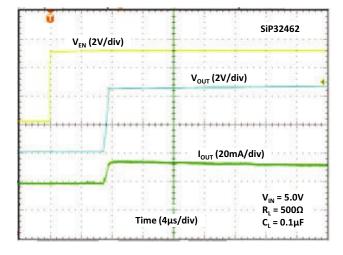


Fig. 32 - Turn-on Time

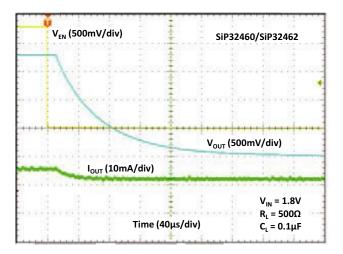


Fig. 35 - Turn-off Time

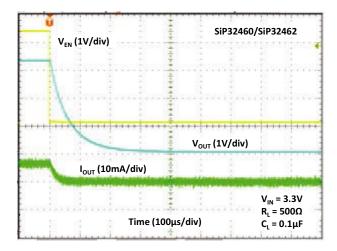


Fig. 36 - Turn-off Time

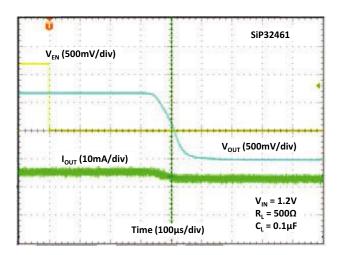


Fig. 39 - Turn-off Time

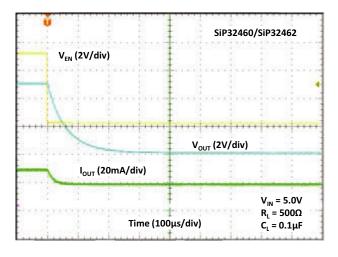


Fig. 37 - Turn-off Time

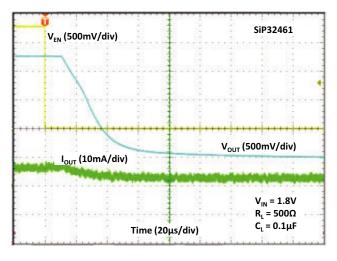


Fig. 40 - Turn-off Time

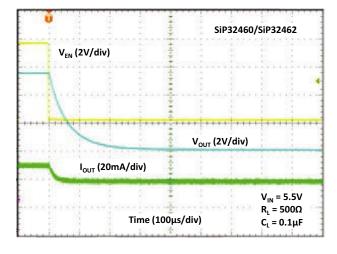


Fig. 38 - Turn-off Time

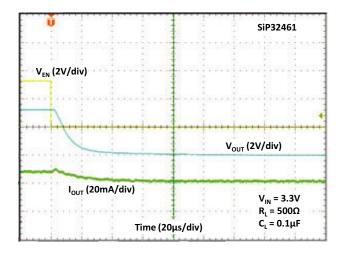
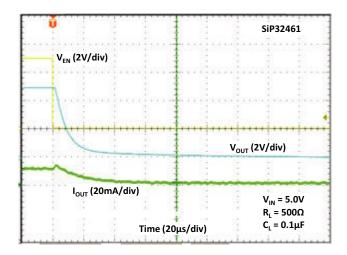


Fig. 41 - Turn-off Time



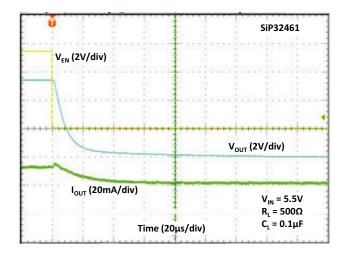


Fig. 42 - Turn-off Time

Fig. 43 - Turn-off Time

DETAILED DESCRIPTION

SiP32460, SiP32461, and SiP32462 are P-channel power MOSFET designed as high side load switches. They incorporate a negative charge pump at the gate to keep the gate to source voltage high when turned on therefore keep the on resistance low at lower input voltage range. SiP32460 and SiP32461 are designed with slow slew rate to minimize the inrush current during turn on. This device has a reverse blocking circuit to prevent the current from going back to the input in case the output voltage is higher than the input voltage. The SiP32461 has an output pulldown resistor to discharge the output capacitance when the device is off.

APPLICATION INFORMATION

Input Capacitor

While a bypass capacitor on the input is not required, a $4.7~\mu F$ or larger capacitor for C_{IN} is recommended in almost all applications. The bypass capacitor should be placed as physically close as possible to the input pin to be effective in minimizing transients on the input. Ceramic capacitors are recommended over tantalum because of their ability to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

A 0.1 μ F capacitor across V_{OUT} and GND is recommended to insure proper slew operation. There is inrush current through the output MOSFET and the magnitude of the inrush current depends on the output capacitor, the bigger the C_{OUT} the higher the inrush current. There are no ESR or capacitor type requirement.

Enable

The EN pin is compatible with CMOS logic voltage levels. It requires at least 0.4 V or below to fully shut down the device and 1 V or above to fully turn on the device. There is a 2.8 $M\Omega$ resistor connected between EN pin and GND pin.

Protection Against Reverse Voltage Condition

This device contains a reverse blocking circuit to keep the output current from flowing back to the input in case the output voltage is higher than the input voltage.

Thermal Considerations

This device is designed to maintain a constant output load current. Due to physical limitations of the layout and assembly of the device the maximum switch current is 1.2 A as stated in the Absolute Maximum Ratings table. However, another limiting characteristic for the safe operating load current is the thermal power dissipation of the package. To obtain the highest power dissipation (and a thermal resistance of 280 °C/W) the device should be connected to a heat sink on the printed circuit board.

The maximum power dissipation in any application is dependant on the maximum junction temperature, $T_{J(max.)} = 125$ °C, the junction-to-ambient thermal resistance, $\theta_{J-A} = 280$ °C/W, and the ambient temperature, T_A , which may be formulaically expressed as:

P (max.) =
$$\frac{T_J (max.) - T_A}{\theta_{J-A}} = \frac{125 - T_A}{280}$$

It then follows that, assuming an ambient temperature of 70 °C, the maximum power dissipation will be limited to about 196 mW.

So long as the load current is below the 1.2 A limit, the maximum continuous switch current becomes a function two things: the package power dissipation and the $R_{DS(ON)}$ at the ambient temperature.

As an example let us calculate the worst case maximum load current at T_A = 70 °C. The worst case $R_{DS(ON)}$ at 25 °C is 65 m Ω at V_{IN} = 1.5 V. The $R_{DS(ON)}$ at 70 °C can be extrapolated from this data using the following formula:

 $R_{DS(ON)}$ (at 70 °C) = $R_{DS(ON)}$ (at 25 °C) x (1 + T_C x ΔT)

Where T_C is 2820 ppm/°C. Continuing with the calculation we have

 $R_{DS(ON)}$ (at 70 °C) = 65 m Ω x (1 + 0.00282 x (70 °C - 25 °C)) = 73.2 m Ω

The maximum current limit is then determined by

$$I_{LOAD}$$
 (max.) $<\sqrt{\frac{P \text{ (max.)}}{R_{DS(ON)}}}$

which in this case is 1.6 A. Under the stated input voltage condition, if the 1.6 A current limit is exceeded the internal die temperature will rise and eventually, possibly damage the device.

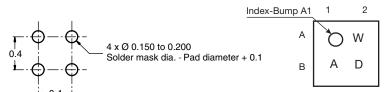
To avoid possible permanent damage to the device and keep a reasonable design margin, it is recommended to operate the device maximum up to 1.2 A only as listed in the Absolute Maximum Ratings table.

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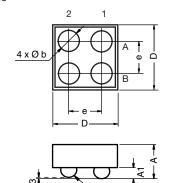
PACKAGE OUTLINE

WCSP: 4 Bumps (2 x 2, 0.4 mm Pitch, 208 µm Bump Height, 0.8 mm x 0.8 mm Die Size)

Mark on backside of die



Recommended Land Pattern All dimensions in millimeters



DIMENSION		MILLIMETERS			INCHES	
DIMENSION	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
А	0.515	0.530	0.545	0.0202	0.0208	0.0214
A1		0.208			0.0081	
b	0.250	0.260	0.270	0.0098	0.0102	0.0106
е		0.400			0.0157	
D	0.720	0.760	0.800	0.0283	0.0299	0.0315

Notes

- (1) Laser mark on the backside surface of die.
- (2) Bumps are SAC396.
- (3) 0.050 max. coplanarity.

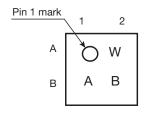
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67754

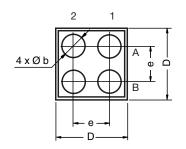
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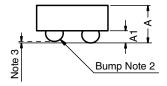
WCSP4: 4 Bumps

(2 x 2, 0.4 mm pitch, 208 μ m bump height, 0.8 mm x 0.8 mm die size)

Mark on backside of die







Notes

- (1) Laser mark on the backside surface of die
- (2) Bumps are SAC396
- (3) 0.050 max. coplanarity

	MILLIMETERS ^a			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
А	0.515	0.530	0.545	0.0202	0.0208	0.0214	
A1		0.208			0.0081		
b	0.250	0.260	0.270	0.0098	0.0102	0.0106	
е	0.400				0.0157		
D	0.720	0.760	0.800	0.0182	0.0193	0.0203	

Note

a. Use millimeters as the primary measurement.

ECN: T11-0497-Rev. B, 10-Oct-11

DWG: 6004



Legal Disclaimer Notice

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