

PNP SILICON POWER TRANSISTORS

SJE1497 transistor is designed for use in general purpose Power amplifier, vertical output application

FEATURES:

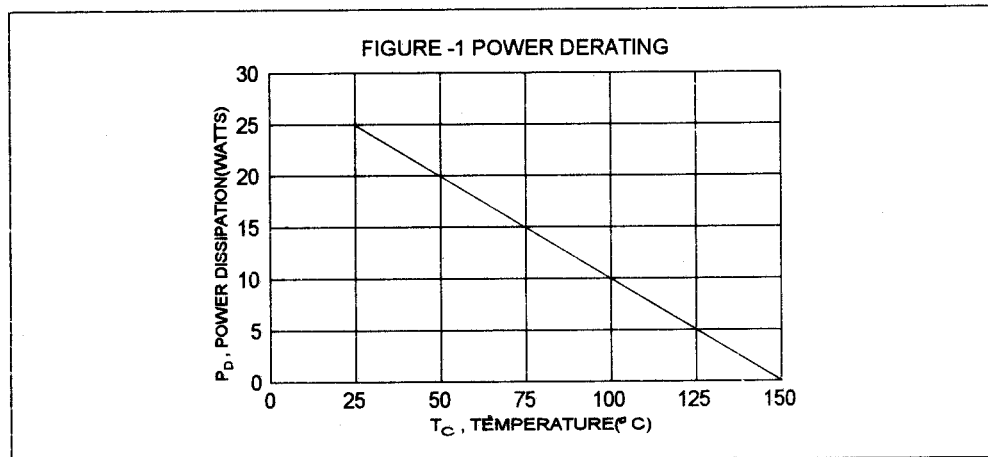
- * Collector-Emitter Voltage
 $V_{CE0} = 150V(\text{Min})$
- * DC Current Gain
 $hFE = 30(\text{Min}) @ I_C = 300mA$

MAXIMUM RATINGS

Characteristic	Symbol	SJE1497	Unit
Collector-Emitter Voltage	V_{CE0}	150	V
Collector-Base Voltage	V_{CB0}	200	V
Emitter-Base Voltage	V_{EB0}	6.0	V
Collector Current - Continuous - Peak	I_C I_{CM}	1.5 3.0	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	25 0.2	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

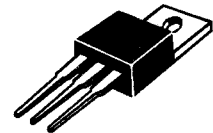
Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	$R_{\theta jc}$	5.0	$^\circ\text{C/W}$



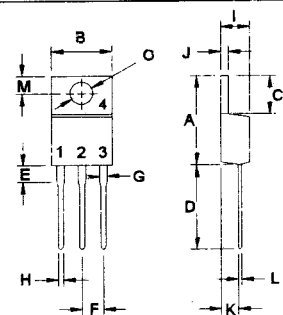
PNP

SJE1497

1.5 AMPERE
POWER
TRANSISTORS
150 VOLTS
25 WATTS



TO-220



PIN 1.BASE
2.COLLECTOR
3.EMITTER
4.COLLECTOR(CASE)

DIM	MILLIMETERS	
	MIN	MAX
A	14.68	15.31
B	9.78	10.42
C	5.01	6.52
D	13.06	14.62
E	3.57	4.07
F	2.42	3.66
G	1.12	1.36
H	0.72	0.96
I	4.22	4.98
J	1.14	1.38
K	2.20	2.97
L	0.33	0.55
M	2.48	2.98
O	3.70	3.90

ELECTRICAL CHARACTERISTICS ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Base Voltage ($I_C = 100 \mu\text{A}$, $I_B = 0$)	V_{CBO}	200		V
Collector-Emitter Voltage ($I_C = 30 \text{ mA}$, $I_B = 0$)	V_{CEO}	150		V
Emitter-Base Voltage ($I_B = 1.0 \text{ mA}$, $I_C = 0$)	V_{EBO}	6.0		V
Collector Cutoff Current ($V_{CB} = 120 \text{ V}$, $I_E = 0$)	I_{CBO}		10	μA
Emitter Cutoff Current ($V_{EB} = 4.0 \text{ V}$, $I_C = 0$)	I_{EBO}		10	μA

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 0.3 \text{ A}$, $V_{CE} = 5.0 \text{ V}$)	hFE	30		
Collector-Emitter Saturation Voltage ($I_C = 1.0 \text{ A}$, $I_B = 200 \text{ mA}$)	$V_{CE(sat)}$		1.0	V
Base-Emitter On Voltage ($I_C = 1.0 \text{ A}$, $V_{CE} = 10 \text{ V}$)	$V_{BE(on)}$		1.5	V

SWITCHING CHARACTERISTICS

Turn-on Time	$V_{CC} = 50 \text{ V}$, $I_C = 0.5 \text{ A}$ $I_{B1} = -I_{B2} = 50 \text{ mA}$ $PW = 20 \mu\text{s}$	t_{on}	0.5	μs
Storage Time		t_s	1.0	μs
Fall Time		t_f	0.5	μs

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2.0\%$

FIG-2 $I_c - V_{ce}$

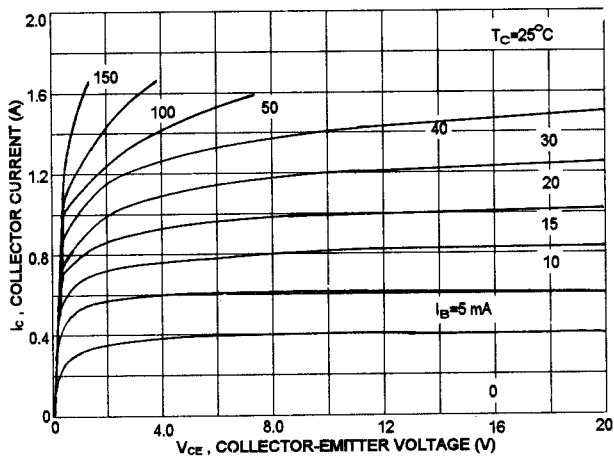


FIG-4 $V_{ce(sat)} - I_c$

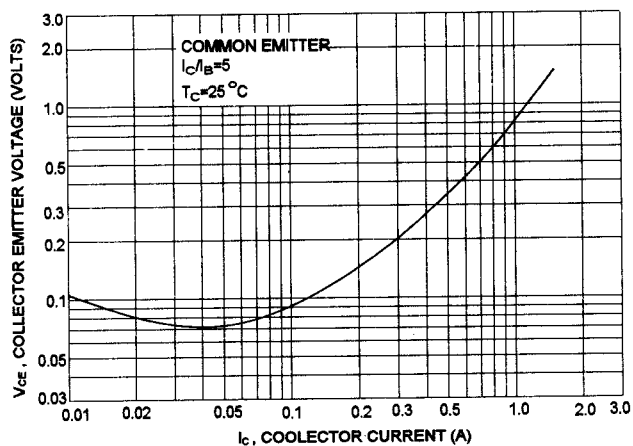
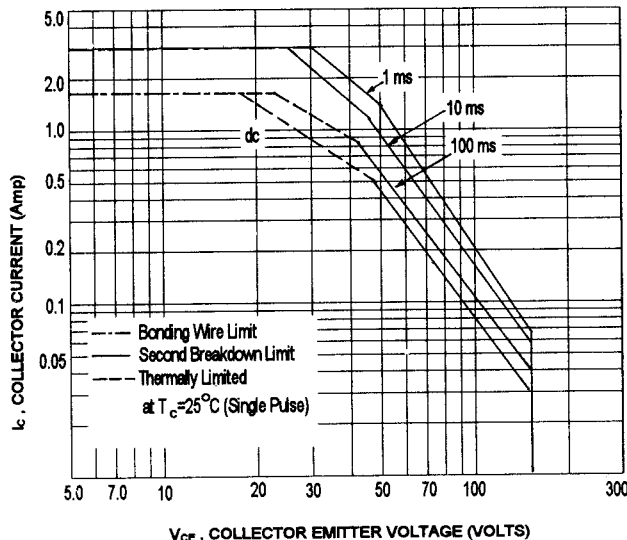


FIG-3 SAFE OPERATING AREA



There are two limitation on the power handling ability of a transistor: average junction temperature and second breakdown safe operating area curves indicate $I_c - V_{ce}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

The data of FIG-3 is base on $T_{j(pk)} = 150^\circ C$; T_c is variable depending on conditions. second breakdown pulse limits are valid for duty cycles to 10% provided $T_{j(pk)} \leq 150^\circ C$. At high case temperatures, thermal limitation will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIG-5 DC CURRENT GAIN

