OVERVIEW

SM5133 series are CMOS LSIs that incorporate two PLLs for signal transmission and reception in cordless telephones.

The SM5133E features 15 communication channels and the SM5133D features 10 communication channels. SM5133 series devices feature parallel input for communication channel selection.

SM5133 series devices operate from a 2.4 to 5.5 V supply and are available in 16-pin plastic DIPs, SOPs and SSOPs.

FEATURES

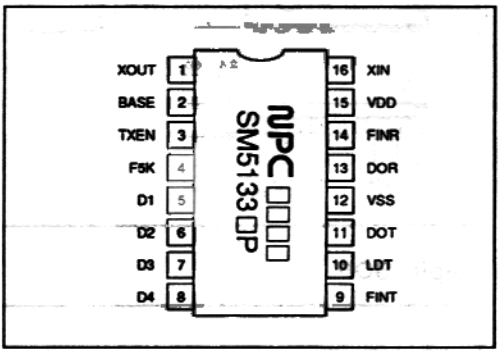
- Transmit and receive PLLs
- Baseset unit and handset unit selection
- 10 communication channels (SM5133D) or 15 communication channels (SM5133E)
- Parallel channel selection
- Built-in digital lock detector
- Standby function suspends transmit function to save power
- 60 MHz maximum operating frequency
- Direct frequency division and locking in transmit PLL at 46 to 49 MHz operating frequency
- 300 mV_{PP} (min) input sensitivity
- 5 kHz reference frequency
- Molybdenum-gate CMOS process
- 2.4 to 5.5 V supply
- 16-pin plastic DIP, SOP and SSOP

LINE-UP

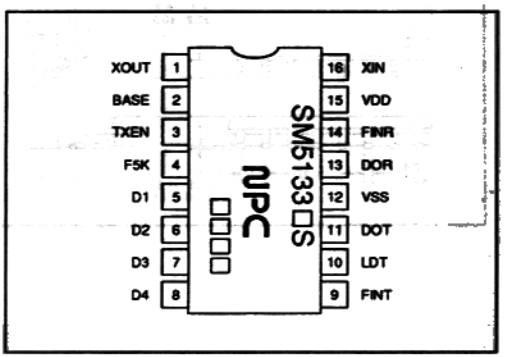
Device	Number of channels	Channel type select	Package
SM5133DP	10	Parallel using pins D1 to D4	16-pin DIP
SM5133DS			16-pin SOP
SM5133DM			16-pin SSOP
SM5133EP	15		16-pin DIP
SM5133ES			16-pin SOP
SM5133EM			16-pin SSOP

PINOUTS

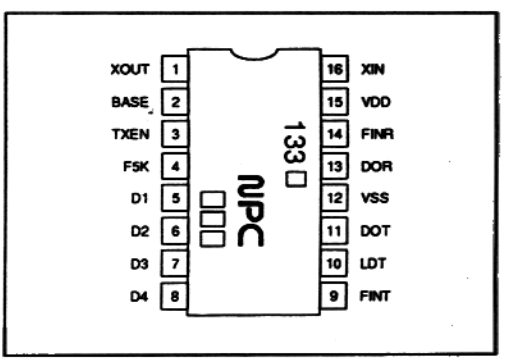
16-pin DIP



16-pin SOP



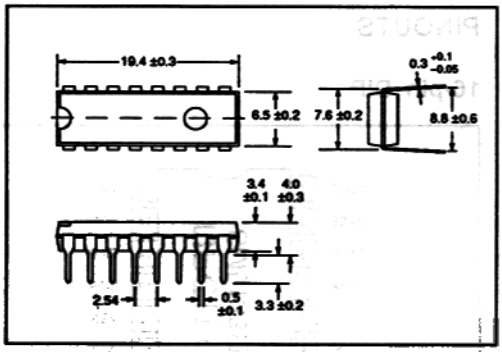
16-pin SSOP



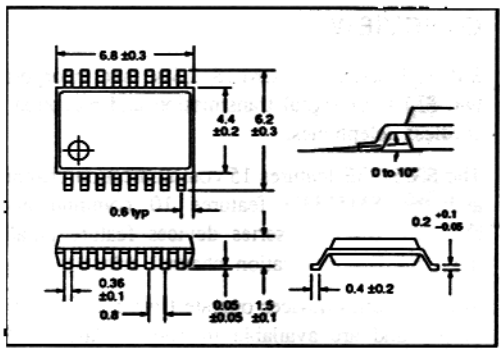
PACKAGE DIMENSIONS

Unit: mm

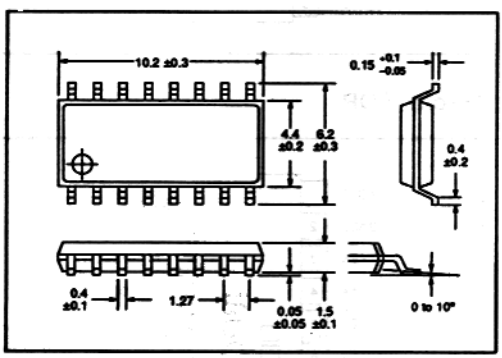
16-pin DIP



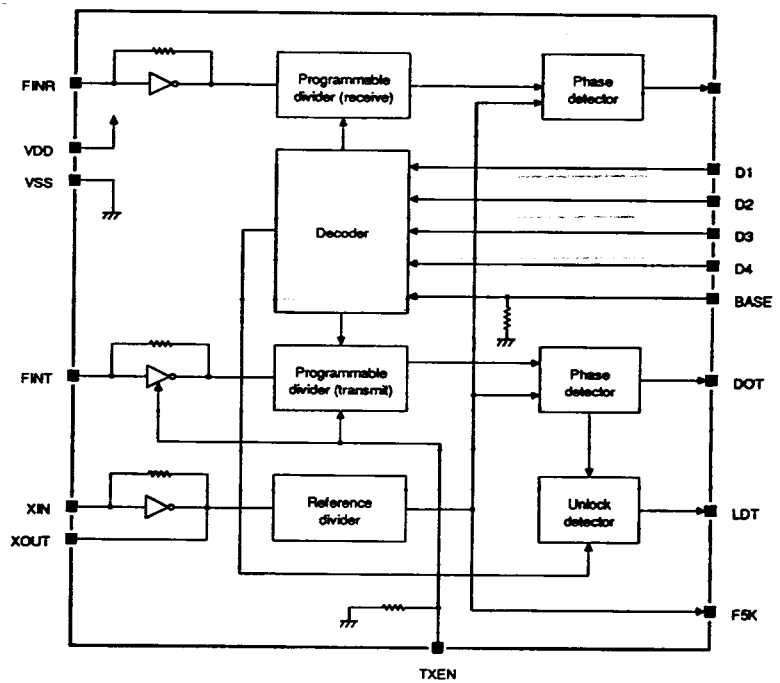
16-pin SSOP



16-pin SOP



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1	XOUT	Crystal oscillator connection. Also connected to 2nd mixer
2	BASE	Baseset/handset unit select input. Handset mode when LOW or open, baseset mode when HIGH. Internal pull-down resistor
3	TXEN	Transmit enable select input. Receive only enabled when LOW, receive and transmit enabled when HIGH. Internal pull-down resistor
4	F5K	5 kHz reference divider output. n-channel open drain
5 to 8	D1 to D4	Communication channel select parallel data input
9	FINT	Transmit programmable divider input. Internal feedback resistance. Allows AC coupling.
10	LDT	Digital lock detector output. HIGH when unlocked (transmit only)
11	DOT	Transmit passive lowpass filter connection
12	VSS	Ground
13	DOR	Receive passive lowpass filter connection
14	FINR	Receive programmable divider input. Internal feedback resistance. Allows AC coupling.
15	VDD	2.4 to 5.5 V supply voltage
16	XIN	Crystal oscillator and capacitor connection. Internal feedback resistance

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	$V_{DD} - V_{SS}$	−0.3 to 7.0	V
Input voltage range	V_{IN}	V_{SS} to V_{DD}	V
Storage temperature range	T_{stg}	−40 to 125	deg. C
Soldering temperature	T_{sld}	255	deg. C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

T_a = 25 deg. C

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	2.4 to 5.5	V

Electrical Characteristics

V_{DD} = 2.4 to 5.5 V, V_{SS} = 0 V, T_a = −30 to 80 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Operating current	I_{DD}	V_{DD} = 3 V. TXEN is HIGH. See note 1.	–	4.0	6.0	mA
		V_{DD} = 5 V. TXEN is HIGH. See note 1.	–	12.0	–	
		V_{DD} = 3 V. TXEN is LOW. See note 2.	–	2.0	3.0	
		V_{DD} = 5 V. TXEN is LOW. See note 2.	–	5.5	–	
Maximum transmit operating frequency	f_{TX}	V_{FINT} = 300 mV_{p-p}, sine wave	60	–	–	MHz
Maximum receive operating frequency	f_{RX}	V_{FINR} = 300 mV_{p-p}, sine wave	50	–	–	MHz
FINT input amplitude	V_{FINT}	f_{TX} = 50 MHz, f_{RX} = 40 MHz, f_{XIN} = 10.24 MHz, sine wave	0.3	–	V_{DD} − 0.5	V_{p-p}
FINR input amplitude	V_{FINR}		0.3	–	V_{DD} − 0.5	V_{p-p}
XIN input amplitude	V_{XIN}		0.8	–	V_{DD} − 0.5	V_{p-p}
BASE and TXEN HIGH-level input current	I_{IH}		–	–	300	µA
LDT, DOT, DOR and F5K HIGH-level output current	I_{OH}	V_{OH} = V_{DD} − 0.4 V	0.4	–	–	mA
LDT, DOT, DOR and F5K LOW-level output current	I_{OL}	V_{OL} = 0.4 V	0.4	–	–	mA

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
IBASE, TXEN and D1 to D4 HIGH-level input voltage.	V_{IH}		V_{DD} – 0.4	–	V_{DD}	V
IBASE, TXEN and D1 to D4 LOW-level input voltage.	V_{IL}		0	–	0.4	V

Notes

1. V_{FINT} = V_{FINR} = 300 mV_{p-p}, f_{TX} = 46.930 MHz, f_{RX} = 39.295 MHz, sine wave input. See TYPICAL APPLICATIONS for external component values.
2. V_{FINR} = 300 mV_{p-p}, f_{RX} = 39.295 MHz, sine wave input. See TYPICAL APPLICATIONS for external component values.

DESIGN NOTES

General

LDT is HIGH when the PLL is unlocked. LDT goes HIGH when the communication channel is switched or when DOT has been HIGH for 3.2 µs. LDT goes LOW 6.4 ±0.4 ms after these conditions no longer apply. See figure 1.

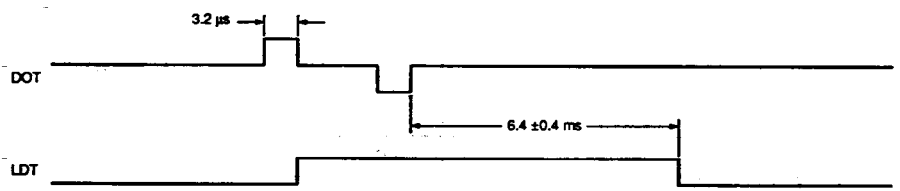


Figure 1. Lock detector timing

F5K has an internal protective diode to prevent electrostatic breakdown. The voltage at this pin must not exceed V_{DD}. F5K should be left open when not in use.

DOT and DOR have 3-state outputs and are intended for use with passive lowpass filters.

Communication Channel Selection

SM5133 series devices have parallel inputs for communication channel selection. The states of D1 to D4 and BASE are used to select one of the available channels.

SM5133D

Base	D4	D3	D2	D1	Channel	Transmit (f_{REF} = 5.0 kHz)		Receive (f_{REF} = 5.0 kHz)		
						f_{TX}/f_{VCO} (kHz)	N	f_{RX} (kHz)	f_{VCO} (kHz)	N
0	0	0	0	1	1	49670	9934	46610	35915	7183
	0	0	1	0	2	49845	9969	46630	35935	7187
	0	0	1	1	3	49860	9972	46670	35975	7195
	0	1	0	0	4	49770	9954	46710	36015	7203
	0	1	0	1	5	49875	9975	46730	36035	7207
	0	1	1	0	6	49830	9966	46770	36075	7215
	0	1	1	1	7	49890	9978	46830	36135	7227
	1	0	0	0	8	49930	9986	46870	36175	7235
	1	0	0	1	9	49990	9998	46930	36235	7247
	1	0	1	0	10	49970	9994	46970	36275	7255
	1	0	1	1	10	49970	9994	46970	36275	7255
	1	1	0	0	10	49970	9994	46970	36275	7255
	1	1	0	1	10	49970	9994	46970	36275	7255
	1	1	1	0	10	49970	9994	46970	36275	7255
	1	1	1	1	10	49970	9994	46970	36275	7255
	0	0	0	0	10	49970	9994	46970	36275	7255
1	0	0	0	1	1	46610	9322	49670	38975	7795
	0	0	1	0	2	46630	9326	49845	39150	7830
	0	0	1	1	3	46670	9334	49860	39165	7833
	0	1	0	0	4	46710	9342	49770	39075	7815
	0	1	0	1	5	46730	9346	49875	39180	7836
	0	1	1	0	6	46770	9354	49830	39135	7827
	0	1	1	1	7	46830	9366	49890	39195	7839
	1	0	0	0	8	46870	9374	49930	39235	7847
	1	0	0	1	9	46930	9386	49990	39295	7859
	1	0	1	0	10	46970	9394	49970	39275	7855
	1	0	1	1	10	46970	9394	49970	39275	7855
	1	1	0	0	10	46970	9394	49970	39275	7855
	1	1	0	1	10	46970	9394	49970	39275	7855
	1	1	1	0	10	46970	9394	49970	39275	7855
	1	1	1	1	10	46970	9394	49970	39275	7855
	0	0	0	0	10	46970	9394	49970	39275	7855

Note

A '0' in the columns for BASE and input data implies LOW-level input voltage, and a '1' implies HIGH-level input voltage.

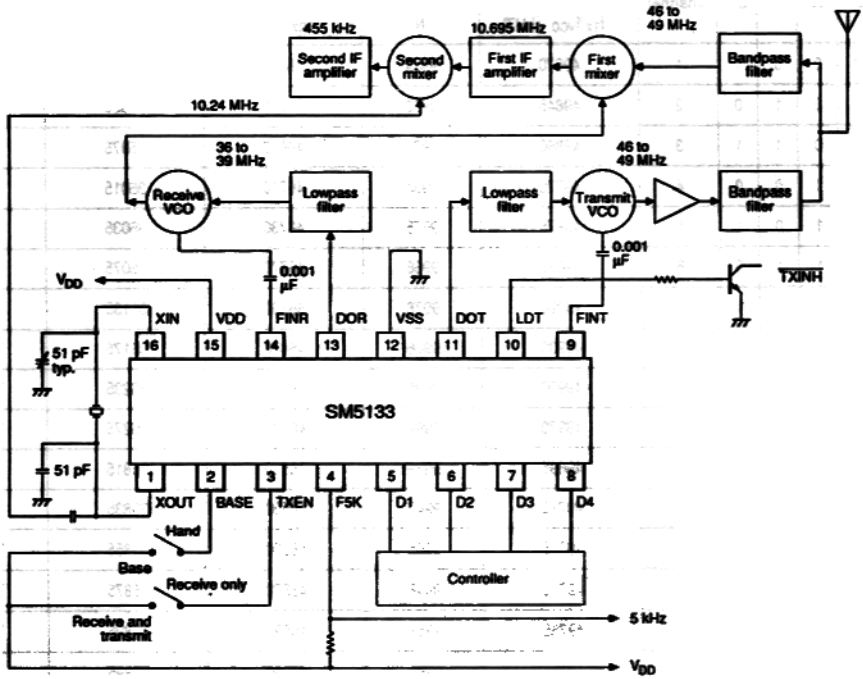
SM5133E

Base	D1	D2	D3	D4	Channel	Transmit (f_{REF} = 5.0 kHz)		Receive (f_{REF} = 5.0 kHZ)		
						f_{TX}/f_{VCO} (kHZ)	N	f_{RX} (kHZ)	f_{VCO} (kHz)	N
0	0	0	0	1	1	49670	9934	46610	35915	7183
	0	0	1	0	2	49845	9969	46630	35935	7187
	0	0	1	1	3	49860	9972	46670	35975	7195
	0	1	0	0	4	49770	9954	46710	36015	7203
	0	1	0	1	5	49875	9975	46730	36035	7207
	0	1	1	0	6	49830	9966	46770	36075	7215
	0	1	1	1	7	49890	9978	46830	36135	7227
	1	0	0	0	8	49930	9986	46870	36175	7235
	1	0	0	1	9	49990	9998	46930	36235	7247
	1	0	1	0	10	49970	9994	46970	36275	7255
	1	0	1	1	11	49695	9939	46510	35815	7163
	1	1	0	0	12	49710	9942	46530	35835	7167
	1	1	0	1	13	49725	9945	46550	35855	7171
	1	1	1	0	14	49740	9948	46570	35875	7175
	1	1	1	1	15	49755	9951	46590	35895	7179
	0	0	0	0	15	49755	9951	46590	35895	7179
1	0	0	0	1	1	46610	9322	49670	38975	7795
	0	0	1	0	2	46630	9326	49845	39150	7830
	0	0	1	1	3	46670	9334	49860	39165	7833
	0	1	0	0	4	46710	9342	49770	39075	7815
	0	1	0	1	5	46730	9346	49875	39180	7836
	0	1	1	0	6	46770	9354	49830	39135	7827
	0	1	1	1	7	46830	9366	49890	39195	7839
	1	0	0	0	8	46870	9374	49930	39235	7847
	1	0	0	1	9	46930	9386	49990	39295	7859
	1	0	1	0	10	46970	9394	49970	39275	7855
	1	0	1	1	11	46510	9302	49695	39000	7800
	1	1	0	0	12	46530	9306	49710	39015	7803
	1	1	0	1	13	46550	9310	49725	39030	7806
	1	1	1	0	14	46570	9314	49740	39045	7809
	1	1	1	1	15	46590	9318	49755	39060	7812
	0	0	0	0	15	46590	9318	49755	39060	7812

Note

A '0' in the columns for BASE and input data implies LOW-level input voltage, and a '1' implies HIGH-level input voltage.

TYPICAL APPLICATIONS



Note

A crystal with f = 10.24 MHz, C_I = 20 Ω and C_L = 30 pF is recommended.