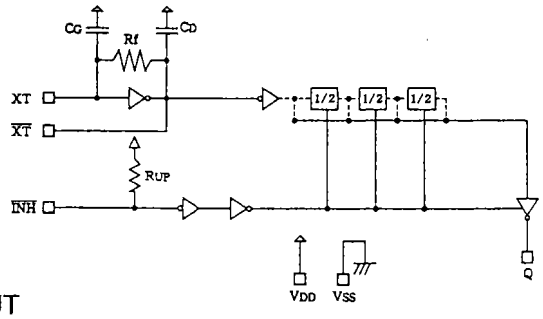
■ OVERVIEW

The SM5610 series are C-MOS ICs for quartz crystal oscillating module. Each IC has a high frequency oscillating circuit and dividers with low current consumption.
There are many kinds of type, capacitor for oscillation on chip or not, output frequency: f0 (fundamental), f0/2, f0/4, or f0/8, and I/O level TTL or CMOS (Refer to the SERIES TABLE.

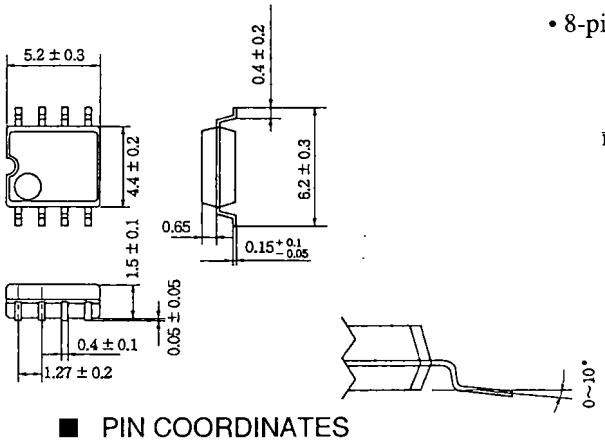
■ FEATURES

- Operating voltage (4V - 6V)
- Built-in feed back resistance of oscillation circuit
- 3-state function
- Law current consumption
- Chip form, 8-pin SOP
- Molybdenum gate C-MOS
- For fundamental wave use

■ BLOCK DIAGRAM

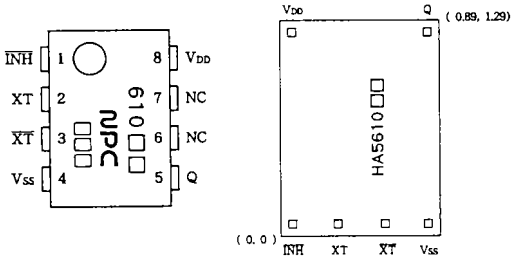


■ PACKAGE DIMENSION



■ PIN OUT

• 8-pin SOP (TOP VIEW)



CHIP SIZE: 0.89 × 1.29mm
CHIP THICKNESS: 400 ±30 µm

■ PIN COORDINATES

UNIT: µm

NAME	X	Y
$\overline{INH}$	145	140
XT	345	140
$\overline{XT}$	545	140
V_{SS}	745	140
Q	745	1150
V_{DD}	145	1155

■ PIN DESCRIPTION

NAME	FUNCTION
XT	Input terminal for oscillating
$\overline{XT}$	Output terminal or oscillating
$\overline{INH}$	"L" High impedance On-chip pull-up resistance
V_{DD}	Power supply
V_{SS}	Ground
Q	Output (Selected by master slice)
	f_0, $f_0/2$, $f_0/4$, or $f_0/8$

f_0: Fundamental frequency

■ SERIES TABLE

VERSIONS	Output frequency	Output duty level	Output current
SM5610K1	f_o	TTL	16mA
K3	$f_o/2$	TTL	16mA
K5	$f_o/4$	TTL	16mA
K7	$f_o/8$	TTL	16mA
H1	f_o	CMOS	4mA
H3	$f_o/2$	CMOS	4mA
H5	$f_o/4$	CMOS	4mA
H7	$f_o/8$	CMOS	4mA
N1	f_o	CMOS	16mA
N3	$f_o/2$	CMOS	16mA
N5	$f_o/4$	CMOS	16mA
N7	$f_o/8$	CMOS	16mA

Note: SOP package is named SM5610 □ □ S.

■ ABSOLUTE MAXIMUM RATING (V_{SS}=0V)

ITEM	SYMBOL	CONDITIONS	UNIT
Supply voltage	V_{DD}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to V_{DD}+0.5	V
Output voltage	V_{OUT}	-0.5 to V_{DD}+0.5	V
Storage temperature	T_{STG1}	-65 to +150 (chip)	°C
	T_{STG2}	-40 to +125 (SOP)	
Output current	I_{OUT}	N, K series 25	mA
		H series 10	
* Power dissipation	P_W	200	mW
* Soldering temperature	T_{SLD}	255	°C
* Soldering time	t_{SLD}	10	S

Note: * mark is useful at SOP package

■ RECOMMENDED OPERATIONAL CONDITIONS

(V_{SS}=0V)

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Operating voltage	V_{DD}	4.0	5.0	6.0	V
Input voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating temperature	T_{OPR}	-40		+85	°C

■ ELECTRICAL CHARACTERISTICS

(V_{SS}=0V, Ta=-40 to 85°C, unless otherwise noted)

ITEM	SYMBOL	CONDITIONS			LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
H-level output voltage	V_{OH}	SM5610K, N	Q pin, Fig. 1	V_{DD}=4.5V. I_{OH}=16.0mA	3.9	4.2		V
				V_{DD}=4.0V. I_{OH}=14.4mA	3.4	3.7		
		SM5610H		V_{DD}=4.5V. I_{OL}=4.0mA	3.9	4.2		
				V_{DD}=4.0V. I_{OL}=3.6mA	3.4	3.7		
L-level output voltage	V_{OL}	SM5610K, N	Q pin, Fig. 1	V_{DD}=4.5V. I_{OH}=16.0mA		0.3	0.4	V
				V_{DD}=4.0V. I_{OH}=14.4mA		0.3	0.4	
		SM5610H		V_{DD}=4.5V. I_{OL}=4.0mA		0.3	0.5	
				V_{DD}=4.0V. I_{OL}=3.6mA		0.3	0.5	
Output leak current	I_Z	Q pin, Fig. 1, $\overline{INH}$="L", V_{DD}=6.0V		V_{OH}=V_{DD}			10	µA
				V_{OL}=V_{SS}			10	
H-level input voltage	V_{IH}	$\overline{INH}$ pin		V_{DD}=5±0.5V	2.0			V
				V_{DD}=5±1.0V	2.2			
L-level input voltage	V_{IL}	$\overline{INH}$ pin		V_{DD}=5±1.0V			0.8	V
Current consumption	I_{DD1}	Load circuit 1 (SM5610N, H) Load circuit 2 (SM5610K), Fig. 2, $\overline{INH}$=OPEN, CL=15pF		V_{DD}=5V, Ta=25°C		15	20	mA
				V_{DD}=5.5V			30	
				V_{DD}=6.0V			35	
	I_{DD2}	Load circuit 1 (SM5610N, H) Load circuit 2 (SM5610K), Fig. 2, $\overline{INH}$=OPEN, CL=50pF		V_{DD}=5V, Ta=25°C		21	26	
				V_{DD}=5.5V			36	
				V_{DD}=6.0V			41	
$\overline{INH}$ pin pull-up resistance	R_{UP}	Fig. 3			50		250	kΩ
Feedback resistance	R_f	Fig. 4		V_{DD}=5±0.5V	1.0		5.0	MΩ
				V_{DD}=5±1.0V	0.9		5.5	
Internal capacitor	C_G	Design value			19	27	35	pF
	C_D				19	27	35	

■ SWITCHING CHARACTERISTICS

1. K series

V_{SS} = 0V, Ta= -40 to +85°C unless otherwise noted.

ITEM	SYMBOL	CONDITIONS			LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Output rise time	T_{r1}	Load circuit 2, Fig. 2 0.4 to 2.4V	C_L=15pF	V_{DD}=5±0.5V		1.5	3.0	ns
				V_{DD}=5±1.0V			3.5	
	T_{r2}		C_L=50pF	V_{DD}=5±0.5V		3.0	6.0	
				V_{DD}=5±1.0V			7.0	
Output fall time	T_{f1}	Load circuit 2, Fig. 2 2.4V to 0.4V	C_L=15pF	V_{DD}=5±0.5V		1.5	3.0	ns
				V_{DD}=5±1.0V			3.5	
	T_{f2}		C_L=50pF	V_{DD}=5±0.5V		3.0	6.0	
				V_{DD}=5±1.0V			7.0	
Output duty cycle	DUTY	Load circuit 2, Fig. 2, C_L=15pF, Ta=25°C, V_{DD}=5.0V			45		55	%
Output disable delay time	T_{PLZ}	Fig. 2, Ta=25°C, V_{DD}=5±1.0V, Load C_L≤50pF					100	ns
Output enable delay time	T_{PZL}						100	
Maximum operating frequency	f_{MAX}	Load circuit 2, Fig. 2, V_{DD}=5±1.0V			30			MHz

2. H series

Vss = 0V, Ta= -40 to +85°C unless otherwise noted.

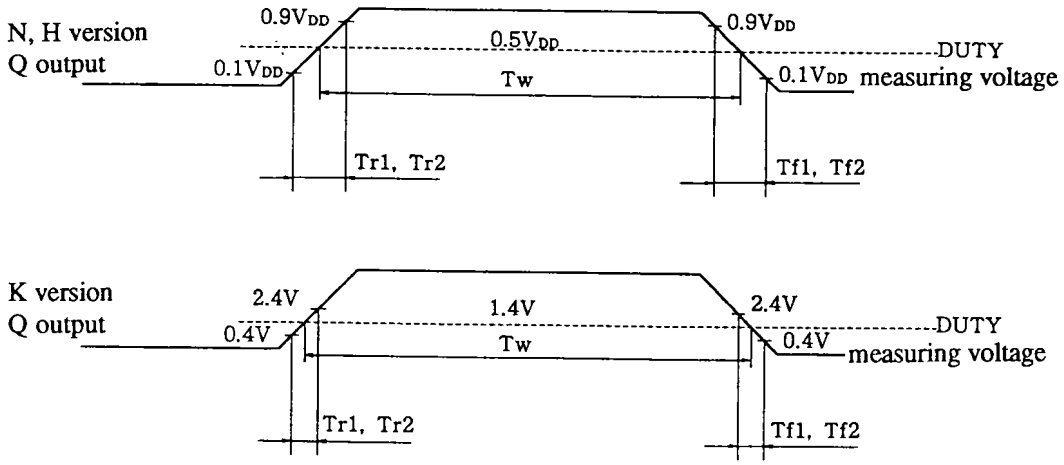
ITEM	SYMBOL	CONDITIONS			LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Output rise time	T_{r1}	Load circuit 1, Fig. 2 0.1V_{DD} to 0.9V_{DD}	C_L=15pF	V_{DD}=5±0.5V		5.0	10	ns
				V_{DD}=5±1.0V			12	
	T_{r2}		C_L=50pF	V_{DD}=5±0.5V		13	26	
				V_{DD}=5±1.0V			30	
Output fall time	T_{f1}	Load circuit 1, Fig. 2 0.9V_{DD} to 0.1V_{DD}	C_L=15pF	V_{DD}=5±0.5V		5.0	10	ns
				V_{DD}=5±1.0V			12	
	T_{f2}		C_L=50pF	V_{DD}=5±0.5V		13	26	
				V_{DD}=5±1.0V			30	
Output duty cycle	DUTY	Load circuit 1, Fig. 2, C_L=15pF, Ta=25°C, V_{DD}=5.0V			45		55	%
Output disable delay time	T_{PLZ}	Fig. 2, Ta=25°C, V_{DD}=5±1.0V, Load C_L≤50pF					100	ns
Output enable delay time	T_{PZL}						100	
Maximum operating frequency	f_{MAX}	Load circuit 1, Fig. 2, V_{DD}=5±1.0V			30			MHz

3. N series

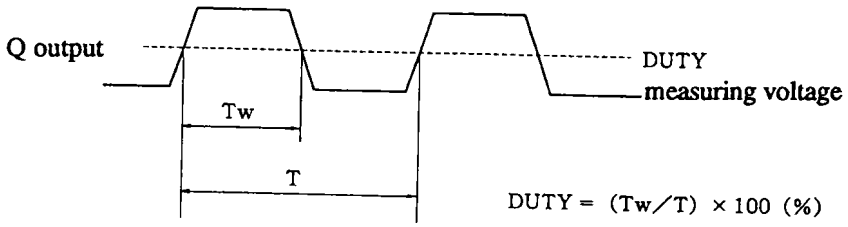
Vss = 0V, Ta= -40 to +85°C unless otherwise noted.

ITEM	SYMBOL	CONDITIONS			LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Output rise time	T_{r1}	Load circuit 1, Fig. 2 0.1V_{DD} to 0.9V_{DD}	C_L=15pF	V_{DD}=5±0.5V		1.5	3.0	ns
				V_{DD}=5±1.0V			3.5	
	T_{r2}		C_L=50pF	V_{DD}=5±0.5V		3.0	6.0	
				V_{DD}=5±1.0V			7.0	
Output fall time	T_{f1}	Load circuit 1, Fig. 2 0.9V_{DD} to 0.1V_{DD}	C_L=15pF	V_{DD}=5±0.5V		1.5	3.0	ns
				V_{DD}=5±1.0V			3.5	
	T_{f2}		C_L=50pF	V_{DD}=5±0.5V		3.0	6.0	
				V_{DD}=5±1.0V			7.0	
Output duty cycle	DUTY	Load circuit 1, Fig. 2, C_L=50pF, Ta=25°C, V_{DD}=5.0V			45		55	%
Output disable delay time	T_{PLZ}	Fig. 2, Ta=25°C, V_{DD}=5±1.0V, Load C_L≤50pF					100	ns
Output enable delay time	T_{PZL}						100	
Maximum operating frequency	f_{MAX}	Load circuit 1, Fig. 2, C_L=50pF, V_{DD}=5±1.0V			30			MHz

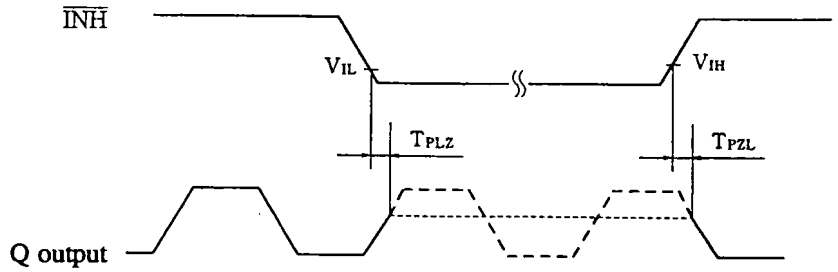
■ WAVEFORMS FOR SWITCHING TIME



■ DUTY FACTOR



■ OUTPUT DISABLE TIME



INH input waveform Tr = Tf 10 ns or less

■ FUNCTION

CONTROL	Output terminal
$\overline{INH}$	Q
H (OPEN)	Output ($f_o/f_o/2$; $f_o/4$ or $f_o/8$)
L	High impedance

f_o : Fundamental frequency