

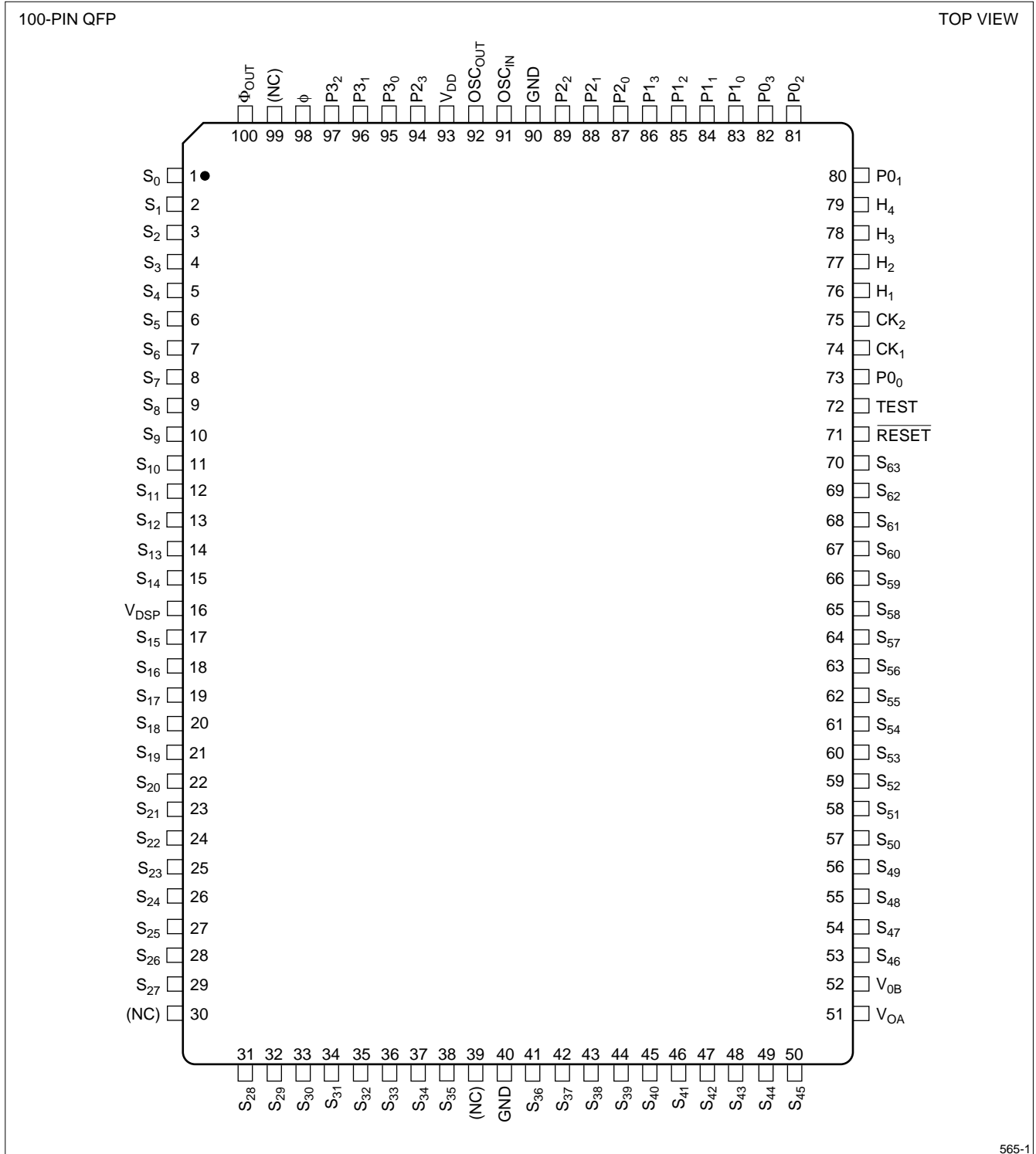
FEATURES

- 8,192 × 8-bits ROM Capacity
- 256 × 4-bits RAM Capacity (Including 64 × 4-bits Display RAM)
- 98 Instruction Sets
- A RAM Area is Used as Stack Area
- I/O Ports
 - 4 Input
 - 11 Input/Output (plus 16 Also Used as LCD Segment Port)
- Interrupts
 - Internal Interrupt × 4 (Timer/Counter, f4 Signal, Serial I/O, Divider Overflow)
 - External Interrupt × 1 (P0 Signal)
- Timer/Counter 8-bits × 1
- Serial Interface 8-bits × 1
- Built-in Main Clock Oscillator for System Clock
- Built-in Sub Clock Oscillator for Real Time Clock
- Built-in 15 Stages Divider for Real Time Clock
- Built-in LCD Driver
 - 256 Segments
 - 1/3 Bias
 - 1/4 Duty Cycle (If LCD Drive circuit is used, a crystal oscillator circuit needs to be constituted between OSC_{IN} and OSC_{OUT})
- Built-in Carrier Output Circuit for Remote Control
 - Carrier Frequency 37.9 kHz
 - Basic Oscillation Frequency (Main Clock) 455 kHz
 - 1/3 or 1/2 (Mask Option) Duty Cycle
 - Reversal Polarity (Mask Option)
- Instruction Cycle Time 8.79 μs (TYP., 455 kHz at 3 V)
- Buzzer Output
- Standby Function
- Supply Voltage 2.4 V to 5.5 V
- 100-pin QFP (QFP100-P-1420) Package

DESCRIPTION

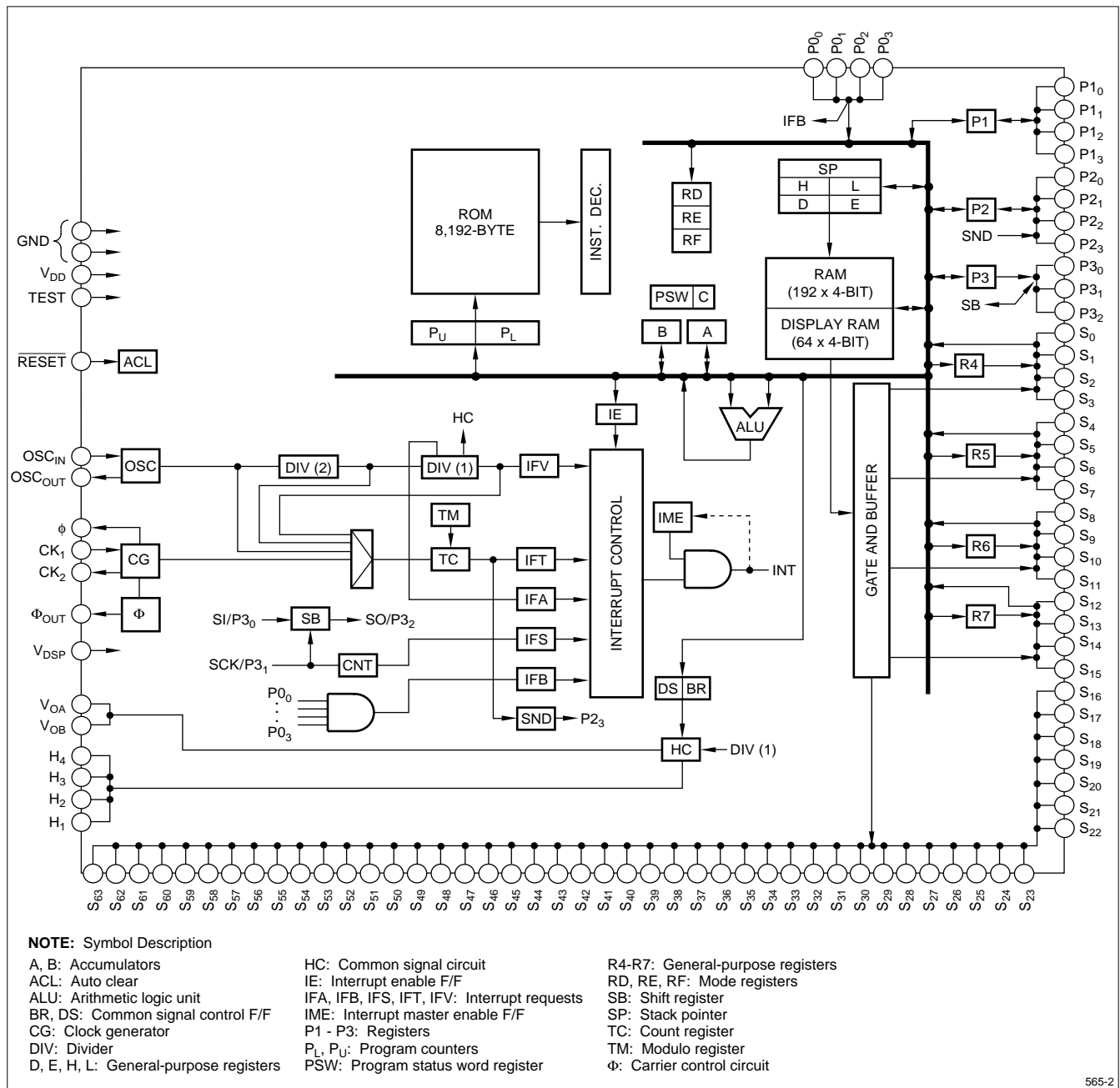
The SM565 is a CMOS 4-bit single-chip microcomputer incorporating carrier output circuit for remote control, ROM, RAM, I/O ports, serial interface and timer/counter. It provides five kinds of interrupts and subroutine stack function using the RAM area. Provided with a 256 segments LCD drive circuit, this microcomputer is applicable to a multi-functional AV remote control system, high performance hand-held LCD games or any other similar system with low power consumption.

PIN CONNECTIONS



565-1

Figure 1. 100-pin QFP



565-2

Figure 2. Block Diagram

PIN DESCRIPTION

PIN NAME	I/O	FUNCTION
P0 ₀ - P0 ₃	I	A _{CC} ← P0 ₀ - P0 ₃ , with pull-up resistor
P1 ₀ - P1 ₃	I/O	I/O selectable by instructions, with pull-up resistor
P2 ₀ - P2 ₃	I/O	I/O selectable independently, with pull-up resistor. Sound output only when P2 ₃ pin is used as an output
P3 ₀ - P3 ₂	I/O	Serial interface I/O by setting the mode register RE, with pull-up resistor
S ₀ - S ₁₅	O or I/O	Selectable between segment ports and I/O ports through an RC register
S ₁₆ - S ₆₃	O	Display RAM contents output as LCD segment signals
H ₁ - H ₄	O	4-value output capability; used for LCD common output
TEST	I	For test (connected to GND normally), with pull-down resistor
RESET	I	Auto clear, with pull-up resistor
φ	O	System clock output
Φ _{OUT}	O	Carrier output pin for remote control
CK ₁ , CK ₂		For system clock oscillation
OSC _{IN} , OSC _{OUT}		For clock oscillation
V _{DSP} , V _{OA} , V _{OB}		Power supply for LCD driver
V _{DD} , GND		Power supply for logic circuit

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply Voltage	V _{DD}	-0.3 to +7	V	1
	V _{DSP}	-0.3 to +7	V	1
Input Voltage	V _{IN}	-0.3 to V _{DD} + 0.3	V	1
Output Voltage	V _{OUT}	-0.3 to V _{DD} + 0.3	V	1
Output Current	I _{OUT}	20	mA	2
Operating Temperature	T _{OPR}	-20 to +70	°C	
Storage Temperature	T _{STG}	-55 to +150	°C	

NOTES:

1. The maximum applicable voltage on any pin with respect to GND.
2. Sum of current from (or flowing into) output pins.

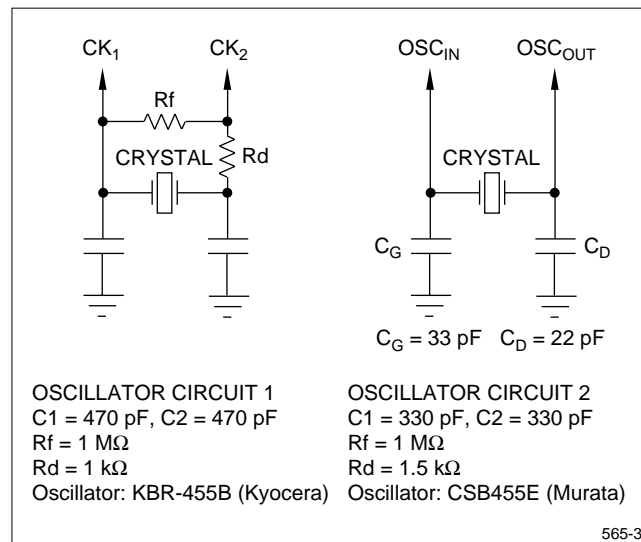
RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply Voltage	V_{DD}		2.4		5.5	V	
	V_{DSP}		2.4		V_{DD}	V	
Basic Oscillation Frequency	f			455		kHz	
Instruction Cycle	t			8.79		μ s	
Crystal Oscillation Frequency	f_{OSC}			32.768		kHz	1

NOTE:

- Starting condition: within 10 seconds after power on.

Oscillation Circuit



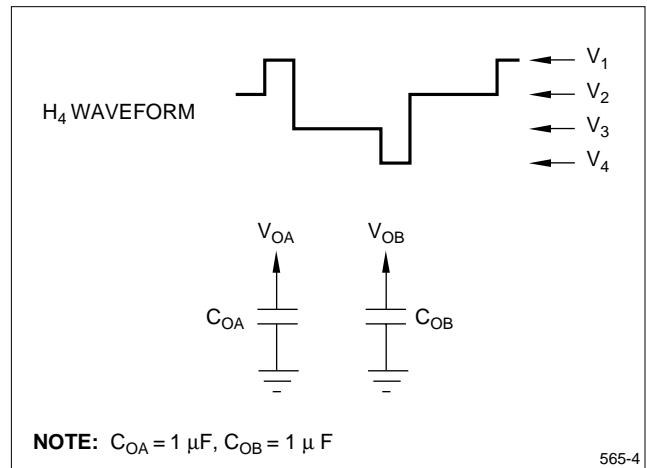
DC CHARACTERISTICS

 $V_{DD} = 2.4 \text{ V to } 5.5 \text{ V}, T_{OPR} = -20^{\circ}\text{C to } +70^{\circ}\text{C}$

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage	V_{IH1}		$0.7 \times V_{DD}$		V_{DD}	V	1
	V_{IL1}		0		$0.3 \times V_{DD}$	V	1
	V_{IH2}		$V_{DD} - 0.5$		V_{DD}	V	2
	V_{IL2}		0		0.5	V	2
Input Current	I_{IH}	$V_{IN} = 0 \text{ V},$	2		200	μA	1
Output Current	I_{OH1}	$V_{OH} = V_{DD} - 0.5 \text{ V}$	50			μA	3
	I_{OL1}	$V_{OL} = 0.5 \text{ V}$	250			μA	3
	I_{OH2}	$V_{OH} = V_{DD} - 0.5 \text{ V}$	50			μA	4
	I_{OH2D}	$V_{OH} = V_{DD} - 0.5 \text{ V}$	160			μA	5
	I_{OL2}	$V_{OL} = 0.5 \text{ V}$	500			μA	6
	I_{OH3}	$V_{OH} = V_{DD} - 0.5 \text{ V}$	20			μA	7
	I_{OH3D}	$V_{OH} = V_{DD} - 0.5 \text{ V}$	90			μA	8
Output Impedance	R_C			5	20	$\text{k}\Omega$	9
	R_S			10	40	$\text{k}\Omega$	10
Output Voltage	V_1	$V_{DSP} = 3.0 \text{ V}, \text{ No load}$	2.7		3	V	11
	V_2		1.7	2	2.3	V	11
	V_3		0.7	1	1.3	V	11
	V_4		0		0.3	V	11
Supply Current	I_{OP}	$f = 455 \text{ kHz}, V_{DD} = 3.0 \text{ V}$		160	320	μA	12
	I_{SB}	Standby current $V_{DSP} = 3.0 \text{ V}$		15	40	μA	13
		Standby current $V_{DD} = 3.0 \text{ V}$		8	20	μA	14

NOTES:

- Applicable pins: $P0_0 - P0_3, \overline{\text{RESET}}, P1_0 - P1_3, P2_0 - P2_3, P3_0 - P3_2$ (during input mode).
- Applicable pins: $CK_1, \text{TEST}, \text{OSC}_{IN}$.
- Applicable pin: CK_2 .
- Applicable pins: $P1_0 - P1_3, P2_0 - P2_2, P3_0 - P3_2$ (during output mode).
- Applicable pins: $P2_3, \Phi_{OUT}$ (during output mode).
- Applicable pins: $P1_0 - P1_3, P2_0 - P2_2, P3_0 - P3_2, \Phi_{OUT}$ (during output mode).
- Applicable pins: $S_0 - S_{15}$ (during data output mode).
- Pins cited in note 7 are applicable with mask option used.
- Applicable pins: $H_1 - H_4$.
- Applicable pins: $S_0 - S_{63}$ (during LCD output mode).
- Applicable pins: $H_1 - H_4, S_0 - S_{63}$ (during LCD output mode).
- No load condition
- No load condition when bleeder resistance is ON, $V_{DSP} = 3.0 \text{ V}$, during 32.768 kHz crystal oscillation.
- No load condition when bleeder resistance is OFF, during 32.768 kHz crystal oscillation.



PIN FUNCTIONS

GND, V_{DD}, V_{DSP} (Power Supply Inputs)

Both GND pins 40 and 90 should be grounded. The V_{DD} pin is the positive power supply with respect to GND. The V_{DSP} is the positive power supply for a LCD driver with respect to GND.

TEST (Test Input)

The TEST pin should be left open or connected to GND with a pull-down resistor.

RESET (Input)

The RESET pin accepts an active LOW system reset which initializes the internal logic of the device. Normally a capacitor of about 0.1 μ F is connected between this pin and GND to provide a power on reset function.

OSC_{IN}, OSC_{OUT} (Crystal Oscillator Pins)

The OSC_{IN} and OSC_{OUT} pins connect with an external crystal oscillator and these pins and the GND connect with a capacitor, which constitute an oscillator circuit.

The output of the oscillator is coupled to a clock divider for real-time clock operation.

CK₁, CK₂ (System Clock Oscillator Pins)

The CK₁ and CK₂ pins provide a system clock oscillator.

H₁ to H₄ (Common Signal Outputs)

The H₁ to H₄ pins are used to drive the common signal of a LCD.

S₀ to S₆₃ (Segment Outputs)

The S₀ to S₆₃ pins drive LCD segments. Pins S₀ through S₁₅ may also be used as I/O ports when specified with the mode register RC.

P0₀ to P0₃ (Inputs)

The P0 pins are normally used to accept key input data. A falling edge at these pins resets the IFB flag.

P1₀ to P1₃ (Input/Output)

The P1 pins are I/O pins connected to the positive supply with pull-up resistors. They may be switched between input and output modes through an instruction.

P2₀ to P2₃ (Input/Output)

The P2₀ to P2₃ pins are bit-independent I/O ports which can be independently set to input or output mode with the mode register RF.

When the P2₃ is used for an output pin, it serves exclusively as a sound output pin, which can output a sound signal with any frequency set up by the timer counter.

Pins P2₀ and P2₁ output the OD and R/W signals with the mode register RC.

P3₀ to P3₂ (Input/Output)

The P3₀ to P3₂ pins are I/O pins which are connected to the positive supply with pull-up resistors. These pins can be set to I/O mode for use in a serial interface with the mode register RE.

Φ_{OUT} (Carrier Output Pin for Remote Control)

A carrier signal output pin for remote control. It is used to control carrier signal output by setting the bits in the bit 3 of R7 register.

SYSTEM CONFIGURATION

ROM and Program Counter

The on-chip ROM has a configuration of 128-page × 64-step × 8-bit, and stores programs and table data.

The program counter consists of a 7-bit page address counter P_U and a 6-bit binary counter P_L used to specify the steps within a page.

The locations shown in Figure 3 are allocated in the on-chip ROM.

Stack Pointer (SP)

The stack pointer (SP) is an 8-bit shift register which holds the starting address of the stack area of RAM space. Immediately after the reset, the contents of the stack pointer are uninitialized and must be set to an appropriate value. If, for instance, the initial value of the stack pointer is set to 80_H , the data memory is beginning with the highest address (excluding the display RAM area). $7F_H$ is usable as a stack area.

RAM

Data memory has a 256-word × 4-bit configuration, and is used to store processing data and other information. Data memory is also used as a stack area to save register values, the program counter value and program status word (PSW) at the time a subroutine jump or an interrupt occurs. Figure 4 shows the RAM configuration. 64×4 -bit of entire RAM space is used as a display RAM area from which data is output to LCD segment driving pins. A LCD with a 1/4 duty and 1/3 bias format can be directly driven by writing display data into the display RAM area. The display RAM outputs are, as shown in Figure 5, connected to segment output pins S_0 to S_{63} for individual set of common outputs H_1 to H_4 . The segment output pins provide a single digit of display RAM data M_0 to M_3 , as a LCD driving waveform signal according to H_1 to H_4 outputs. The operations of the display RAM are identical to those of other RAM areas.

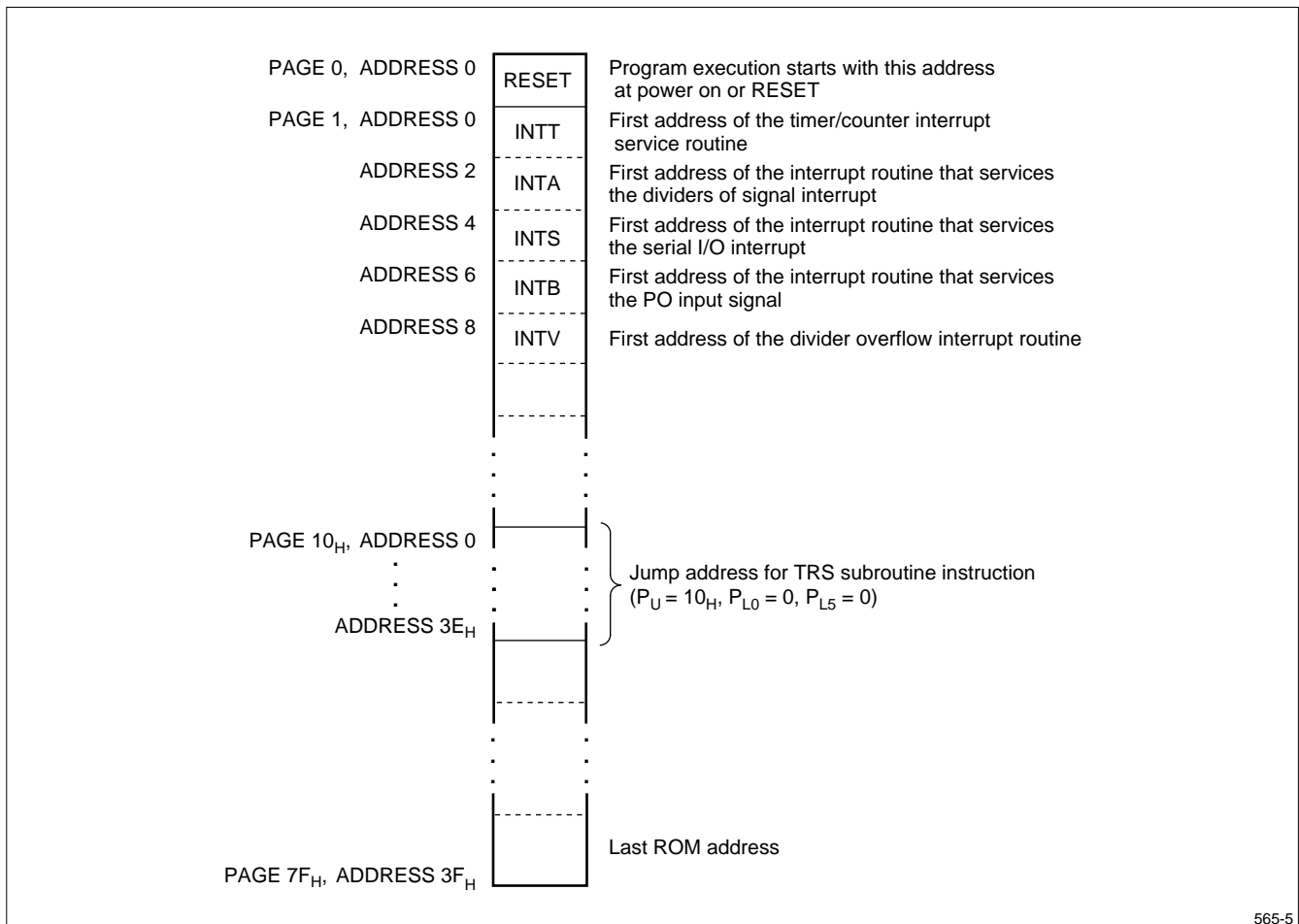


Figure 3. Program ROM Map

565-5

HIGHER ADDRESS H LOWER ADDRESS L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0													S ₀	S ₁₆	S ₃₂	S ₄₈
1													S ₁	S ₁₇	S ₃₃	S ₄₉
2													S ₂	S ₁₈	S ₃₄	S ₅₀
3													S ₃	S ₁₉	S ₃₅	S ₅₁
4													S ₄	S ₂₀	S ₃₆	S ₅₂
5													S ₅	S ₂₁	S ₃₇	S ₅₃
6													S ₆	S ₂₂	S ₃₈	S ₅₄
7													S ₇	S ₂₃	S ₃₉	S ₅₅
8													S ₈	S ₂₄	S ₄₀	S ₅₆
9													S ₉	S ₂₅	S ₄₁	S ₅₇
A													S ₁₀	S ₂₆	S ₄₂	S ₅₈
B													S ₁₁	S ₂₇	S ₄₃	S ₅₉
C													S ₁₂	S ₂₈	S ₄₄	S ₆₀
D													S ₁₃	S ₂₉	S ₄₅	S ₆₁
E													S ₁₄	S ₃₀	S ₄₆	S ₆₂
F													S ₁₅	S ₃₁	S ₄₇	S ₆₃

NOTE: The area with the thick is allocated for a display RAM and the S_n (n = 0 to 63) shows the related segment outputs.

Figure 4. RAM Configuration

Accumulator (A), Subaccumulator (B) and Arithmetic and Logic Unit (ALU)

The accumulator (A) is a 4-bit working register which is the nucleus of the single chip system. It holds the results of operations and transfers data to memory, I/O ports and registers.

A subaccumulator (B) is another 4-bit register. It is used as one of the general purpose registers, and when combined with the A to form a B-A register pair allows data transfer on an 8-bit basis.

The arithmetic and logic unit (ALU) performs, in conjunction with a carry flag (C), binary addition, shift operations and logical operations such as AND, OR, EX-OR and complement.

General Purpose Registers (H, L, D, E)

Registers H and L are 4-bit general purpose registers. They can transfer and compare data with the A on a 4-bit basis. Registers D and E are 4-bit registers and can transfer data with the H and L registers on an 8-bit basis. The H and L as well as the D and E registers can be combined into 8-bit register pairs, and can be used as pointers to data memory locations. The L register can be increment or decremented and is used to access I/O ports and mode registers.

Clock Divider, IFV Flag, IFA Flag

The device contains a crystal oscillator and a 15-stage divider as shown in Figure 6. A real-time clock can be provided by connecting an external crystal oscillator between the oscillator pins. When an external 32.768 kHz crystal oscillator is used, the f_0 signal is a frequency of 1 Hz.

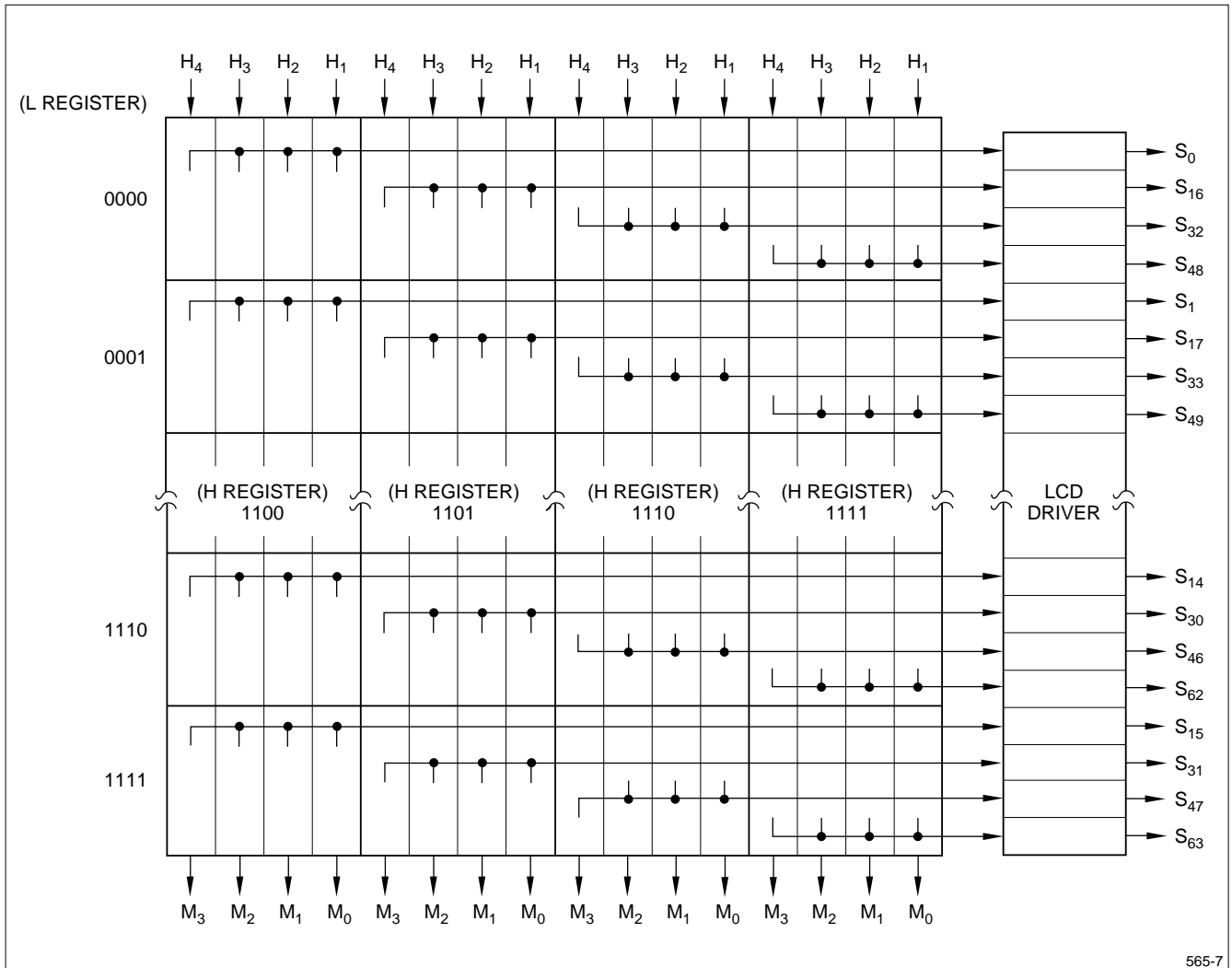


Figure 5. Display RAM and Its LCD Segment Outputs

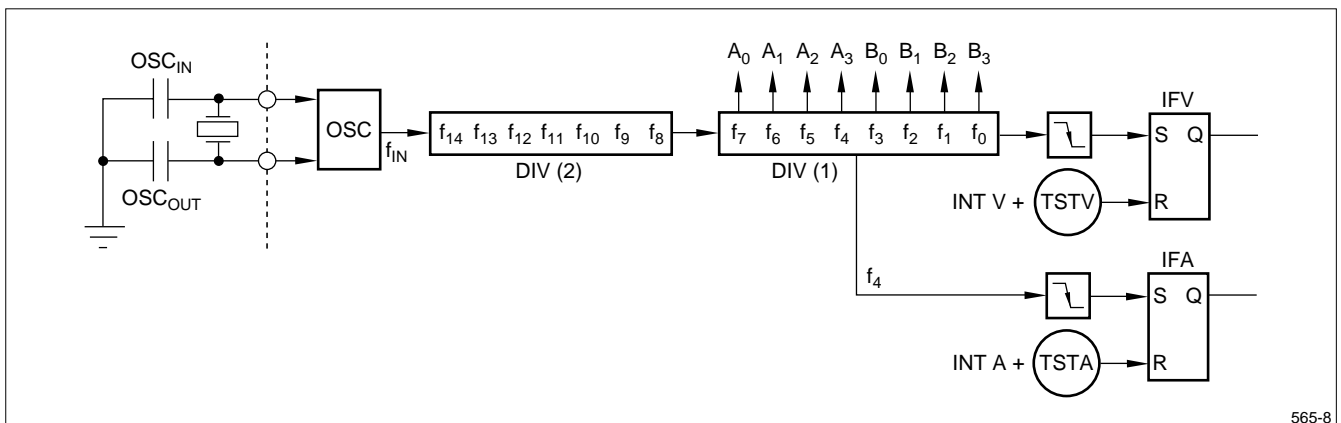


Figure 6. Real-Time Clock Divider

Timer/Counter and the SND Signal

The timer/counter consists of an 8-bit count register (TC) and an 8-bit modulo register (TM).

The count register is an 8-bit incremental binary counter. It is incremented by one at the falling edge of its count pulse (CP) input. If the count register overflows, the timer interrupt request flag IFT is set, and the contents of the modulo register (TM) are loaded into the count register (see Figure 7).

The count pulse Cp can be selected from divider signals f_{1n} and f_0 , and the system clock, by using the mode register RD. If the count register (TC) overflows, the SND flag reverses its status at the falling edge of the TC. A sound signal can be obtained at the TC output by putting P2 in output mode and sending a '1' to pin P2₃ (see Figure 8).

Serial Interface and IFS

The serial interface consists of an 8-bit shift register (SB) and a 3-bit counter, which is used to input and output the serial data. The serial clock can be selected with either an internal clock (system clock) or an external clock.

In serial shift operations, the highest bit data of the shift register (SB) is output from the SO pin, and the data input from the SI pin at the rising edge of a serial clock is loaded into the lowest bit of the shift register. When the internal clock is used, immediately after the SIO instruction is executed, the serial operation begins and stops with eight clocks which are output from the SCK pin.

Upon completion of an 8-bit shift operation, the serial I/O ending flag IFS is set each time a 3-bit counter overflows, and an interrupt request occurs.

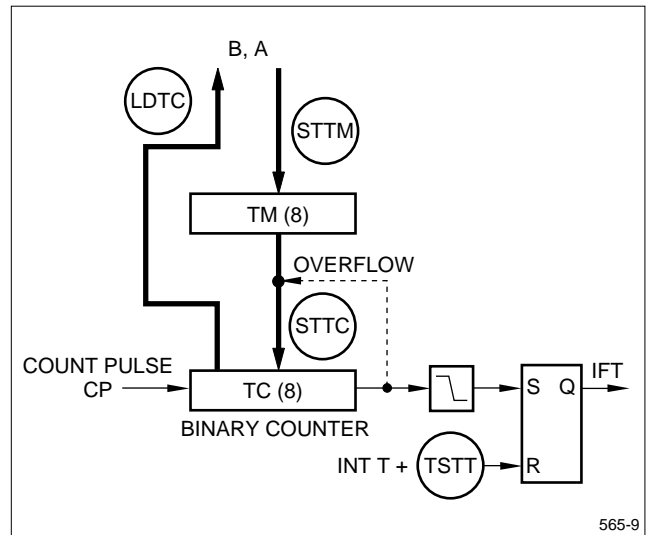


Figure 7. Timer/Counter

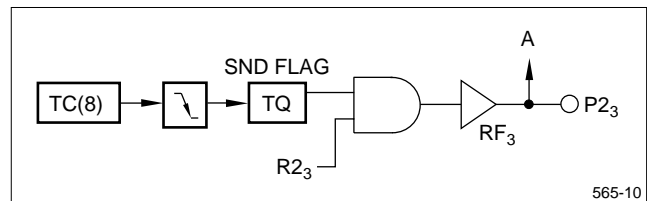


Figure 8. SND Signal

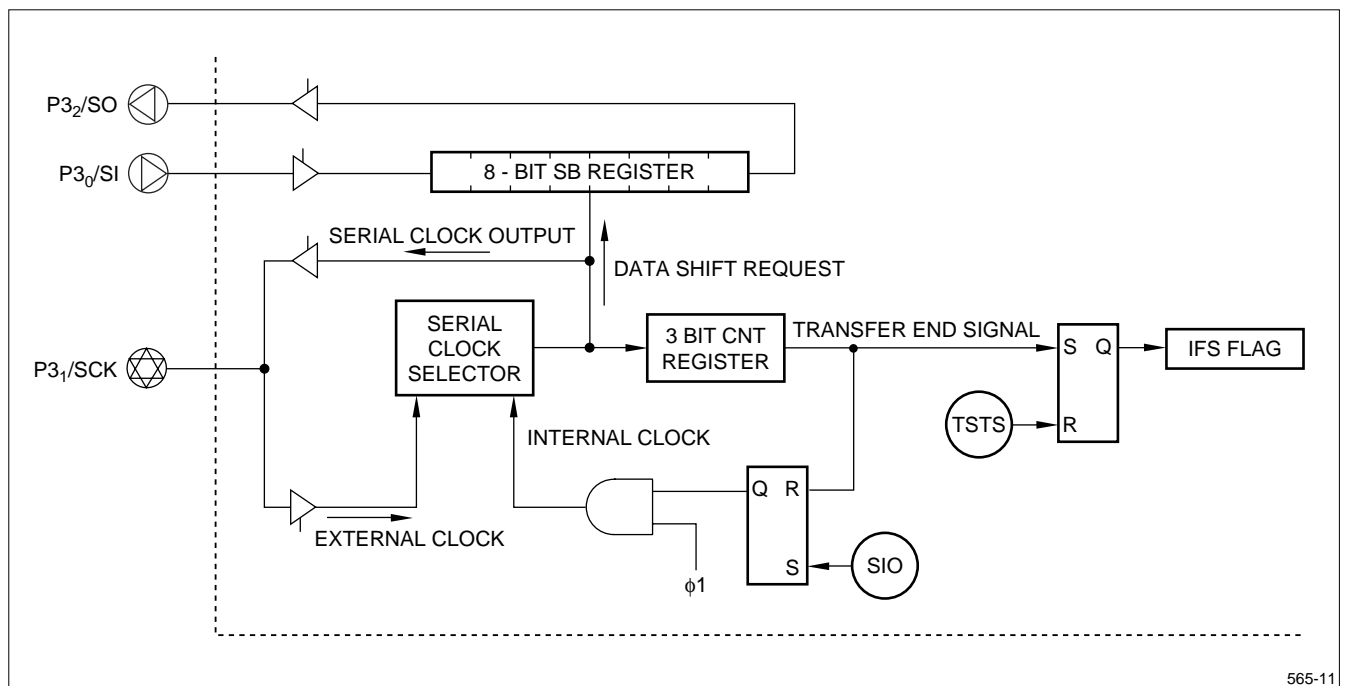


Figure 9. Serial Interface

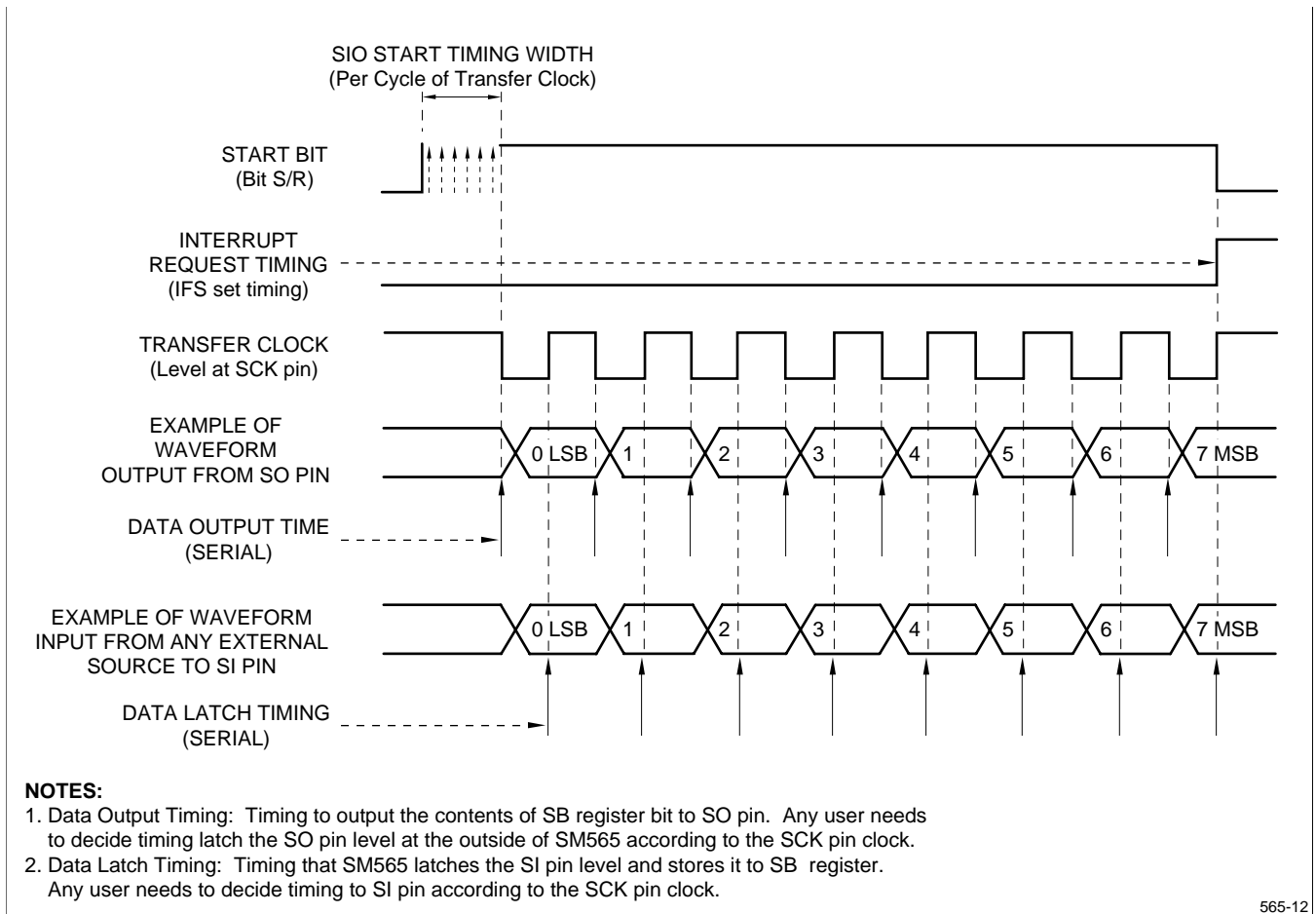


Figure 10. Serial Interface Timing

Input Port P0 and IFB Flag

The IFB flag is set at the falling edge of the signal applied to the input port P0 by which the interrupt is enabled.

When port P0 is used as a key input, it can cause an interrupt each time a key is operated.

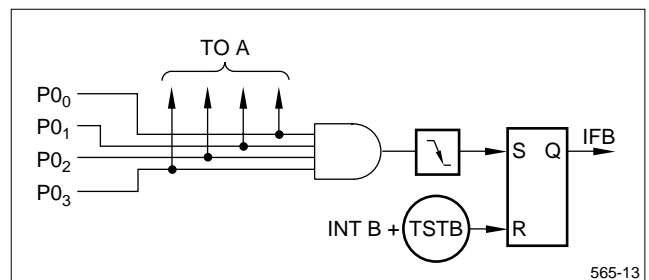


Figure 11. P0 Port

Interrupts

When an interrupt occurs, the corresponding interrupt request flag is set. The CPU acknowledges the interrupt if it is enabled (master interrupt enable flag and the corresponding interrupt enable flag are set). If more than one interrupt occurs simultaneously, all of the corresponding interrupt request flags will be set, but the CPU will only acknowledge that interrupt with the highest priority and other interrupts will be queued.

I/O Ports

Port P0 is a 4-bit parallel input port. The IFB flag is set at the falling edge of this port.

Port P1 can be switched between input and output modes, 4-bits at a time.

Each bit of port P2 can be independently placed in input or output mode by setting the corresponding bit of mode register RF.

Ports P₂₀ and P₂₁ can output the OD and R/W signals, respectively. In those cases, these pins should be kept HIGH in an output mode. Port P₂₃ outputs the SND signal in the output mode.

Port P3 is a 4-bit I/O port which can be placed in input or output mode, 3-bits at a time. Each bit of port P3 can be set to the I/O modes (SI, SO, SCK) of a serial interface.

Ports P1 and P3 are placed in an output mode when a port output instruction is executed, and in an input mode when a port input instruction is executed. After an ACL operation, ports P1, P2, and P3 are all placed in an input mode.

Every input port has pull-up resistors. (Pull-up resistors for I/O ports are effective only when the ports are placed in an input mode.)

Ports P1 through P3 in an output mode can be independently set or reset by instructions.

When a key-matrix is configured by using I/O ports, a short on the output pins may be caused by a multiple key depression. To prevent this from occurring, port P1 should be used an output.

Standby Mode

Executing the CEND instruction places the device in standby mode. To reduce power consumption, the system clock is inactivated. Standby mode may be cleared with the interrupt request or the RESET signal.

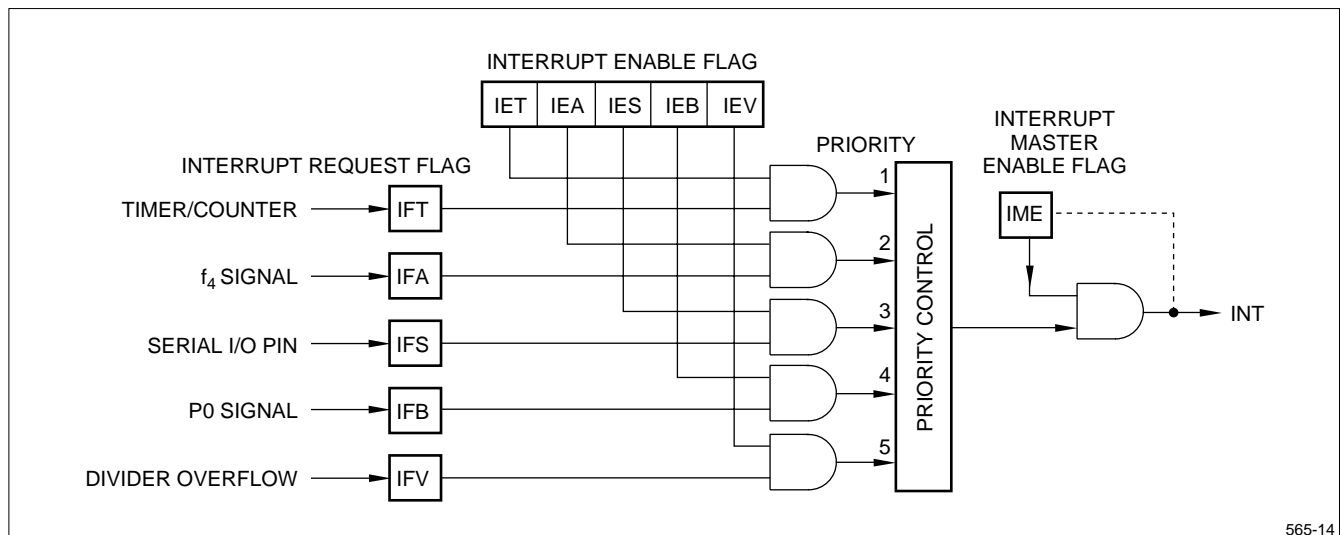


Figure 12. Interrupt Handling

Table 1. Characteristics of I/O Ports and Registers

PORT	FUNCTION	DIRECT 4-BIT PARALLEL I/O		IN, OUT INSTRUCTION		BIT INDEPENDENT SP _n OUTPUT
		INPUT (INA)	OUTPUT (OUTA)	INPUT (IN)	OUTPUT (OUT)	DIRECT PIN-INDEPENDENT OUTPUT RP _n
P0	Input-only port	O	X	O	X	X
P1	I/O port	O	O	X	O	O
P2	I/O port, P ₂₃ sound output	O	O	X	X	O
P3	P ₃₀ - SI, P ₃₁ - SCK, P ₃₂ - SO, multi-control port	O	O	X	X	O

NOTE: O = yes, X = no.

Reset Function (ACL)

Applying a LOW level signal to the $\overline{\text{RESET}}$ pin resets the internal logic of the device and applying a HIGH level signal starts execution of the program at address 0, page 0. Once the device is reset, all I/O ports are placed in input mode, all interrupts are disabled, and the LCD display turns off. The device is also reset when it is powered up.

Main Clock Oscillation Circuit

The main clock oscillator requires an external resistor across pins CK_1 and CK_2 . Instead of using on-chip oscillator, an external clock may be applied to pin CK_1 . In this case, pin CK_2 should be left open. The system clock ϕ is a divided clock equivalent to 1/4 of the clock applied to pin CK_1 .

LCD Driver

Display Segment

The SM565 contains an on-chip LCD driver which can directly drive an LCD with a 1/4 duty and 1/3 bias. Figure 15 shows an example of LCD segment configuration for 1/4 duty.

Each segment of the LCD can be turned on or off by software control of the setting of the corresponding bit '1' or '0' in the display RAM area (see Figure 4).

The LCD digit may have any shape, provided that the maximum number of segments does not exceed 256 (see Figure 15). Figure 14 shows an example of a 7-segment numeric LCD digit.

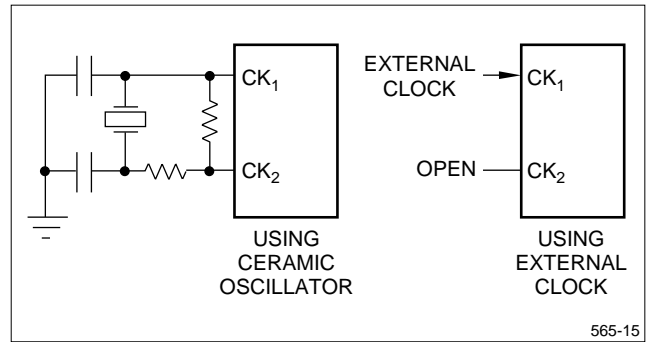


Figure 13. CK_2 Main Clock Sources

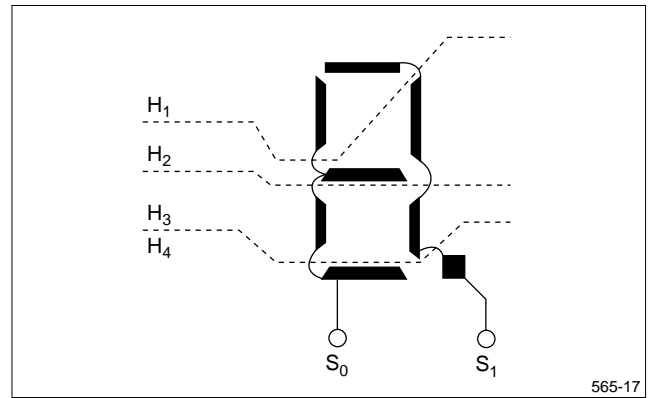


Figure 14. 7-Segment Numeric LCD Digit

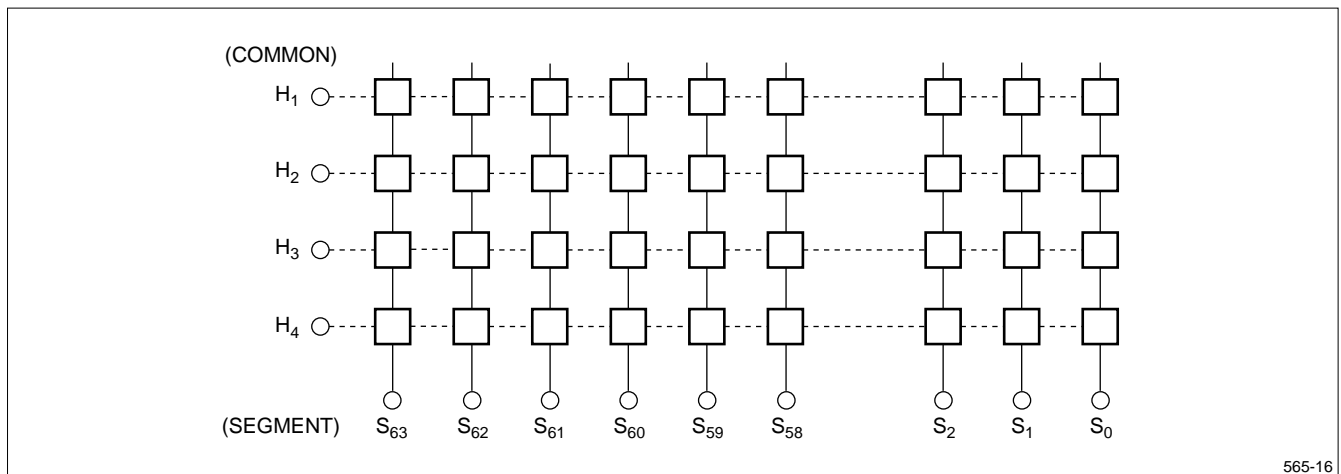


Figure 15. LCD Segment Configuration for 1/4 Duty

LCD Driving Signal Waveform

Figure 16 shows the LCD signal driving waveforms required to display the number '5' on the 7-segment display shown in Figure 14 (segment outputs S_0 and S_1 are used). A voltage of 3 V is applied to pin V_{DSP} in Figure 16. The frame frequency ($1/T$) can be selected from 64 Hz or 128 Hz by mask options.

V_{OA} and V_{OB}

The device contains bleeder resistors to allow 1/3 bias driving. When V_{DSP} is 3 V, voltages of 2 V and 1 V are output from pins V_{OA} and V_{OB} respectively. Normally pins V_{OA} and V_{OB} are left open. When a LCD with a large display area is driven, connect capacitors across pins V_{OA} and V_{DSP} , and across V_{OB} and V_{DSP} to improve the rise time of the LCD driving signal.

Remote Control Carrier Output Function

SM565 has a carrier output function for remote control output. A carrier is output from Φ_{OUT} , and controlled using the register R73. Setting '0' in the bit of R73 causes the output from Φ_{OUT} to be set constant HIGH output. If '1' is set, a carrier, which is a remote control signal, is output. If '0' is set in the bit of R73, the output level is set constant HIGH as stated above. However, it can be set to constant LOW level using the mask option.

Either 1/2 or 1/3 can be selected as the duty of the carrier. (See Table 2 and Figure 17.)

The frequency of the carrier is approximately 37.9 kHz (1/2 duty or 1/3 duty) when the basic oscillation frequency (main clock) is 455 kHz.

Figure 18 shows an example of a circuit that converts remote control carrier signal from the Φ_{OUT} pin into infrared signal.

Table 2. Mask Option for Φ_{OUT} Pin Output

Selection of PLA		Φ_{OUT} OUTPUT	
PLA1	PLA2	Output Waveform	When Remote Control Signal is Not Output
1	1	A	Constant LOW output
2	1	B	Constant LOW output
1	2	\bar{A}	Constant HIGH output
2	2	\bar{B}	Constant HIGH output

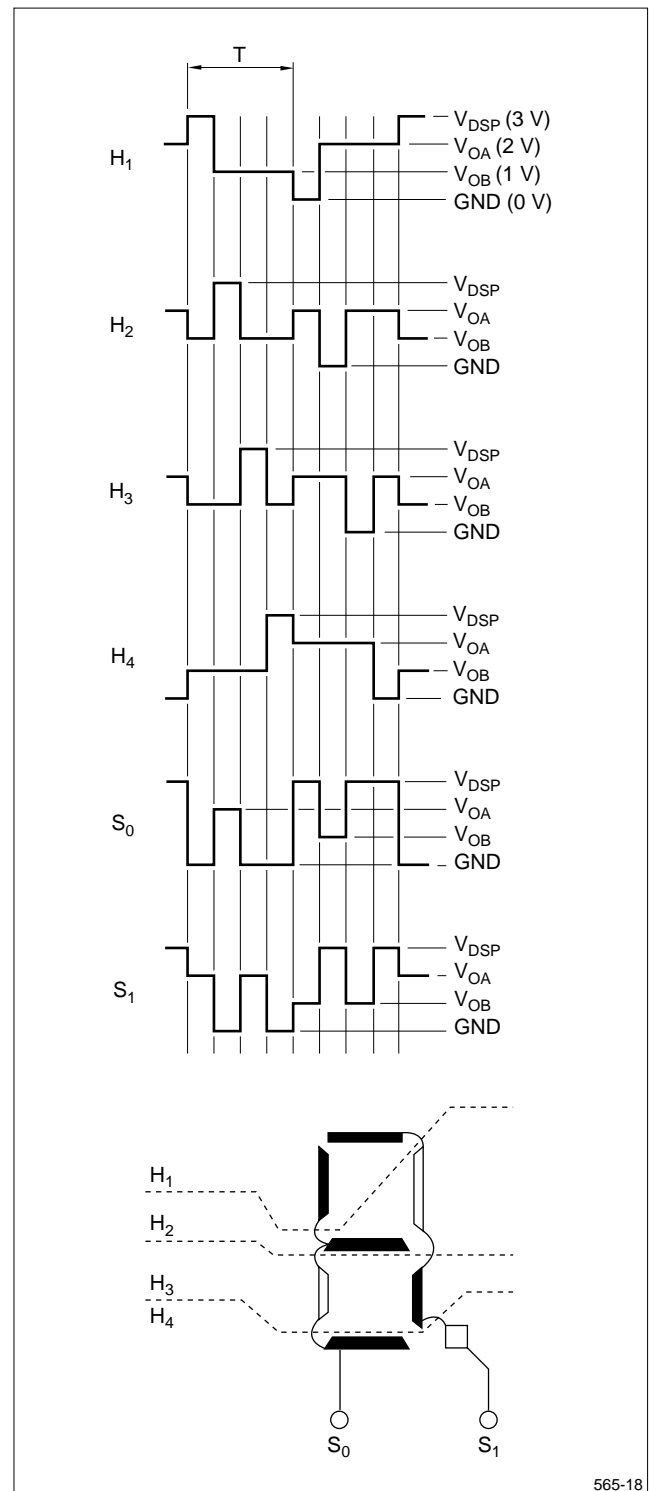


Figure 16. LCD Driving Signal Waveform (Required to Display the Number 5)

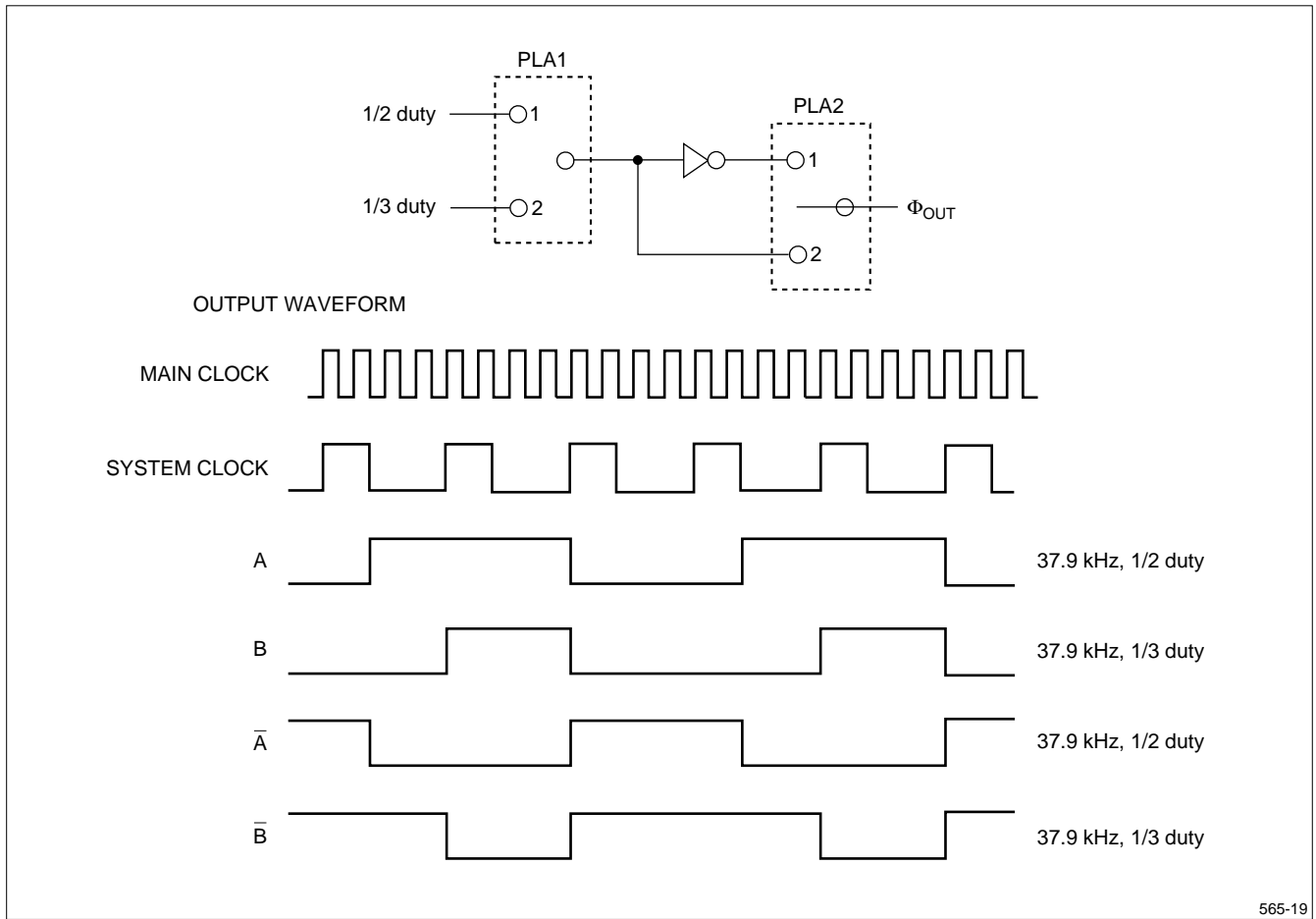


Figure 17. Mask Option for Φ_{OUT} Output

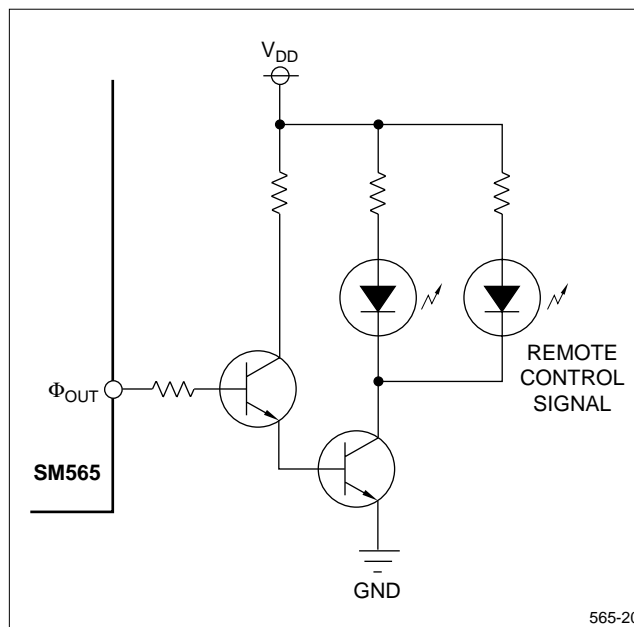


Figure 18. Remote Control Signal Output Circuit

INSTRUCTION SET

ROM Address Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
TR x	80 - BF	$P_L \leftarrow x (I_5 - I_0)$
TL xy (2-byte)	C0 - DF 00 - FF	$P_U \leftarrow x (I_{12} - I_6)$ $P_L \leftarrow y (I_5 - I_0)$
TRS x	E0 - EF	$(SP - 1) - (SP - 4) \leftarrow PC$ $SP \leftarrow SP - 4$ $P_U \leftarrow 10_H$ $P_L \leftarrow x (0, I_3, I_2, I_1, I_0, 0)$
CALL xy (2-byte)	F0 - FF 00 - FF	$(SP - 1) - (SP - 4) \leftarrow PC$ $SP \leftarrow SP - 4, P_U \leftarrow x (I_{11} - I_6)$ $P_L \leftarrow y (I_5 - I_0)$
JBA x (2-byte)	7F 20 - 3F	$P_{U5}, - P_{U2} \leftarrow x (I_3 - I_0)$ $P_{U1}, P_{U0}, P_{L5}, P_{L4} \leftarrow B$ $P_{L3} - P_{L0} \leftarrow A$
RTN	61	$P_U, P_L \leftarrow (SP), (SP + 1), (SP + 2)$
RTNS	62	$P_U, P_L \leftarrow (SP), (SP + 1), (SP + 2),$ $SP \leftarrow SP + 4$
RTNI	63	$P_U, P_L \leftarrow (SP), (SP + 1), (SP + 2),$ $PSW \leftarrow (SP + 3), SP \leftarrow SP + 4$ $IME \leftarrow 1$

RAM Address Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
STL	69	$L \leftarrow A$
STH	68	$H \leftarrow A$
EXHD	3F	$H \leftrightarrow D, L \leftrightarrow E$
LIHL xy (2-byte)	3D 00 - FF	$H \leftarrow (I_7 - I_4), L \leftarrow y (I_3 - I_0)$

Bit Manipulation Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
SM x	40 - 43	$(HL) x \leftarrow 1$
RM x	44 - 47	$(HL) x \leftarrow 0$
RC	26	$C \leftarrow 0$
SC	27	$C \leftarrow 1$
RIME	3A	$IME \leftarrow 0$
SIME	3B	$IME \leftarrow 1$
DI x (2-byte)	7F C0 - DF	$IEF \leftarrow IEF \cap x$
EI x (2-byte)	7F E0 - FF	$IEF \cup x$

Data Transfer Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
EX pr	5C - 5F	$A \leftrightarrow (pr)$
LDX adr (2-byte)	7D 00 - FF	$A \leftarrow (adr)$
STX adr (2-byte)	7E 00 - FF	$(adr) \leftarrow A$
EXX adr (2-byte)	7C 00 - FF	$A \leftrightarrow (adr)$
LAX x	10 - 1F	$A \leftarrow x (I_3 - I_0)$
LIBA xy (2-byte)	3C 00 - FF	$B \leftarrow x (I_7 - I_4)$ $A \leftarrow y (I_3 - I_0)$
LBAT	60	$B \leftarrow ROM (P_{U5} - P_{U2}, B, A)_H$ $A \leftarrow ROM (P_{U5} - P_{U2}, B, A)_L$
LDL	65	$A \leftarrow L$
LD pr	54 - 57	$A \leftarrow (pr)$
ST pr	58 - 5B	$(pr) \leftarrow A$
EXH	6C	$A \leftrightarrow H$
EXL	6D	$A \leftrightarrow L$
EXB	6E	$A \leftrightarrow B$
STB	6A	$B \leftarrow A$
LDB	66	$A \leftarrow B$
LDH	64	$A \leftarrow H$
PSHBA	28	$(SP - 1) \leftarrow B, (SP - 2) \leftarrow A,$ $SP \leftarrow SP - 2$
PSHHL	29	$(SP - 1) \leftarrow H, (SP - 2) \leftarrow L,$ $SP \leftarrow SP - 2$
POPBA	38	$B \leftarrow (SP + 1), A \leftarrow (SP),$ $SP \leftarrow SP + 2$
POPHL	39	$H \leftarrow (SP + 1), L \leftarrow (SP),$ $SP \leftarrow SP + 2$
STSB	70	$SB_H \leftarrow B, SB_L \leftarrow A$
STSP	71	$SP_H \leftarrow B, SP_L \leftarrow A$
STTC	72	$TC \leftarrow TM$
STTM	73	$TM_H \leftarrow B, TM_L \leftarrow A$
LDSB	74	$B \leftarrow SB_H, A \leftarrow SB_L$
LDSP	75	$B \leftarrow SP_H, A \leftarrow SP_L$
LDTTC	76	$B \leftarrow TC_H, A \leftarrow TC_L$
LDDIV	77	$B \leftarrow DIV_H, A \leftarrow DIV_L$

Arithmetic Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
ADX x	00 - 0F	$A \leftarrow A + x (I_3 - I_0)$, Skip if $C_Y = 1$
ADD	36	$A \leftarrow A + (HL)$
ADDC	37	$A \leftarrow A + (HL) + C$, $C \leftarrow C_Y$ Skip if $C_Y = 1$
OR	31	$A \leftarrow A \cup (HL)$
AND	32	$A \leftarrow A \cap (HL)$
EOR	33	$A \leftarrow A \oplus (HL)$
ANDB	22	$A \leftarrow A \cap B$
ORB	21	$A \leftarrow A \cup B$
EORB	23	$A \leftarrow A \oplus B$
COMA	6F	$A \leftarrow \bar{A}$
ROTR	25	$C \rightarrow A_3 \rightarrow A_2 \rightarrow A_1 \rightarrow A_0 \rightarrow C$
ROTL	35	$C \leftarrow A_3 \leftarrow A_2 \leftarrow A_1 \leftarrow A_0 \leftarrow C$
INCB	52	$B \leftarrow B + 1$, Skip if $B = F_H$
DECB	53	$B \leftarrow B - 1$, Skip if $B = 0$
INCL	50	$L \leftarrow L + 1$, Skip if $L = F_H$
DECL	51	$L \leftarrow L - 1$, Skip if $L = 0$
DECM adr	79 00 - FF	$(adr) \leftarrow (adr) - 1$, Skip if $(adr) = 0$
INCM adr	78 00 - FF	$(adr) \leftarrow (adr) + 1$, Skip if $(adr) = F_H$

Test Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
TAM	30	Skip if $A = (HL)$
TAH	24	Skip if $A = H$
TAL	34	Skip if $A = L$
TAB	20	Skip if $A = B$
TC	2A	Skip if $C = 0$
TM x	48 - 4B	Skip if (HL) , $x = 1$
TA x	4C - 4F	Skip if $A_x = 1$
TSTT	2B	Skip if $IFT = 1$, $IFT \leftarrow 0$
TSTA	2C	Skip if $IFA = 1$, $IFA \leftarrow 0$
TSTS	2D	Skip if $IFS = 1$, $IFS \leftarrow 0$
TSTB	2E	Skip if $IFB = 1$, $IFB \leftarrow 0$
TSTV	2F	Skip if $IFV = 1$, $IFV \leftarrow 0$

Special Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
SIO	3E	Serial I/O start
IDIV (2-byte)	7F 10	$DIV \leftarrow 0$
SKIP	00	No operation
CEND (2-byte)	7F 00	Stop system clock

NOTE: The machine code consists of 8-bits including I_7 , I_6 , I_5 , I_4 , I_3 , I_2 , I_1 , and I_0 .

I/O Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
IN	67	$A \leftarrow P_0$
OUT	6B	$P_1 \leftarrow A$
INA x (2-byte)	7F A0 - A9	$A \leftarrow P(x)$, $R(x)$
OUTA (2-byte)	7F B0 - BF	$P(x)$, $R(x) \leftarrow A$
INBA x	7F 80 - 82	$B \leftarrow R(x+1)$ $A \leftarrow R(x)$
OUTBA x (2-byte)	7F 90 - 91	$R(x+1) \leftarrow B$ $R(x) \leftarrow A$
SP xy (2-byte)	7A 00 - F3	$P(y) \leftarrow P(y) \times$
BP xy (2-byte)	7B 00 - F3	$P(y) \leftarrow P(y) \times$
RDS (2-byte)	7F 60	$DS \leftarrow 0$
RBR (2-byte)	7F 70	$BR \leftarrow 0$
SDS (2-byte)	7F 61	$DS \leftarrow 1$
SBR (2-byte)	7F71	$BR \leftarrow 0$
READ (2-byte)	7F 62	$A \leftarrow P_4$ with OD
WRIT (2-byte)	7F 72	$P_4 \leftarrow A$ with R/W
READB (2-byte)	7F 63	$A \leftarrow P_4$, with OD $B \leftarrow P_5$
WRITB (2-byte)	7F 73	$P_4 \leftarrow A$, with R/W $P_5 \leftarrow B$

SYSTEM CONFIGURATION EXAMPLE

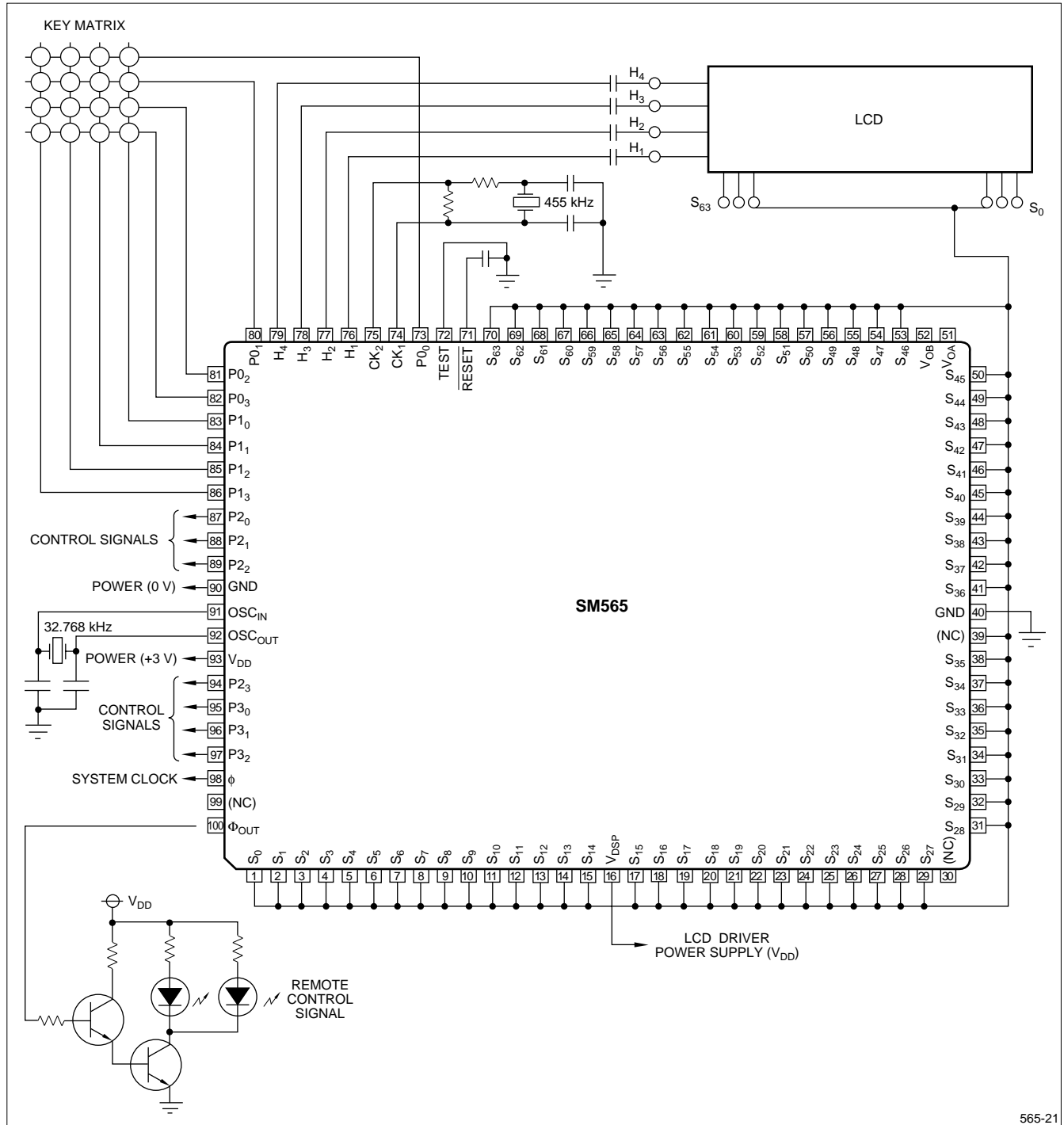


Figure 19. Example of an Infrared Remote Control

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