NIPPON PRECISION CIRCUITS INC.

SM5839A

High-Speed Variable-Length Shift Register

OVERVIEW

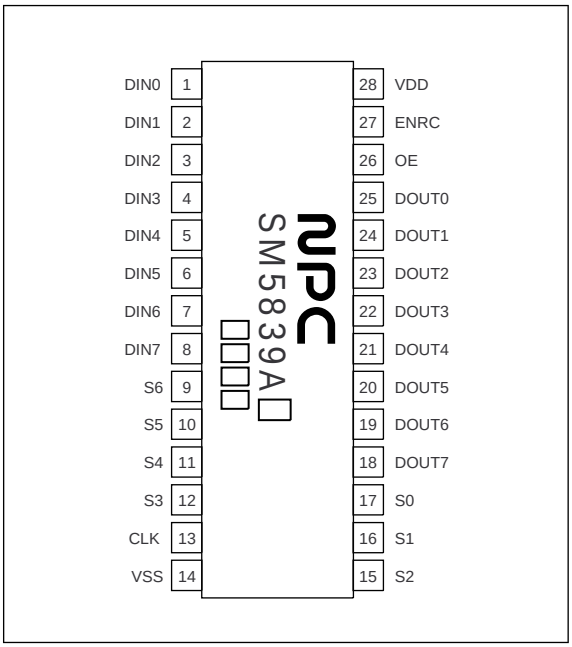
The SM5839A is an 8-bit variable-length shift resister. The input pins can be configured to function as a 2 to 128-step shift resister. The shift clock has a maximum frequency of 54 MHz, making it ideal for high-speed digital signal processing.

FEATURES

- 2 to 128-step selectable variable-length shift resister
- Static circuitry
- 8-bit (byte) word length
- Selectable circulating/non-circulating storage
- 54 MHz maximum operating clock frequency (standard-voltage specification)
- Supply voltage
  - 5.0 ± 0.5 V (standard-voltage specification)
  - 2.7 to 4.5 V (low-voltage specification)
- TTL-compatible input/outputs
- Molybdenum-gate CMOS
- Package
  - 28-pin DIP (SM5839AP)
  - 28-pin VSOP (SM5839AV)

PINOUT

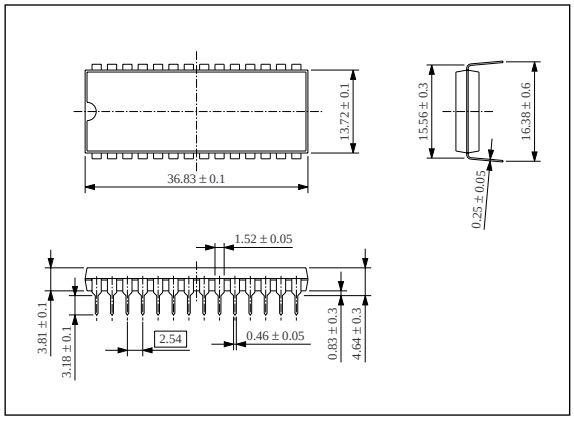
Top view



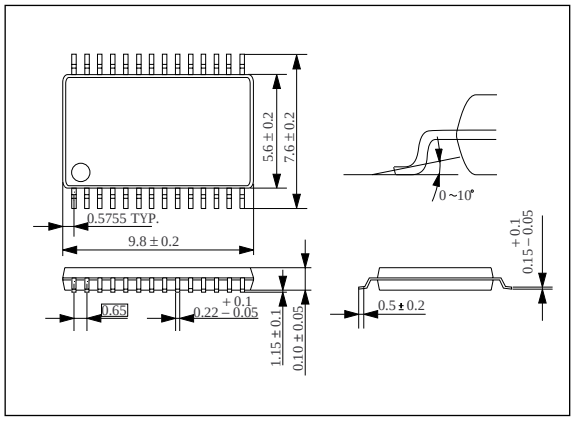
PACKAGE DIMENSIONS

Unit: mm

28-pin DIP (SM5839AP)



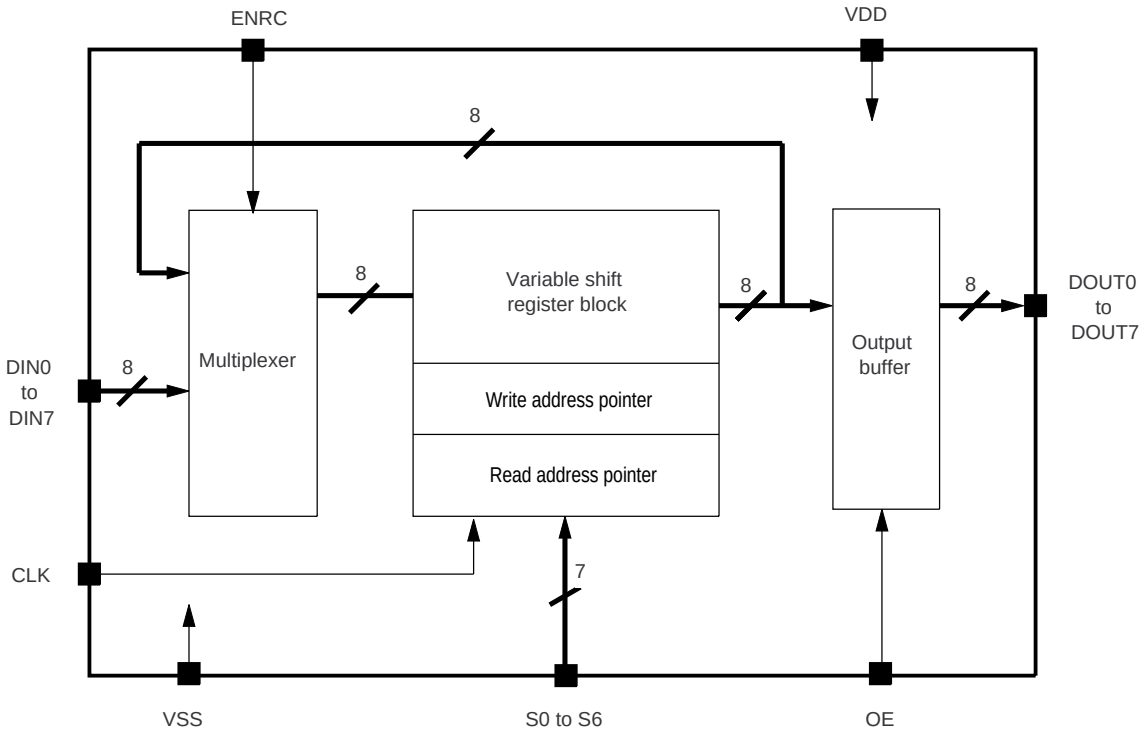
28-pin VSOP (SM5839AV)



ORDERING INFORMATION

Device	Package
SM5839AP	28-pin DIP
SM5839AV	28-pin VSOP

BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O[1]	Description
1	DIN0	Ip	Data input 0
2	DIN1	Ip	Data input 1
3	DIN2	Ip	Data input 2
4	DIN3	Ip	Data input 3
5	DIN4	Ip	Data input 4
6	DIN5	Ip	Data input 5
7	DIN6	Ip	Data input 6
8	DIN7	Ip	Data input 7
9	S6	Ip	Register length select control 6
10	S5	Ip	Register length select control 5
11	S4	Ip	Register length select control 4
12	S3	Ip	Register length select control 3
13	CLK	I	Clock input
14	VSS	–	Ground
15	S2	Ip	Register length select control 2
16	S1	Ip	Register length select control 1
17	S0	Ip	Register length select control 0
18	DOUT7	O	Data output 7
19	DOUT6	O	Data output 6
20	DOUT5	O	Data output 5

Number	Name	I/O[1]	Description
21	DOUT4	O	Data output 4
22	DOUT3	O	Data output 3
23	DOUT2	O	Data output 2
24	DOUT1	O	Data output 1
25	DOUT0	O	Data output 0
26	OE	Ip	Output enable
27	ENRC	Ip	Circulating/non-circulating control
28	VDD	–	Supply voltage

1. Ip = input pin with pull-up resistor, I = input pin, O = output pin. All outputs are 3-state pins.

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}	–40 to 125	°C
Power dissipation	P_D	330	mW
Soldering temperature	T_{sld}	255	°C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage range	V_{DD}	Standard-voltage specification	4.5	–	5.5	V
		Low-voltage specification	2.7	–	4.5	V
Operating temperature	T_{opr}		–20	–	70	°C

DC Characteristics

Standard-voltage specification: V_{DD} = 5.0 ± 0.5 V, V_{SS} = 0 V, T_a = –20 to 70 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Standby current consumption	I_{ST}		–	–	50	µA
Operating current consumption	I_{DD}	OE = 0 V, f_{CLK} = 54 MHz	–	30	50	mA
Input voltage[1]	V_{IH}		2.4	–	–	V
	V_{IL}		–	–	0.5	
Output voltage[2]	V_{OH}	I_{OH} = –0.4 mA	2.5	–	–	V
	V_{OL}	I_{OL} = 1.6 mA	–	–	0.4	
Input current[3]	I_{IL}	V_{IN} = 0 V	–	100	200	µA

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input leakage current[4]	I_{LL}	V_{IN} = 0 V	–	–	1	µA
Input leakage current[1]	I_{LH}	V_{IN} = V_{DD}	–	–	1	µA
Output high-impedance leakage current[2]	I_{ZH}	V_{OUT} = V_{DD}	–	–	5	µA
	I_{ZL}	V_{OUT} = 0 V	–	–	5	

1. All inputs (CLK, DIN0 to DIN7, S0 to S6, OE, ENRC)
2. All outputs (DOUT0 to DOUT7)
3. Inputs DIN0 to DIN7, S0 to S6, OE, ENRC
4. Input CLK only

Low-voltage specification: V_{DD} = 3.0 ± 0.3 V, V_{SS} = 0 V, T_a = –20 to 70 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Standby current consumption	I_{ST}		–	–	50	µA
Operating current consumption	I_{DD}	OE = 0 V, f_{CLK} = 20 MHz	–	10	20	mA
Input voltage[1]	V_{IH}		2.0	–	–	V
	V_{IL}		–	–	0.5	
Output voltage[2]	V_{OH}	I_{OH} = –0.4 mA	2.0	–	–	V
	V_{OL}	I_{OL} = 1.6 mA	–	–	0.8	
Input current[3]	I_{IL}	V_{IN} = 0 V	–	30	60	µA
Input leakage current[4]	I_{LL}	V_{IN} = 0 V	–	–	1	µA
Input leakage current[1]	I_{LH}	V_{IN} = V_{DD}	–	–	1	µA
Output high-impedance leakage current[2]	I_{ZH}	V_{OUT} = V_{DD}	–	–	5	µA
	I_{ZL}	V_{OUT} = 0 V	–	–	5	

1. All inputs (CLK, DIN0 to DIN7, S0 to S6, OE, ENRC)
2. All outputs (DOUT0 to DOUT7)
3. Inputs DIN0 to DIN7, S0 to S6, OE, ENRC
4. Input CLK only

AC Characteristics

Standard-voltage specification: V_{DD} = 5.0 ± 0.5 V, V_{SS} = 0 V, T_a = –20 to 70 °C

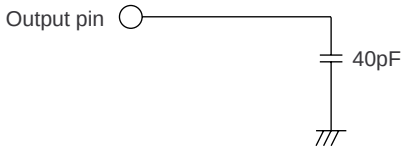
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
CLK clock frequency	f_{CLK}		–	–	54	MHz
CLK rise time	t_{CR}		–	–	100	ns
CLK fall time	t_{CF}		–	–	100	ns
CLK clock pulsewidth	t_{WH}		7	–	–	ns
DIN0 to DIN7, ENRC input setup time	t_{S1}		2	–	–	ns
S0 to S6 input setup time	t_{S2}		12	–	–	ns
DIN0 to DIN7, ENRC input hold time	t_{H1}		2	–	–	ns
S0 to S6 input hold time	t_{H2}		0	–	–	ns
DOUT0 to DOUT7 output data delay time	t_D	Output load circuit 1	–	–	18	ns

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DOUT0 to DOUT7 output data hold time	t_{OH}	Output load circuit 1	4	–	–	ns
DOUT0 to DOUT7 output enable delay time	t_{OEN0}, t_{OEN1}	Output load circuit 2	–	–	18	ns
DOUT0 to DOUT7 output disable delay time	t_{ODE0}, t_{ODE1}	Output load circuit 2	–	–	18	ns

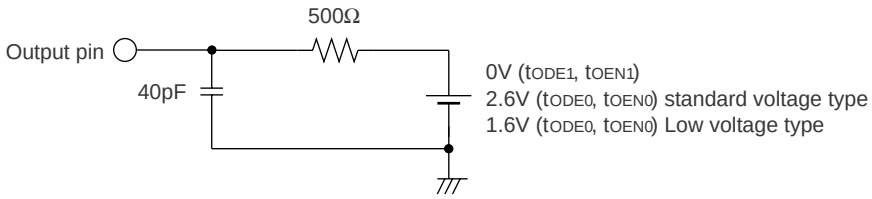
Low-voltage specification: V_{DD} = 2.7 to 4.5 V, V_{SS} = 0 V, T_a = –20 to 70 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
CLK clock frequency	f_{CLK}		–	–	20	MHz
CLK rise time	t_{CR}		–	–	100	ns
CLK fall time	t_{CF}		–	–	100	ns
CLK clock pulsewidth	t_{WH}		10	–	–	ns
DIN0 to DIN7, ENRC input setup time	t_{S1}		5	–	–	ns
S0 to S6 input setup time	t_{S2}		22	–	–	ns
DIN0 to DIN7, ENRC input hold time	t_{H1}		2	–	–	ns
S0 to S6 input hold time	t_{H2}		0	–	–	ns
DOUT0 to DOUT7 output data delay time	t_D	Output load circuit 1	–	–	35	ns
DOUT0 to DOUT7 output data hold time	t_{OH}	Output load circuit 1	7	–	–	ns
DOUT0 to DOUT7 output enable delay time	t_{OEN0}, t_{OEN1}	Output load circuit 2	–	–	35	ns
DOUT0 to DOUT7 output disable delay time	t_{ODE0}, t_{ODE1}	Output load circuit 2	–	–	35	ns

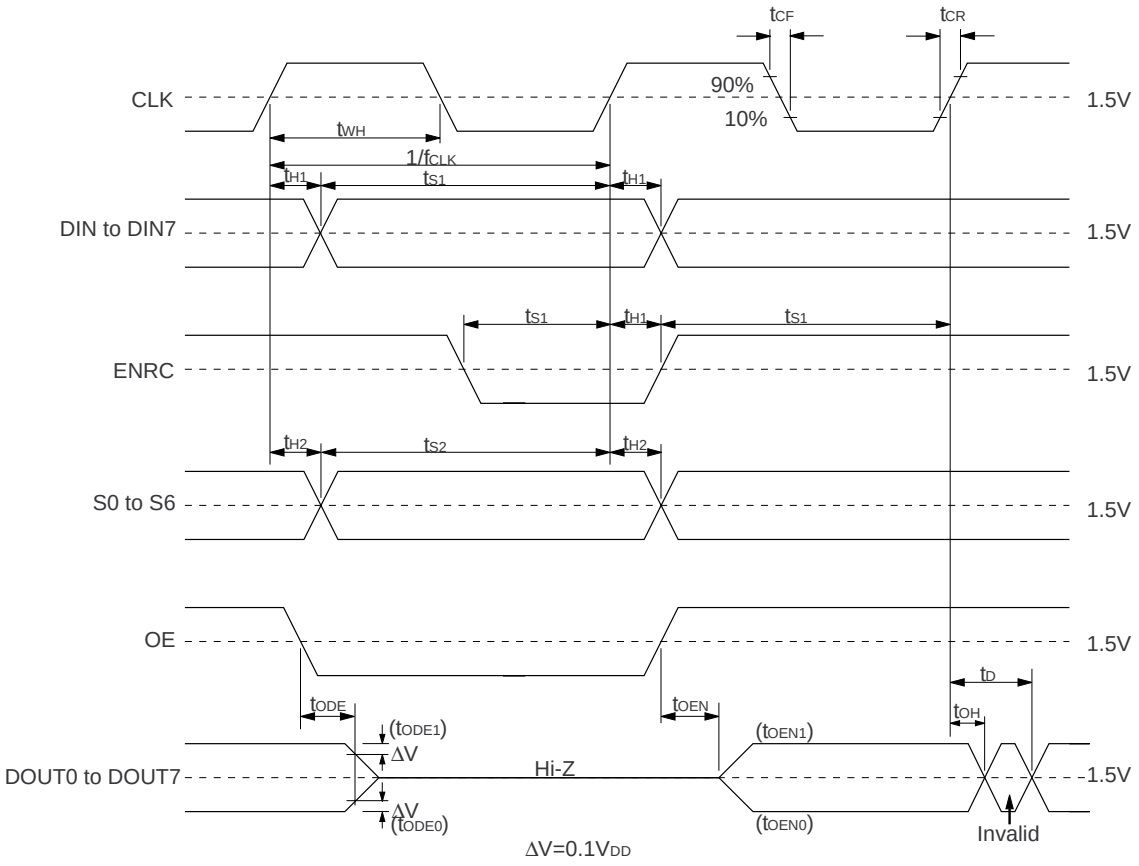
Output load circuit 1



Output load circuit 2



TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

Initialization

After power is first applied, up to a maximum of 128 input data cycles are considered invalid. However, any cycle that momentarily sets the register length to 2 steps (by setting S1 to S6 all LOW) and then to the desired value is considered to be the first valid cycle.

Resister Length Select

The S0 to S6 inputs set the register length (L) to the decimal-value given by the following equation using positive logic (HIGH = 1 and LOW = 0).

$$L = 64 \cdot (S6) + 32 \cdot (S5) + 16 \cdot (S4) + 8 \cdot (S3) + 4 \cdot (S2) + 2 \cdot (S1) + (S0) + 1$$

Length	S6	S5	S4	S3	S2	S1	S0
128	1	1	1	1	1	1	1
127	1	1	1	1	1	1	0
126	1	1	1	1	1	0	1
125	1	1	1	1	1	0	0
↓	↓	↓	↓	↓	↓	↓	↓
66	1	0	0	0	0	0	1
65	1	0	0	0	0	0	0
64	0	1	1	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓
3	0	0	0	0	0	1	0
2	0	0	0	0	0	0	×

Clock and Output Control

Input			Shift register	Output
ENRC	CLK	OE		DOUT0 to DOUT7
×	×	L	–	High impedance
×	×	H	–	Enabled
H	L → H	×	Circulating	–
L	L → H	×	Non-circulating	–

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