SHARP

Microcomputer Data Sheet

SM5L1/SM5L2/SM5L3
4-Bit Single Chip Microcomputers

FEATURES

- ROM capacity:
  - 2,048 × 8-bits (SM5L1)
  - 3,072 × 8-bits (SM5L2)
  - 4,096 × 8-bits (SM5L3)
- RAM capacity:
  - 69 × 4-bits, including 21 × 4-bits display RAM (SM5L1)
  - 130 × 4-bits, including 34 × 4-bits display RAM (SM5L2)
  - 170 × 4-bits, including 42 × 4-bits display RAM (SM5L3)
- 51 instruction sets
- Four levels of subroutine nesting
- I/O port:
  - One input
  - Five outputs
  - Eight input/outputs
- Interrupts:
  - Internal interrupt × 1 (divider overflow)
  - External interrupt × 1 (INTA)
- Built-in main clock oscillator for system clock
- Signal generation for real time clock
- Built-in 15 stage divider for real time clock
- Built-in LCD driver:
  - 84 segments (SM5L1), 136 segments (SM5L2), 168 segments (SM5L3), 1/2 bias, 1/4 duty cycle
- Built-in melody generator circuit:
  - Melody ROM
    - 160 steps (SM5L1), 256 steps (SM5L2/3)
  - Generating time (at 32.768 kHz)
    - 20 sec. (MAX.) (SM5L1)
    - 32 sec. (MAX.) (SM5L2/3)
- Instruction cycle time: 61 µs (TYP. at 32.768 kHz)
- Standby function
- Supply voltage: 1.5 V ± 20%
- Packages:
  - 60-pin QFP (QFP060-P-1414) (SM5L1)
  - 72-pin QFP (QFP072-P1010) (SM5L2)
  - 80-pin QFP (QFP080-P-1420) (SM5L2/3)

DESCRIPTION

The SM5L1/L2/L3 (SM5Lx series) are CMOS 4-bit single chip microcomputers operated on 1.5 V single power supply. This microcomputer integrates 4-bit parallel processing function, ROM, RAM, display RAM, 15-stage divider, two types of interrupt and four levels of subroutine stack. With a built-in LCD drive circuit for a maximum of 84/136/168 (SM5L1/L2/L3) elements, in a two-mode standby function, and a melody generator circuit in a single chip, the SM5Lx series permits the design of system configuration with a minimum of peripheral components. It can be used in a variety of products from handheld equipment to electrical appliances, such as audio timers, and also achieves lower power consumption.

PIN CONNECTIONS

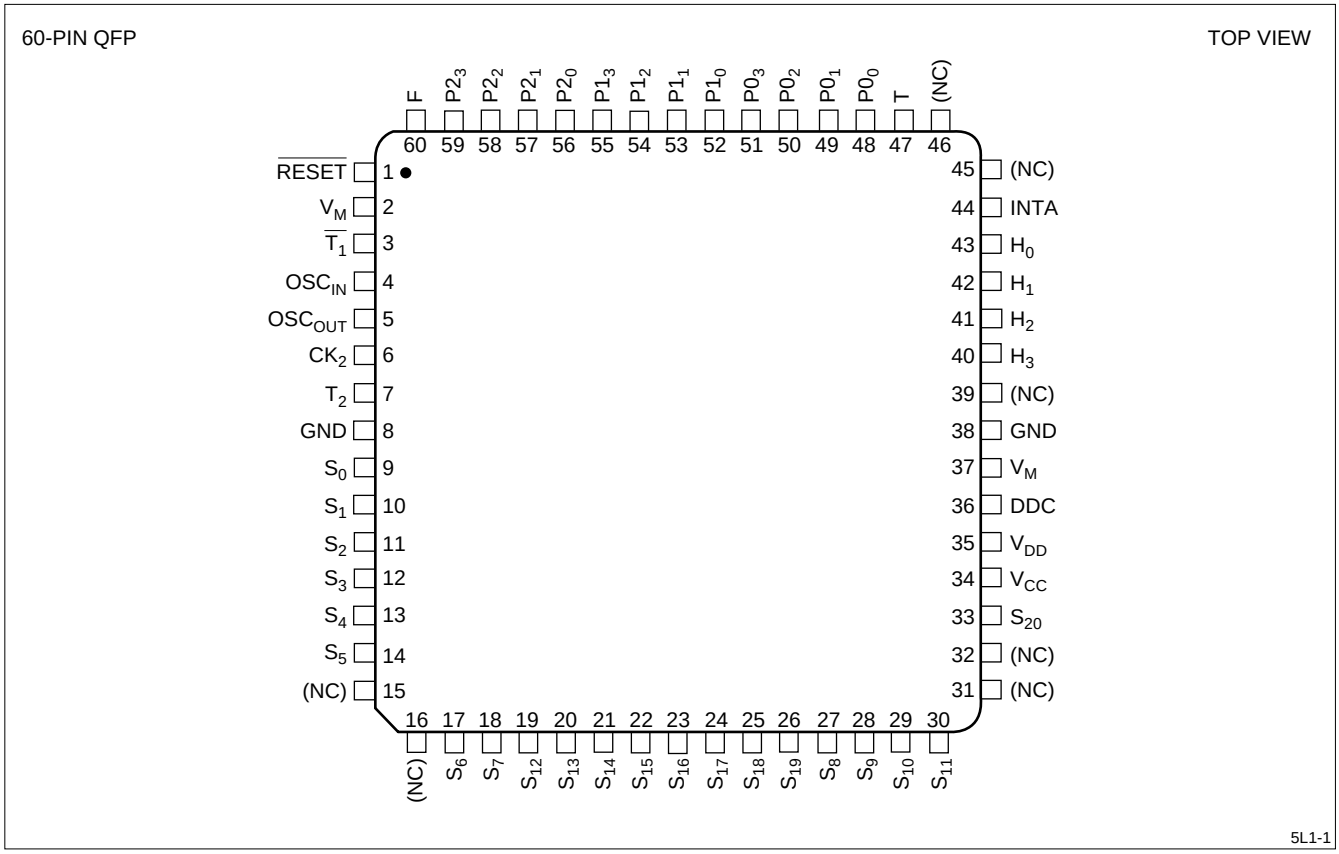


Figure 1. 60-pin QFP (SM5L1)

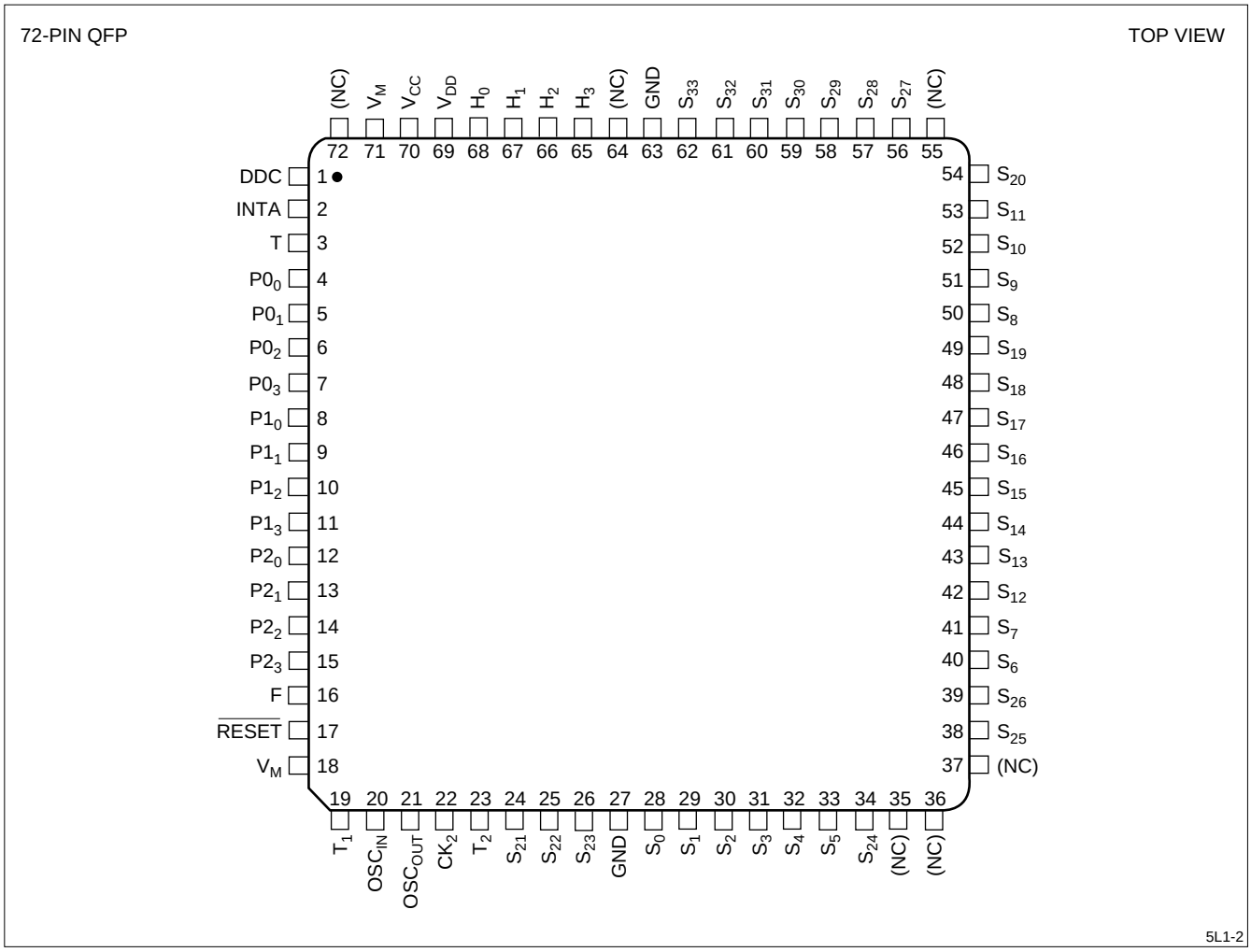


Figure 2. 72-pin QFP (SM5L2)

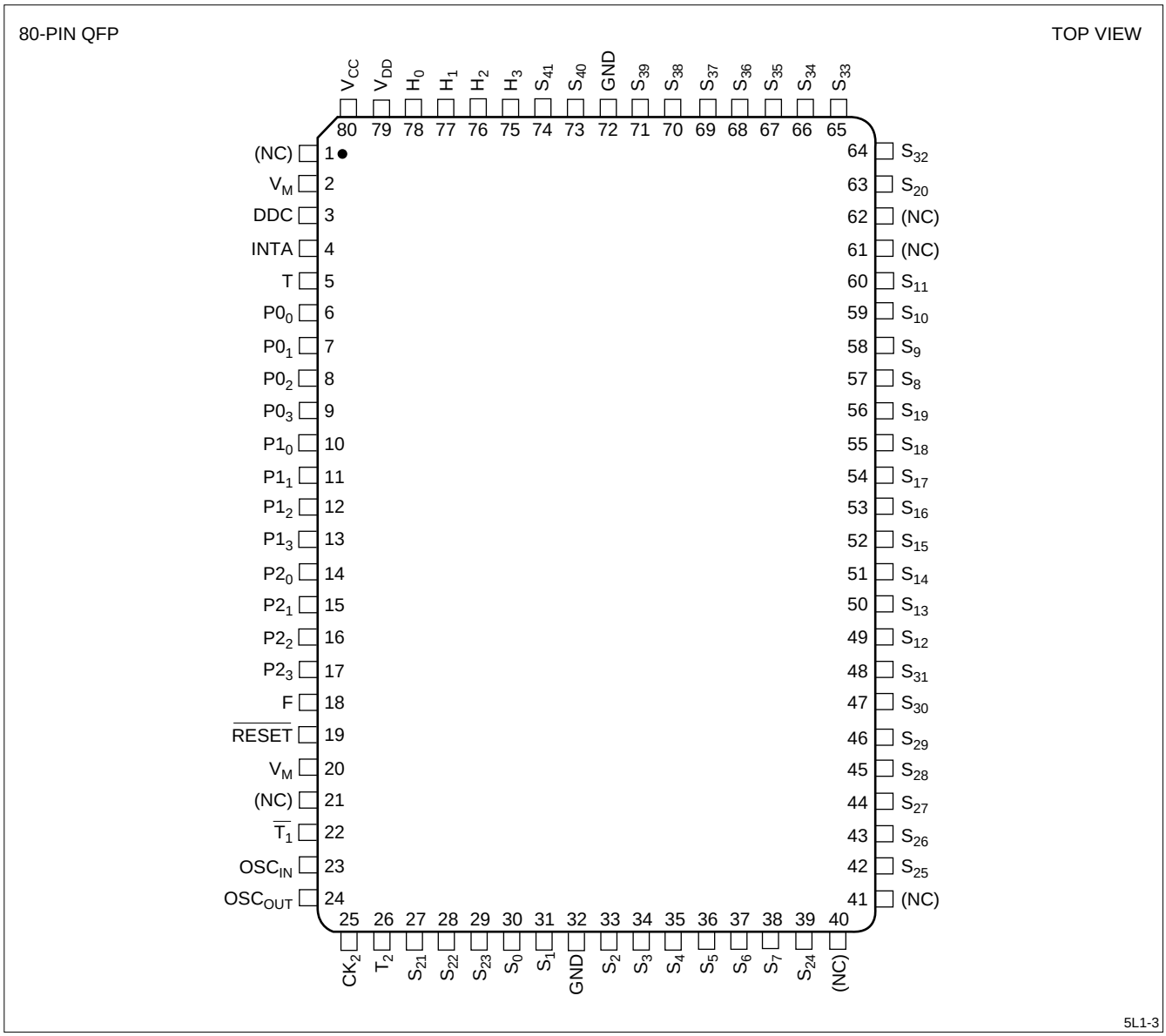
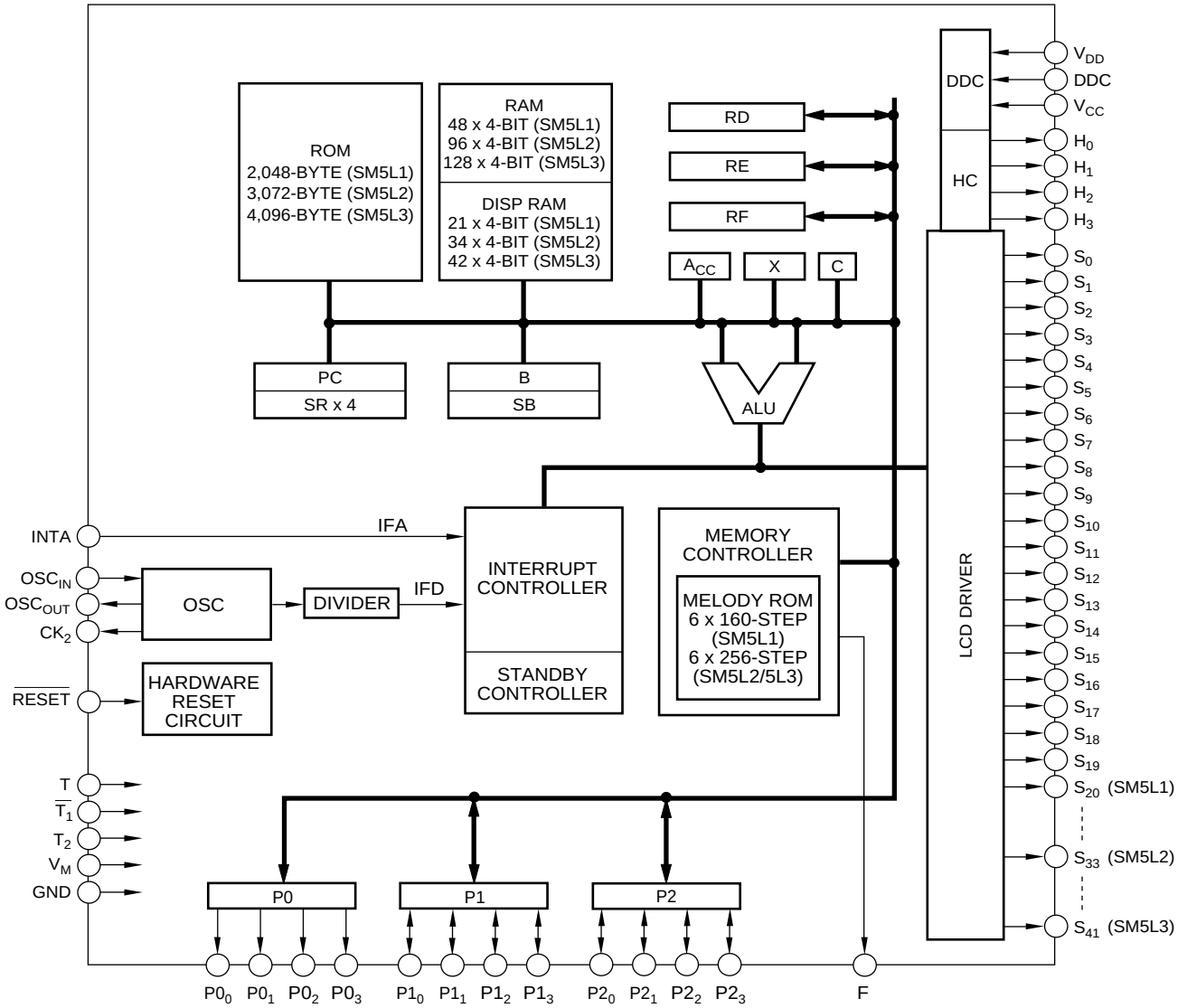


Figure 3. 80-pin QFP (SM5L2/3)

BLOCK DIAGRAM



NOTE: Symbol descriptions

A_{CC}: Accumulator
ALU: Arithmetic logic unit
B: RAM address register
C: Carry flag
DDC: Display boost circuit
HC: Common signal generator circuit
IFA: External interrupt flag
IFD: Divider overflow flag
OSC: System clock oscillator
P0 - P2: Port registers
PC: Program counter
RAM: Data memory
RD, RE, RF: Mode registers
ROM: Program memory
SB: Stack B register
SR: PC stack register
X: X register

5L1-4

Figure 4. SM5L1/SM5L2/SM5L3 Block Diagram

PIN DESCRIPTION

PIN NAME	I/O	FUNCTION
GND, V_M	I	Power supply pins. The V_M pin applies a positive supply with respect to the GND.
T, $\overline{T}_1$, T_2	I	LSI chip test pins. Cannot be used by the user. Connect T and T_2 pin to GND. Connect $\overline{T}_1$ pin to V_M.
$\overline{RESET}$	I	Input pin with built-in pull-up resistor. Hardware reset the LSI chip when a LOW level signal is input. Normally a capacitor is connected between it and GND to form a power-on reset circuit.
OSC_{IN}, OSC_{OUT}, CK_2	I/O	CR or crystal oscillator pins. Connect a CR or crystal oscillating element across OSC_{IN} - OSC_{OUT} (crystal) or OSC_{IN} - CK_2 (CR) to form a clock generator circuit. Use of a CR or crystal oscillating element is determined by the mask option.
F	O	Melody output pin. Outputs the contents of a melody ROM with 12 musical scale (555 to 2,114 Hz) in two octaves.
H_0 - H_3	O	Common output pins. Pins for the LCD's common signals.
S_0 - S_{20} (SM5L1) S_0 - S_{33} (SM5L2) S_0 - S_{41} (SM5L3)	O	Pins for the LCD's segment signals.
INTA	I	Input pin for external interrupt. The IFA flag is set at the leading edge of INTA.
$P0_0$ - $P0_3$	O	Output pins. The accumulator A_{CC} can be transferred to this port by instruction.
$P1_0$ - $P1_3$, $P2_0$ - $P2_3$	I/O	I/O pins which can switch to input or output pins in 4-bit units by instruction. They can be used as output pins when configured for a key matrix. The SM5Lx is forced to hardware reset when all of $P1_0$ - $P1_3$ pins are HIGH level (by mask option).

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_M	-0.3 to 2.0	V	
	V_{DD}	-0.3 to 4.0	V	
Input voltage	V_I	-0.3 to V_M + 0.3	V	
Output voltage	V_O	-0.3 to V_M + 0.3	V	
Source output current for each pin	I_{O1}	2	mA	1
	I_{O2}	2	mA	2
	I_{O3}	2	mA	3
	I_{O4}	2	mA	4
Sink output current for each pin	I_{O5}	2	mA	1
	I_{O6}	100	µA	2
	I_{O7}	2	mA	3
	I_{O8}	2	mA	4
Total source output current	I_{OH}	10	mA	
Total sink output current	I_{OL}	10	mA	
Operating temperature	T_{OPR}	0 to 50	°C	
Storage temperature	T_{STG}	-55 to 150	°C	

NOTES:
1. Applicable pins: $P0_0$ - $P0_3$.
2. Applicable pins: $P1_0$ - $P1_3$, $P2_0$ - $P2_3$.
3. Applicable pin: F.
4. Applicable pins: H_0 - H_3, S_0 - S_{20} (SM5L1), S_0 - S_{33} (SM5L2),S_0 - S_{41} (SM5L3).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_M	1.2 to 1.8	V	
	V_{DD}	2.4 to 3.6	V	
Instruction cycle	T_{SYS}	122 to 50	µs	
Oscillation starting voltage	V_{OSC}	1.4	V	1

NOTE:
1. Use the crystal oscillation circuit.

Oscillation Circuit

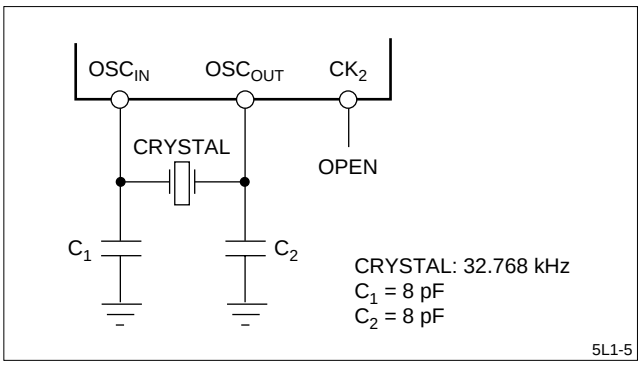


Figure 5. Crystal Oscillation (Frequency = 32.768 kHz)

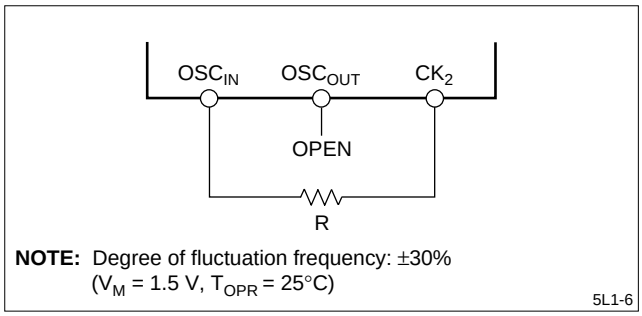


Figure 6. CR Oscillation (Frequency = 40 kHz)

NOTE: Mount the R, C and crystal as close to the LSI chip as possible to minimize the effects of stray capacitance.

DC CHARACTERISTICS

V_M = 1.5 V ±0.1 V, T_{OPR} = 0°C to 50 °C

PARAMETER	SYMBOL	CONDITIONS	MIN.[1]	TYP.[2]	MAX.[1]	UNIT	NOTE
Input voltage	V_{IH1}		0.8 × V_M		V_M	V	3
	V_{IL1}		0		0.2 × V_M	V	3
	V_{IH2}		V_M – 0.25		V_M	V	4
	V_{IL2}		0		0.25	V	4
Input current	I_{IH1}	V_{IH} = V_M			1.0	µA	5
	I_{IH2}	V_{IH} = V_M		1.5/3/3		µA	6
	I_{IL1}	V_{IL} = 0 V		1.5/3/3		µA	7
Boost output voltage	V_{DD1}	V_M = 1.4 V RL = 5 MΩ	2.5			V	8
	V_{DD2}	V_M = 1.6 V RL = 5 MΩ	2.9			V	8
Output current	$-I_{OH1}$	V_{OH} = V_M – 0.5 V	100			µA	9
	I_{OL1}	V_{OL} = 0.5 V	100			µA	9
	$-I_{OH2}$	V_{OH} = V_M – 0.5 V	100			µA	10
	I_{OL2}	V_{OL} = 0.5 V	3.0			µA	10
Output impedance	D_{COM}	V_M = 1.5 V		15		kΩ	11
	D_S	V_M = 1.5 V		30		kΩ	12
Supply current	I_{DA}	V_M = 1.5 V T_{SYS} = 122 µs		8/10/12	15	µA	13
	I_{DH1} (Halt Mode)			5/7/8	8	µA	14
	I_{DH12} (Halt Mode)			3/4/5	5	µA	15
	I_{DS} (Stop Mode)			1/1.5/2	3	µA	16

NOTES:
1. SM5L1 specifications.
2. */*/* = SM5L1/L2/L3.
3. Applicable pins: $P1_0$ - $P1_3$, $P2_0$ - $P2_3$.
4. Applicable pins: OSC_{IN}, $\overline{RESET}$, T, INTA.
5. Applicable pins: $P2_0$ - $P2_3$.
6. Applicable pins: T, INTA, $P1_0$ - $P1_3$.
7. Applicable pin: $\overline{RESET}$.
8. Applicable pin: V_{DD}.
9. Applicable pins; $P0_0$ - $P0_3$, F.
10. Applicable pins: $P1_0$ - $P1_3$, $P2_0$ - $P2_3$.
11. Applicable pins: H_0 - H_3.
12. Applicable pins: S_0 - S_{20} (SM5L1), S_0 - S_{33} (SM5L2), S_0 - S_{41} (SM5L3)
13. No load condition. Supply current under the operation when driving a CR oscillator
14. No load condition. Supply current when driving a CR oscillator and turning LCD ON placed the device in halt mode.
15. No load condition. Supply current when driving a CR oscillator and turning LCD OFF placed the device in halt mode.
16. No load condition. Supply current when the entire system is inactivated.

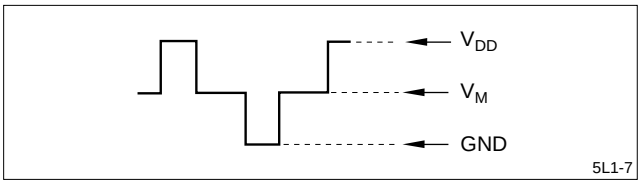


Figure 7. LCD Waveform Example

SYSTEM CONFIGURATION

A Register and X Register

The A register (or accumulator: A_{CC}) is a 4-bit general purpose register. The register is mainly used in conjunction with the ALU, C flag and RAM to transfer numerical value and data to perform various operations. The A register is also used to transfer data between input and output pins.

The X register (or auxiliary accumulator) is a 4-bit register and can be used as a temporary register. It loads contents of the A register or its content is transferred to the A register.

When the table reference instruction PAT is used, the X and A registers load ROM data. A pair of A and X registers can accommodate 8-bit data.

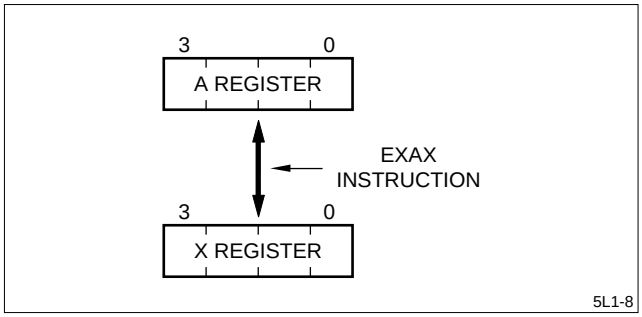


Figure 8. Data Transfer Example Between A Register and X Register

Arithmetic and Logic Unit (ALU) and Carry Signal Cy

The ALU performs 4-bit parallel operation. The ALU operates binary addition in conjunction with RAM, C flag and A register. The carry signal Cy is generated if a carry occurs during ALU operation. Some instructions use Cy: ADC instruction sets/clears the content of the C flag; ADX instruction causes the program to skip the next instruction. Note that Cy is the symbol for carry signal and not for C flag.

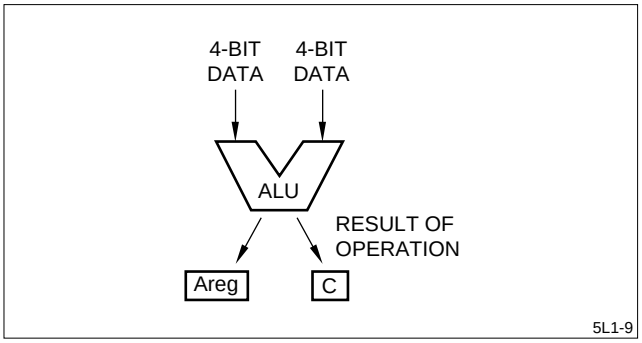


Figure 9. ALU

B Register and SB Register

B REGISTER (B_M, B_L)

The B register is an 8-bit register that is used to specify the RAM address. The upper 4-bit section is called the B_M register and lower 4-bit section is called the B_L register.

SB REGISTER

The SB register is an 8-bit register used as the save register for the B register. The contents of B register and SB register can be exchanged through EX instruction.

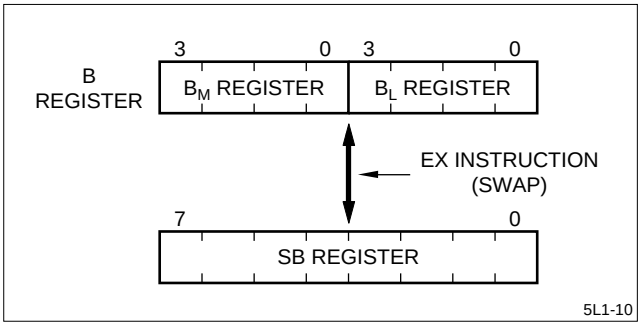


Figure 10. B Register and SB Register

Data Memory (RAM)

The data memory (RAM) is used for storage. The RAM capacity consists of:

- SM5L1: 69 × 4-bit, includes 21 × 4-bit display RAM.
- SM5L2: 130 × 4-bit, includes 34 × 4-bit display RAM.
- SM5L3: 170 × 4-bit, includes 42 × 4-bit display RAM.

Display RAM, outputs data to an external pin for driving the segments of the LCD. Therefore, by writing data to the display RAM, the LCD can be driven at 1/4 duty (1/2 bias) to enable automatic display of the LCD.

As shown in Figure 14, the display RAM is connected to segment outputs.

- SM5L1: Port S_0 to S_{20}
- SM5L2: Port S_0 to S_{33}
- SM5L3: Port S_0 to S_{41}

These segment outputs correspond to the LCD common outputs H_0 to H_3. Data M_0 to M_3 is for one column of the display RAM and is output as a LCD drive waveform which corresponds to outputs H_0 to H_3. As a RAM, the display RAM operates exactly the same as other RAMs.

B_M \ B_L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
8	S_0	S_2	S_4	S_6	S_8	S_{10}	S_{12}	S_{14}	S_{16}	S_{18}	S_{20}					
9	S_1	S_3	S_5	S_7	S_9	S_{11}	S_{13}	S_{15}	S_{17}	S_{19}						

NOTE: The area surrounded by the thick line represents the display RAM where S_0 - S_{20} corresponds to the segment output.

5L1-11

Figure 11. RAM Organization (SM5L1)

B_M \ B_L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5																
8	S_0	S_2	S_4	S_6	S_8	S_{10}	S_{12}	S_{14}	S_{16}	S_{18}	S_{20}	S_{22}	S_{24}	S_{26}	S_{28}	S_{30}
9	S_1	S_3	S_5	S_7	S_9	S_{11}	S_{13}	S_{15}	S_{17}	S_{19}	S_{21}	S_{23}	S_{25}	S_{27}	S_{29}	S_{31}
A	S_{32}															
B	S_{33}															

NOTE: The area surrounded by the thick line represents the display RAM where S_0 - S_{33} corresponds to the segment output.

5L1-12

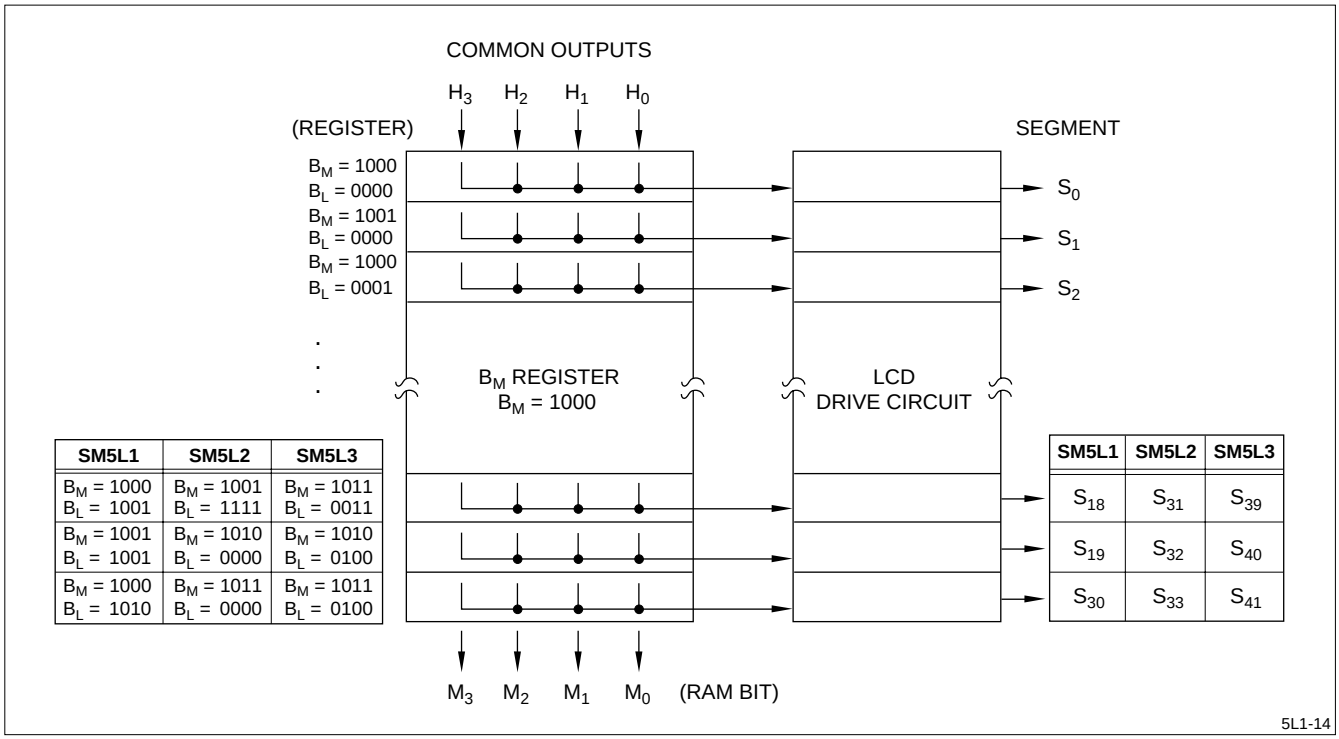
Figure 12. SM5L2 RAM Organization

B_M \ B_L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5																
6																
7																
8	S_0	S_2	S_4	S_6	S_8	S_{10}	S_{12}	S_{14}	S_{16}	S_{18}	S_{20}	S_{22}	S_{24}	S_{26}	S_{28}	S_{30}
9	S_1	S_3	S_5	S_7	S_9	S_{11}	S_{13}	S_{15}	S_{17}	S_{19}	S_{21}	S_{23}	S_{25}	S_{27}	S_{29}	S_{31}
A	S_{32}	S_{34}	S_{36}	S_{38}	S_{40}											
B	S_{33}	S_{35}	S_{37}	S_{39}	S_{41}											

NOTE: The area surrounded by the thick line represents the display RAM where S_0 - S_{41} corresponds to the segment output.

5L1-13

Figure 13. SM5L3 RAM Organization



SM5L1	SM5L2	SM5L3
B_M = 1000 B_L = 1001	B_M = 1001 B_L = 1111	B_M = 1011 B_L = 0011
B_M = 1001 B_L = 1001	B_M = 1010 B_L = 0000	B_M = 1010 B_L = 0100
B_M = 1000 B_L = 1010	B_M = 1011 B_L = 0000	B_M = 1011 B_L = 0100

SM5L1	SM5L2	SM5L3
S_{18}	S_{31}	S_{39}
S_{19}	S_{32}	S_{40}
S_{30}	S_{33}	S_{41}

Figure 14. Relationship between the Display RAM and LCD Segment Outputs/Common Outputs

Program Counter PC and Stack Register SR

A ROM address is specified by the program counter (PC). The PC is comprised of 12 bits where 6-bits (P_U) are used to specify the page, and 6-bit are used to specify the step. P_U is a register and P_L is a binary counter. The program counter PC and the Stack Register SR are shown in Figure 15.

The table reference instruction PAT executes a similar operation to that of the subroutine jump and uses one level of the stack register.

Program Memory (ROM)

The ROM is used for program storage. The ROM capacity of the SM5Lx is 2,048/3,072/4,096-step. The ROM is organized into 32/48/64-page where one page is organized into 64 steps.

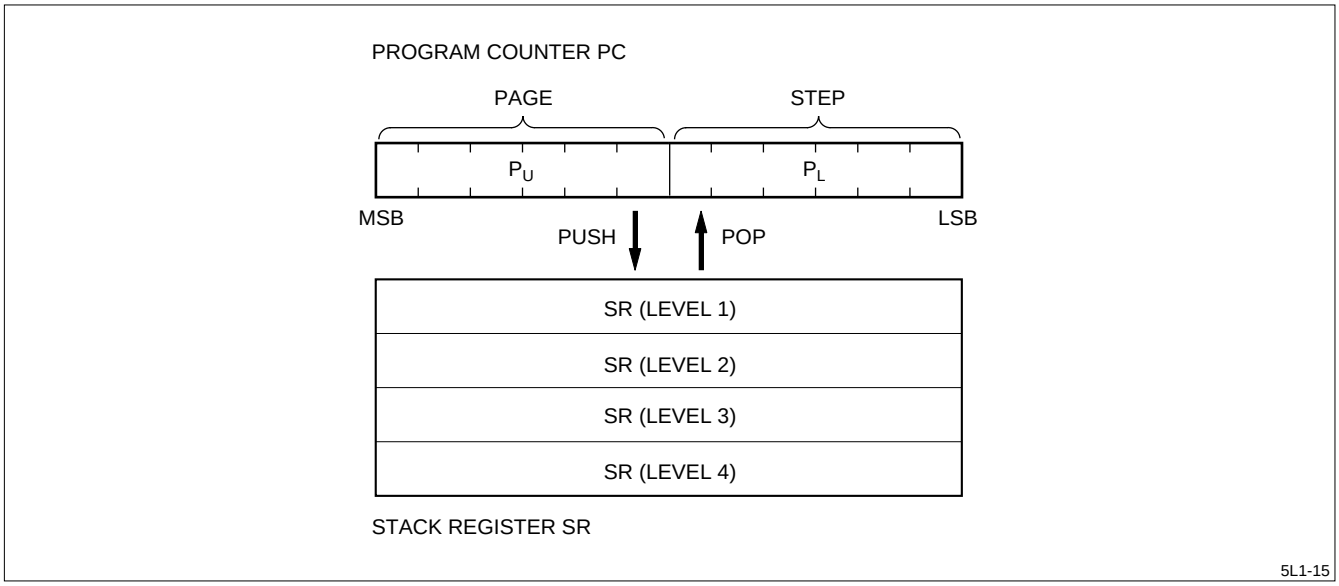


Figure 15. Program Counter PC and Stack Register SR

Page	00_H	01_H	02_H	03_H	04_H	05_H	06_H	07_H	08_H	09_H	$0A_H$	$0B_H$	$0C_H$	$0D_H$	$0E_H$	$0F_H$
P_U	000000	000001	000010	000011	000100	000101	000110	000111	001000	001001	001010	001011	001100	001101	001110	001111
	Program Start	First page of subroutine TRS	Interrupt	Standby Release	Table Reference Page PAT											

Page	10_H	11_H	12_H	13_H	14_H	15_H	16_H	17_H	18_H	19_H	$1A_H$	$1B_H$	$1C_H$	$1D_H$	$1E_H$	$1F_H$
P_U	010000	010001	010010	010011	010100	010101	010110	010111	011000	011001	011010	011011	011100	011101	011110	111111
																Last Page (SM5L1)

Page	20_H	21_H	22_H	23_H	24_H	25_H	26_H	27_H	28_H	29_H	$2A_H$	$2B_H$	$2C_H$	$2D_H$	$2E_H$	$2F_H$
P_U	100000	100001	100010	100011	100100	100101	100110	100111	101000	101001	101010	101011	101100	101101	101110	101111
																Last Page (SM5L2)

Page	30_H	31_H	32_H	33_H	34_H	35_H	36_H	37_H	38_H	39_H	$3A_H$	$3B_H$	$3C_H$	$3D_H$	$3E_H$	$3F_H$
P_U	110000	110001	110010	110011	110100	110101	110110	110111	111000	111001	111010	111011	111100	111101	111110	111111
																Last Page (SM5L3)

5L1-16

Figure 16. ROM Organization

Flags

The SM5Lx provides three flag (C flag and interrupt request flags IFA and IFD) which can be used to set or determine conditions.

Output Latch Registers and Mode Registers

The output latch registers are connected to the P0, P1 and P2 pins. By instruction, the contents of the A_{CC} can be transferred to the output latch registers. The SM5Lx also contains mode registers RD, RE and RF. Setting the value of each register enables the LCD or interrupt to be controlled. Setting a register is performed in the same way as for the other output pins. The function of the mode registers are shown in Table 1.

INTA PIN

- INTA level can be loaded to A_{CC} (bit 0), as follows:
  LBLX 4
  IN
- INTA level does not load directly through the noise debounce circuit (see Figure 17).

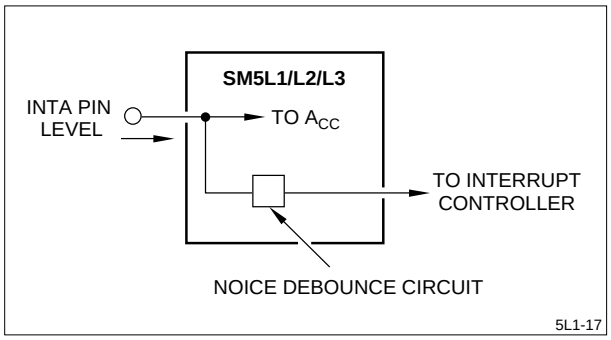


Figure 17. INTA Pin

CAUTION

Connecting Consideration of I/O Port

When using an I/O port as bidirectional bus such as data bus, avoid setting the I/O port to output when the target pin is also set output.

Whenever the output data conflict with each other, system failure will happen, due to damaged circuits or instantaneous supply voltage drop.

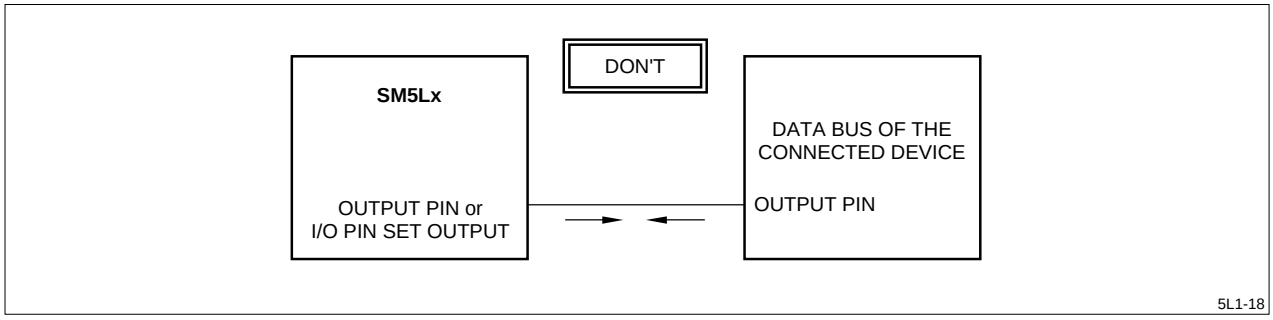


Figure 18. I/O Port Connection Precaution

Table 1. Mode Register Setting

REGISTER		SET VALUE	MODE DESCRIPTION
TYPE	BIT		
RD	RD0	0	Clears the ME F/F to stop a melody.
		1	Sets the ME F/F to start a melody from a ROM pointer address.
	RD1	—	Sets by stop instruction (of melody code) and reset by TPB instruction.
	RD2, RD3	—	Sets '0' only.
RE	RE0	0	Masks the interrupt based on the IFA flag.
		1	Accepts the interrupt based on the IFA flag.
	RE1	—	Sets '0' only.
	RE2	0	Masks the interrupt based on the IFD flag.
		1	Accepts the interrupt based on the IFD flag.
	RE3	—	No setting.
RF	RF0	0	Turns off the LCD.
		1	Turns on the LCD.
	RF1	0	Stops the function of a booster circuit.
		1	Operates the function of a booster circuit.
	RF2	0	Creates the system clock frequency by dividing the main oscillation frequency by 2.
		1	Creates the system clock frequency by dividing the main oscillation frequency by 4.
	RF3	—	Sets '0' only.

System Clock Generator and Dividers

The main oscillation frequency which is input through OSC_{IN} - OSC_{OUT} or OSC_{IN} - CK_2 is divided into two or four to generate the system clock f_{SYS}. This function is shown in Figure 19.

System clock f_{SYS} determines the execution instruction cycle so that the system clock period is the same as the instruction cycle.

However, the instruction execution cycle of two-word instruction is twice that of one word instructions.

Use of a CR oscillating element or a crystal oscillating element for the oscillator circuit is determined by the mask option. The crystal oscillator which is input through OSC_{IN} - OSC_{OUT} can be used as both real time clock and display signal of LCD. On the final stage of the divider, fc can be set to 1 Hz or 2 Hz (in case of 32 kHz crystal oscillation) depending on the mask option.

Either of the system clock frequencies 16.384 kHz or 8.192 kHz (in case of 32.768 kHz oscillation) can be selected by the RF2 flag (see Table 2). The 8.192 kHz clock has slower command execution speed, but uses less power for the same function.

The system clock is initialized to 16.384 kHz after hardware reset operation.

Table 2 shows the relationship between the contents of RF2 flag for the OSC resonator and the generated frequency, f_{SYS}.

Table 2. OSC Resonator and Frequency f_{SYS}

FOR OSC RESONATOR	CONTENTS OF RF2 FLAG	GENERATED FREQUENCY f_{SYS}
32.768 kHz crystal oscillation	0	16.384 kHz
	1	8.192 kHz
40 kHz CR oscillation	0	20 kHz
	1	10 kHz

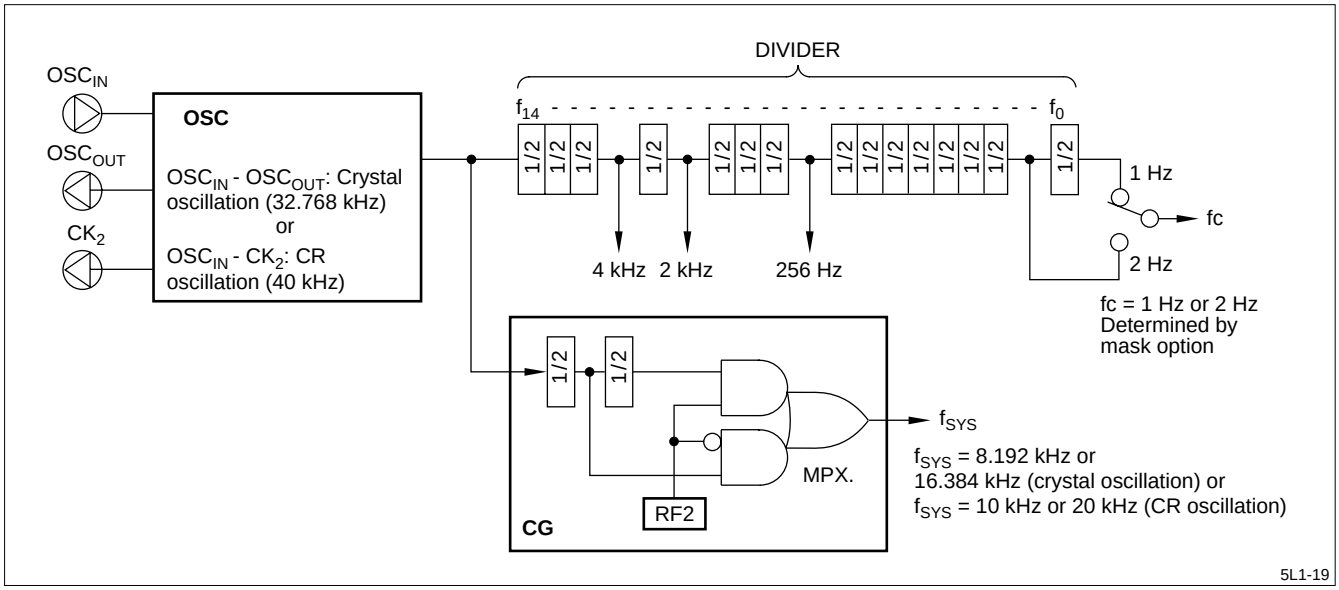


Figure 19. System Clock Generator and Divider

FUNCTIONAL DESCRIPTION

Melody Output Function

The built-in melody generation circuit provides a variety of sound signals. Figure 20 shows the block diagram of the melody generating circuit.

The melody ROM can store notes, rest and stop commands in 160/256/256 step (1 step consists of 6-bits), allowing the generation of 12 scale over two octaves (555 to 2,097 Hz) and the section of the time base for notes (125/62.5 ms).

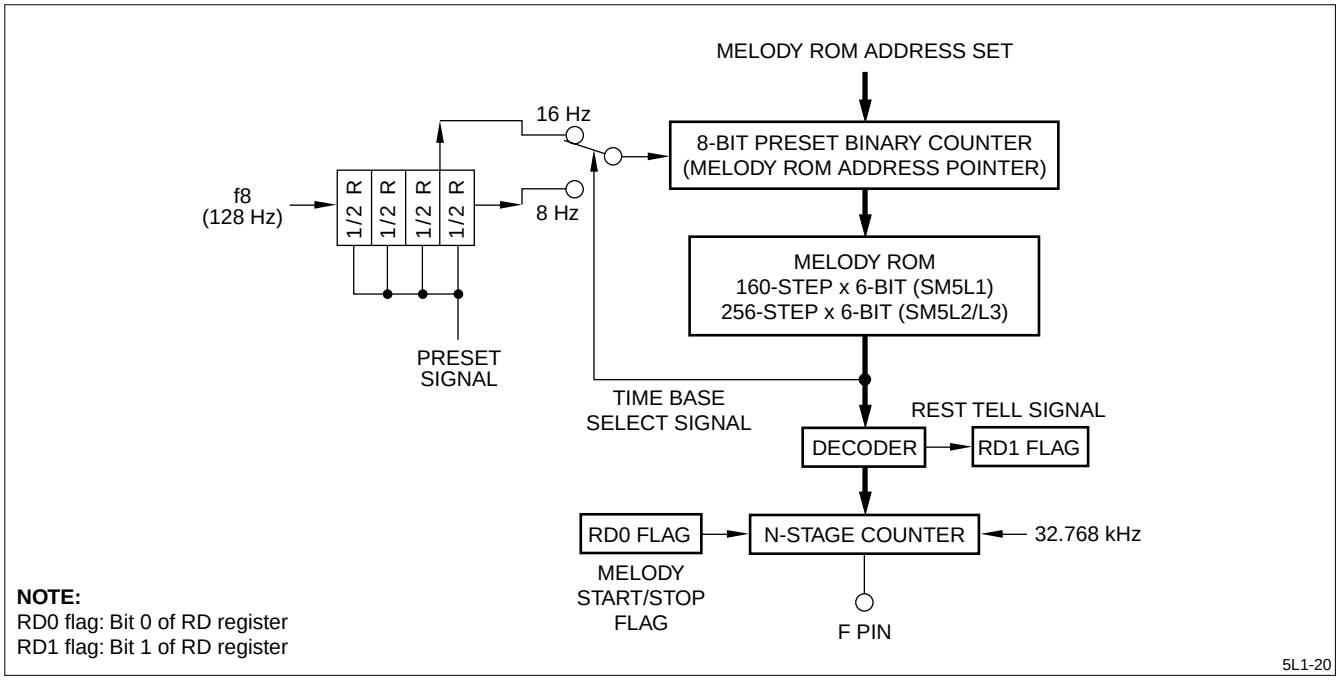


Figure 20. Melody Generating Circuit

CONTROL PROCEDURE

The binary counter for designating the address of the melody ROM can be arbitrarily set using the PRE instruction. A performance is started and stopped by the RD0 flag to '1' and '0'.

The stop code generates a 'rest tell signal', and at the same time, sets the RD1 flag.

Accordingly, to stop a performance at the end of melody, the RD0 flag must be clear upon detection of RD1 flag = 1.

Next step of PRE instruction, put the NOP instruction.

The following is an example of a melody generating program.

```
MELO    LAX     2
        ATX
        LAX     1
        PRE             ;Set the starting address of the
                        melody at the 21st hexadecimal
                        step
        NOP             ;Dummy command
        :
        :
        LBLX    0DH
        LAX     1
        OUT             ;Start the melody
        TPB     1       ;Executed for clear the RD1 flag
        NOP             ;Dummy command
        :
        :
        LBLX    0DH
L1      TPB     1       ;Test the RD1 flag
        TR      L1      ;Loop for detect the stop code
        LAX     0
        OUT             ;Stop the melody
```

Using these functions, the user can generate music, sound effects, alarm signals, etc. as desired, and any portion of the music can be repeated. Figure 21 lists the melody output frequencies. The output frequency can be halved by making bit 5 (OCT) of the melody ROM LOW ('0'). In Figure 21, m_0 to m_3 show data in bits 1 to 4 of the melody ROM.

	m_3 m_2 m_1 m_0	OUTPUT FREQUENCY (Hz)	CLOCK NUMBER (NOTE 1)	(NOTE 2)
do	0 0 1 0	2114.1	15.5	7 8 8 8
si	0 0 1 1	1985.9	16.5	8 8 8 9
la#	0 1 0 0	1872.4	17.5	8 9 9 9
la	0 1 0 1	1771.2	18.5	9 9 9 10
sol#	0 1 1 0	1680.4	19.5	9 10 10 10
sol	0 1 1 1	1560.4	21.0	10 11 10 11
fa#	1 0 0 0	1489.5	22.0	11 11 11 11
fa	1 0 0 1	1394.4	23.5	11 12 12 12
mi	1 0 1 0	1310.7	25.0	12 13 12 13
re#	1 0 1 1	1236.5	26.5	13 13 13 14
re	1 1 0 0	1170.3	28.0	14 14 14 14
do#	1 1 0 1	1110.8	29.5	14 15 15 15

NOTES:
1. Number of clocks for one cycle.
2. The number (n) in the waveforms represents the number of periods of the oscillation frequency (32.768 kHz) from the crystal oscillator for the duration in that particular part of the waveform.

5L1-21

Figure 21. Melody Output Frequencies

MELODY ROM INSTRUCTION

The melody ROM instruction is composed of 6 bits. The 6-bit instruction (one set) corresponding to a musical note, generates a sound signal.

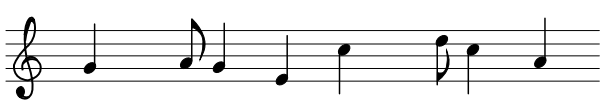
Table 3. Melody Bit Description

BIT	DESCRIPTION
I	Control the tone length. When '1', 125 ms; when '0', 62.5 ms.
OCT	When the octave is '1', the frequency is determined by m_3 - m_0. When the octave is '0', 1/2 of the frequency determined by m_3 - m_0.
m_3 - m_0	Frequency as shown in Figure 21. Pause when $m_3 = m_2 = m_1 = m_0 = 0$, stop instruction when $m_3 = m_2 = m_1 = 0$, $m_0 = 1$.

EXAMPLE OF WRITING ON THE MELODY ROM

An example of writing a tone such as the following, on the melody ROM are shown in Figure 22 and Table 4.

The tone length of an initial musical note which is generated from ROM addressed data assigned by a PRE instruction has an error of maximum ±4 ms. Therefore, by applying a pause as an initial note, a melody performs with a precisely regulated tone length.



MUSICAL SCALE	TONE LENGTH (ms)	OCT	m3	m2	m1	m0
sol	375	0	0	1	1	1
la	125	0	0	1	0	1
sol	250	0	0	1	1	1
mi	250	0	1	0	1	0
do	375	1	0	0	1	0
re	125	1	1	1	0	0
do	250	1	0	0	1	0
la	250	0	0	1	0	1

5L1-22

Figure 22. Melody ROM Tone Writing Example

Table 4. Melody ROM Instruction Example

ADDRESS	DATA	MUSICAL NOTE INSTRUCTION
00	00	pause
01	27	sol
02	27	sol
03	27	sol
04	25	la
05	27	sol
06	27	sol
07	2A	mi
08	2A	mi
09	22	do
0A	22	do
0B	22	do
0C	3C	re
0D	22	do
0E	22	do
0F	25	la
10	25	la
11	01	stop

Standby Function

A standby function is available which temporarily stops program execution to conserve power consumption. The state during which a program is in execution is called the operation mode and the state during which the execution is temporarily stopped is called the standby mode.

The standby mode further contains two modes, the stop mode and the halt mode. The stop mode stops the system section. In the stop mode, the display (LCD) is blanked. And the response speed of LCD returning to the display state (the operation) drops slightly.

The halt mode stops only the system clock generator circuit, the state of the LCD is retained. This mode is used to activate the system immediately after a condition causes a release to the operation mode.

To enter the standby mode, select either stop mode or halt mode, whichever is appropriate. See Figure 23.

During the standby mode, the contents of the RAM and C flag are retained. The contents of the flags, registers and output latches shown below are also retained.

- Flags
  - IFA flag
  - IFD flag
  - IME flag
- Registers
  - A_{CC}
  - X register
  - B_M, B_L register
  - SP
  - SR
- Output latch registers
  - P0 register
  - P1 register
  - P2 register

A release from the standby mode to the operation mode is performed by a reset port input, an interrupt from the nonmaskable INTA and divider. A maskable interrupt request cannot become a factor in releasing back to the operation mode. The mask setting is performed with RE register, see Table 1.

CAUTION

When all of $P1_0$ to $P1_3$ levels are HIGH, the SM5Lx is programmed to release the standby mode and enter a normally hardware reset operation (mask option).

TRANSITION FROM THE OPERATION MODE TO THE STANDBY MODE

The HALT instruction is executed to set the halt mode and the STOP instruction is executed to set the stop mode.

Since the interrupt is used to release from the standby mode, the mode does not transfer to the standby mode if any of the following conditions are satisfied during execution of the STOP or HALT instruction.

- RE0 is set and the INTA level is HIGH.
- RE2 is set and the IFD flag is set.

If any of the conditions above are satisfied, the mode does not transfer to the standby mode even if the STOP or HALT instruction is executed and the instruction at the address following that of the STOP or HALT instruction is executed. Therefore, place the JUMP instruction which specified step '0' on page 3 to the location at the address following that of the STOP or HALT instruction.

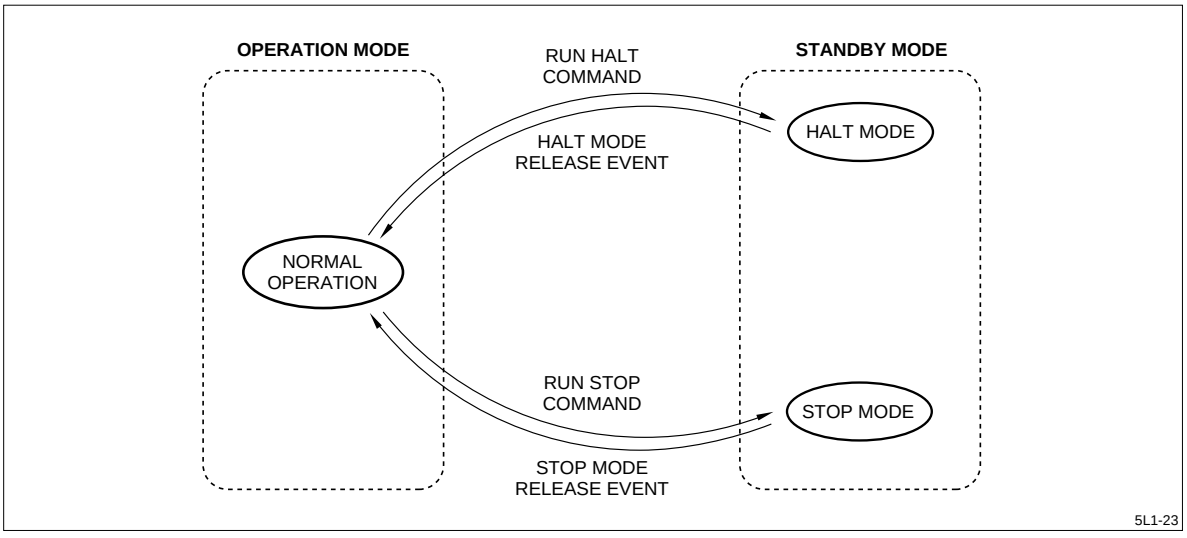


Figure 23. Operation Shift of Program

RELEASE FROM THE STANDBY MODE TO THE OPERATION MODE

Release from the standby mode to the operation mode is based on an interrupt request from the INTA pin or divider overflow. However, the reset is limited to a nonmaskable interrupt request.

The program restarts from step 0 on page 3. However, if the IME flag is set, the instruction at step 0 on page 3 is executed and a subroutine jump is performed to the interrupt processing routine specified on page 2 according to the type of interrupt.

Even if LOW level input on INTA pin is removed before 900 command cycles, the stop mode is released.

However, the program will not jump to 20_H page, interrupt process routine.

Interrupt request flag IFA is not set: the program continues at step 0 of 03_H page.

Interrupts

Interrupts originate from an INTA input or divider overflow. The IFA and IFD flags become interrupt request flags.

The interrupt block is composed of mask flags (RE0, RE2), the IME flag and interrupt processing circuit.

As shown in Figure 24, resetting a mask flag enables the interrupt request flag to be independently masked. Thus, the mask flags can be used in a program to establish the interrupt priority. The priority for interrupts generated simultaneously is shown in Table 5.

Table 5. Interrupt Event Summary

INTERRUPT REQUEST (REQUEST FLAG)	JUMP DESTINATION		PRIORITY ORDER	INTERRUPT ENABLE FLAG
	PAGE	STEP		
INTA input (IFA)	2	0	1	RE0
Divider overflow (IFD)	2	4	2	RE2

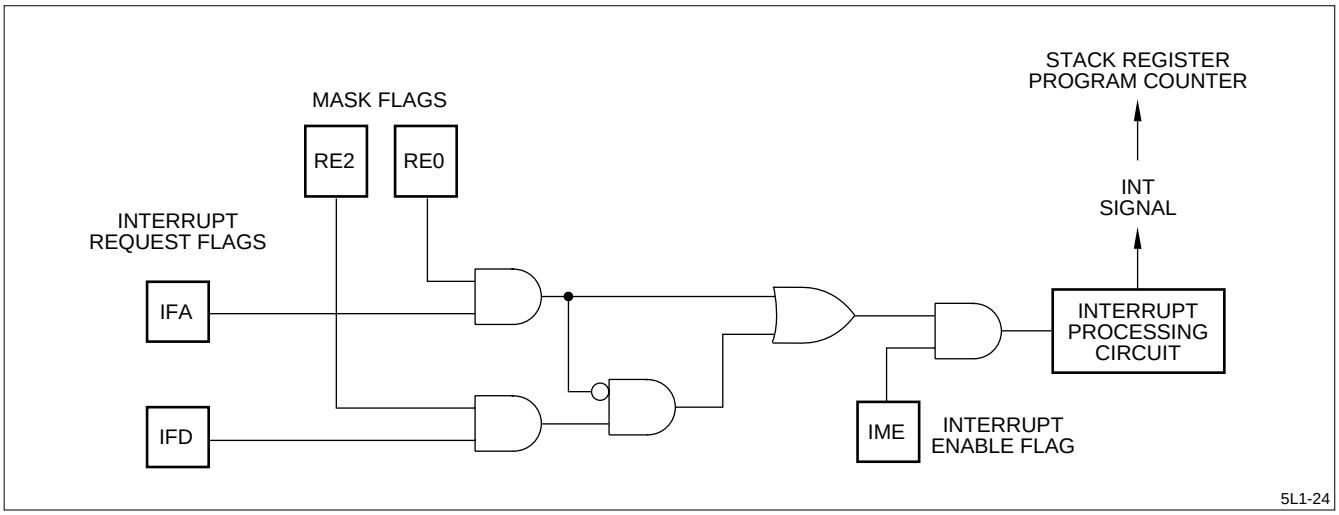


Figure 24. Interrupt Block

When the IME flag is set, the interrupt circuit activates according to the interrupt request and a subroutine jump is performed to the specified address. The jump destinations according to interrupt origin are shown in Table 5. When the IME flag is cleared, an interrupt is not accepted even if an interrupt request is generated. The interrupt timing is shown in Figure 25 and Figure 26. The timing chart in Figure 25 shows the interrupt enable state when an interrupt request has been generated. In this case, the interrupt processing signal INT goes HIGH, one instruction cycle after the interrupt request flag is set. When INT goes HIGH, the contents of the program counter are pushed into the stack register and execution jumps to the specified address. At this time, the INT signal and the IME flag are cleared to establish the interrupt disable mode. The IME flag is set again when the RTNI instruction is executed to establish the interrupt enable mode.

The timing chart shown in Figure 26 shows the state when interrupts are enabled while multiple interrupts are generated. In this case, a subroutine jump is performed according to the interrupt having the highest priority. When returning from the subroutine by executing the RTNI instruction, the instruction (two words are executed for a two-word instruction) at the location of return is executed and the interrupt for the next highest priority is accepted.

If an interrupt request is generated during execution of a two cycle instruction, the instruction is executed after which interrupt processing is performed. If consecutive LAX instructions are skipped or if the SKIP conditions are satisfied, the skip operation is terminated after which interrupt processing is performed.

NOTE: Figures 25 and 26 show non-masked interrupt request flags.

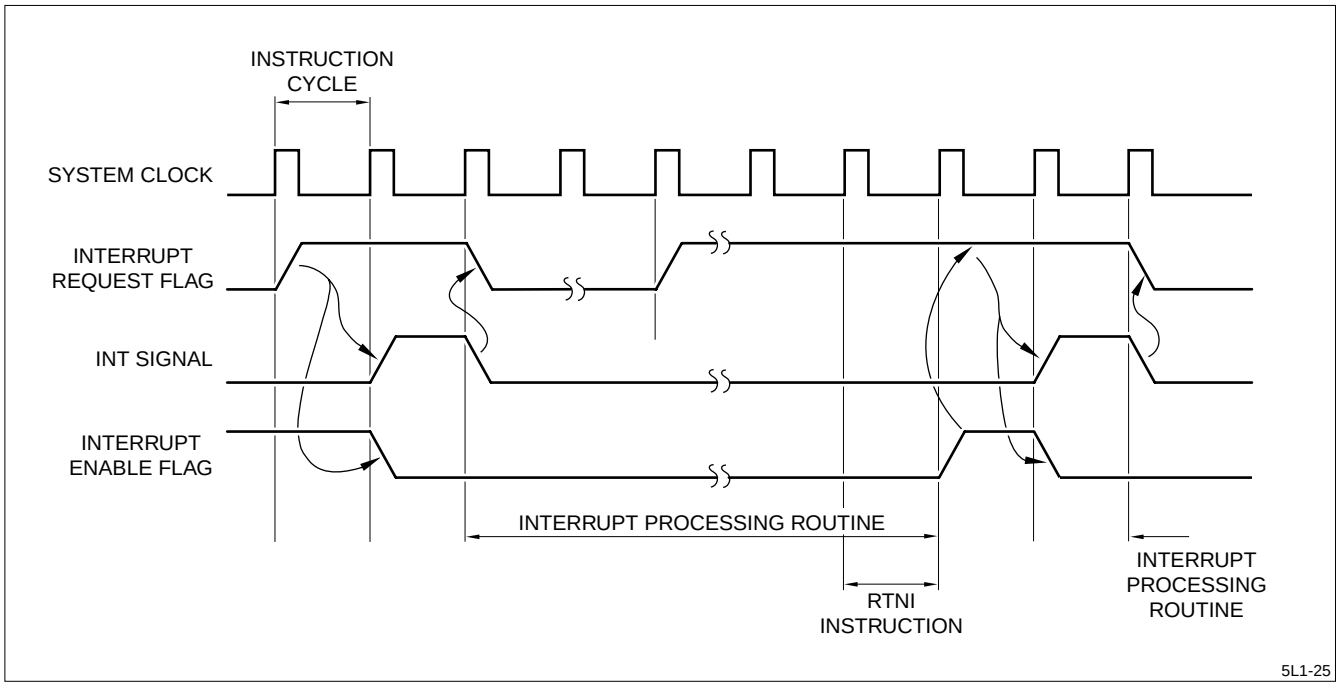


Figure 25. Interrupt Timing Chart

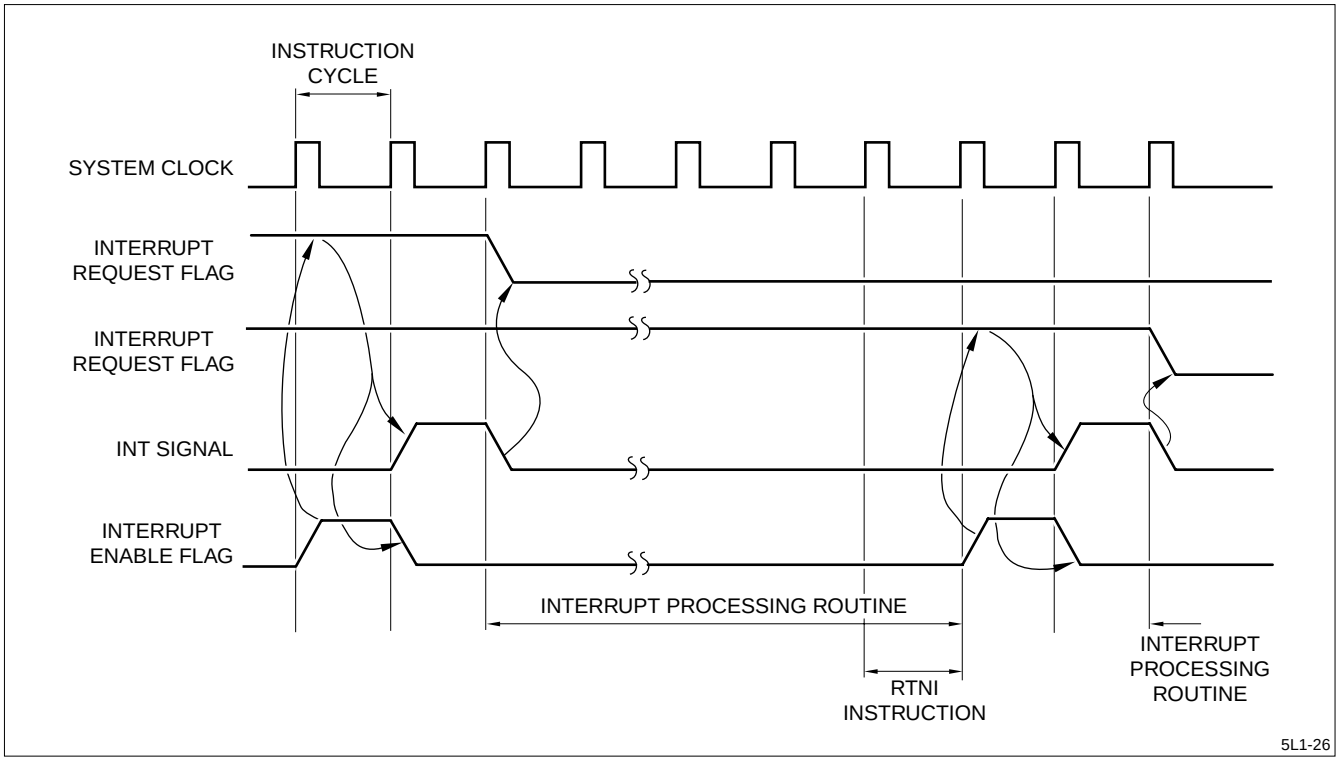


Figure 26. Interrupt Timing Chart

Hardware Reset Function

The hardware reset function mode is activated two instruction cycles after the falling edge from $\overline{\text{RESET}}$ pin. When the $\overline{\text{RESET}}$ pin is changed from HIGH to LOW, the pulse which is input by the OSC_{IN} pin is counter 2^{15} times after which the reset mode clears and the program counter starts from address 0 on page 0.

The initialized status of the system after reset is shown in Table 6.

The following reset functions are available:

- The I/O port is set as an input port and the mode register RD, RE and RF are cleared. The output only port (P0) is cleared and output LOW.
- The interrupt request flags (IFA, IFD) and the interrupt enable flag (IME) are cleared and all interrupts become disabled.
- The program counter start from step 0 on page 0.

For activate reset function, when power is turned on, you must connect a capacitor (0.1 µF, TYP.) across the $\overline{\text{RESET}}$ pin and GND.

Table 6. Reset Status

FLAG OR REGISTER, X REGISTER	STATUS[1]	NOTES
PC	0	
SP	Level 1	
RAM	Undefined	2
A_{CC}	Undefined	2
X register	Undefined	2
P0 - P2 output latch registers	0	
Divider	0	
IFA flag	0	
IFD flag	0	
IME flag	0	
C flag	Undefined	2
B_M, B_L registers	Undefined	2
Register RD (bit 1)	Undefined	2
Register RD (bit 0)	0	
Register RE (bit 2, 1, 0)	0	
Register RF (bit 3, 2, 1, 0)	0	

NOTES:
1. In reset mode and at program start.
2. Undefined flags and registers should be initialized by software.
3. When all P1 pins ($P1_0$ to $P1_3$) level goes to HIGH, the SM5Lx is programmed to reset operation (mask option).

LCD Function

DISPLAY SEGMENT

The SM5Lx contains a built-in circuit which directly drive a 1/4 duty, 1/2 bias LCD. A sample LCD pattern is shown in Figure 27.

A segment of the LCD can be turned on or off by setting the corresponding bit in the display RAM (see Figure 14) to '1' or '0'. The displayed segments can assume any configuration containing up to a maximum of 84/136/168 segments. An example of seven segment numeric display is shown in Figure 28.

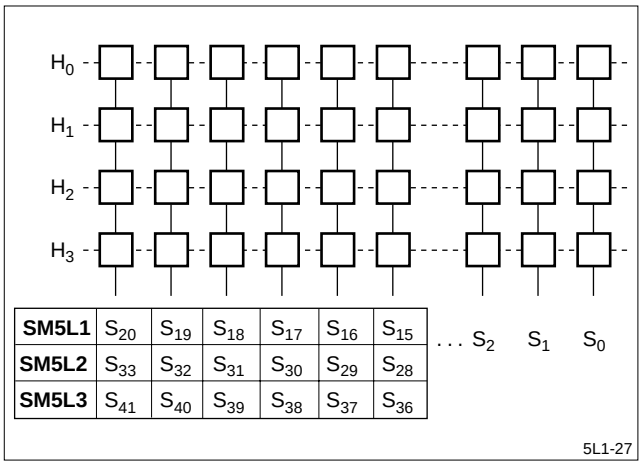


Figure 27. LCD Pattern

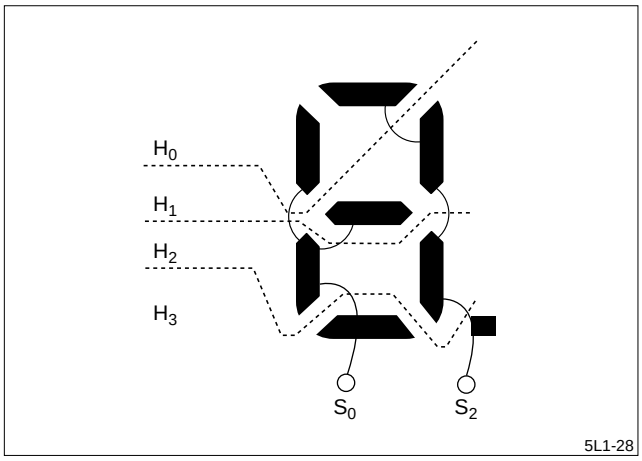


Figure 28. Sample LCD Pattern for Seven Segment Numeric Display

LCD DRIVE WAVEFORMS

The LCD drive waveforms for the LCD pattern of Figure 28 displaying a '5' are shown in Figure 29 (the segment output uses S_0 and S_1). For Figure 29, 3 V is applied to the V_{DD} pin, a 1.5 V is applied to the V_M pin.

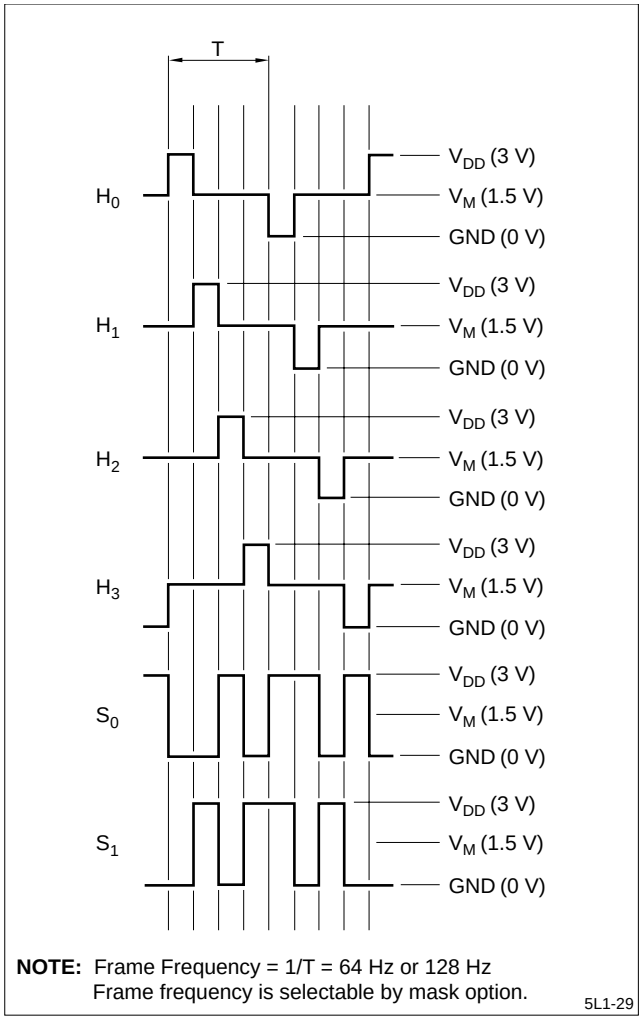


Figure 29. LCD Drive Waveforms

BOOSTER CIRCUIT

The device contains a booster circuit which generates a voltage two time higher than 1.5 V power supply.

It is necessary to apply external capacitors between DDC pin and V_{CC} pin as well as V_{DD} pin and GND (see Figure 30).

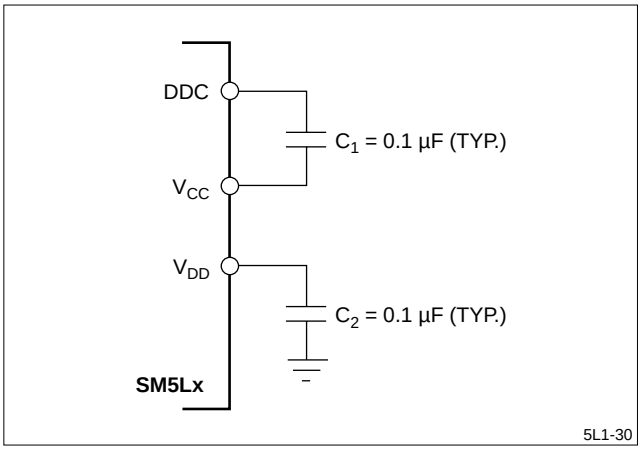


Figure 30. Booster Circuit

BLANK DISPLAY

There are two ways blank the entire display to match the purpose.

- Blanking the display for a short time
  - Set bit 0 of the RF register to '1': Display
  - Set bit 0 of the RF register to '0': Blank state
- Blanking the display for a long period mainly to reduce supply current.
  - Set bit 0 and 1 of the RF register to '1': Display
  - Set bit 0 and 1 of the RF register to '0': Blank state

When bit 1 of the RF register is set '0', the booster circuit does not operate and the common outputs and segment outputs are fixed to V_M level, and the display blanks. By cutting off the function of the booster circuit, the supply current can be greatly reduced. However, when the display is blanked using the second method, the response speed of the LCD returning to the display state drops slightly. The RF register is on the blank state after initialization (reset state) from hardware reset.

INSTRUCTION SET

Definition of Symbols

The following symbols are used in descriptions for the instructions.

SYMBOL	DEFINITION
M	Content of RAM at the address specified by the B register
←	Transfer direction
∪	Logical OR
∩	Logical AND
⊕	Logical XOR
Ai	ith bit of the A_{CC}
Push	Contents of the PC are decremented to the stack register
Pop	The decremented contents are transferred back to the PC
Pj	Pj register (j = 3, 2, 1, 0)
Rj	Rj register (j = F, E, D)
ROM ( )	ROM contents for address within ( )
Cy	Carry of ALU (different from the C flag)

- Each bit of a register can be represented. For example the ith bit of X register and R(0) register are represented as Xi and R(0) i. (i = 0, 1, 2, 3, …)
- Increment and decrement denote the binary addition of 1_H and F_H, respectively.
- To skip a certain instruction means that the instruction is ignored and that no operation is performed until the execution transfers to the next instruction. In other words, the instruction is regarded as a NOP instruction. Therefore, one cycle is required to skip a one-word instruction and two cycles are required to skip a two word instruction.

ROM Address Control Instructions

MNEMONIC	MACHINE CODE	OPERATIONS
TR x	80 to BF	$P_L \leftarrow x\ (I_5 - I_0)$
TL xy	E0 to EF 00 to FF	$P_U \leftarrow x\ (I_{11} - I_6)$ $P_L \leftarrow y\ (I_5 - I_0)$
TRS x	C0 to DF	Push, $P_U \leftarrow 01_H$, $P_L \leftarrow x\ (I_4, I_3, I_2, I_1, I_0, 0)$
CALL xy	F0 to FF 00 to FF	Push, $P_U \leftarrow x\ (I_{11} - I_6)$ $P_L \leftarrow y\ (I_5 - I_0)$
RTN	7D	Pop
RTNS	7E	Pop, skip the next step
RTNI	7F	Pop, IME ← 1

Data Transfer Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
LAX x	10 to 1F	$A_{CC} \leftarrow x\ (I_3 - I_0)$
LBMX x	30 to 2F	$B_M \leftarrow x\ (I_3 - I_0)$
LBLX x	20 to 2F	$B_L \leftarrow x\ (I_3 - I_0)$
LDA x	50 to 53	$A_{CC} \leftarrow M$, $B_{Mi} \leftarrow B_{Mi} \oplus \times (I_1 - I_0)$ (i = 1, 0)
EXC x	54 to 57	$M \leftrightarrow A_{CC}$, $B_{Mi} \leftarrow B_{Mi} \oplus \times (I_1 - I_0)$ (i = 1, 0)
EXCI x	58 to 5B	$M \leftrightarrow A_{CC}$, $B_L \leftarrow B_L + 1$ $B_{Mi} \leftarrow B_{Mi} \oplus \times (I_1 - I_0)$ (i = 1, 0) Skip if Cy =1 ($B_L = 0F_H \rightarrow 0$)
EXCD x	5C to 5F	$M \leftrightarrow A_{CC}$, $B_L \leftarrow B_L + 0F_H$ $B_{Mi} \leftarrow B_{Mi} \oplus \times (I_1 - I_0)$ (i = 1, 0) Skip if Cy =1 ($B_L = 0 \rightarrow 0F_H$)
EXAX	64	$A_{CC} \leftrightarrow X$
ATX	65	$x \leftarrow A_{CC}$
EXBM	66	$B_M \leftrightarrow A_{CC}$
EXBL	67	$B_L \leftrightarrow A_{CC}$
EX	68	$B \leftrightarrow SB$

Arithmetic Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
ADX x	00 to 0F	$A_{CC} \leftarrow A_{CC} + x\ (I_3 - I_0)$, Skip if Cy = 1
ADD	7A	$A_{CC} \leftarrow A_{CC} + M$
ADC	7B	$A_{CC} \leftarrow A_{CC} + M + C$, $C \leftrightarrow Cy$ Skip if Cy = 1
COMA	79	$A_{CC} \leftarrow \overline{A}_{CC}$
INCB	78	$B_L \leftarrow B_L + 1$, Skip if $B_L = 0F_H$
DECB	7C	$B_L \leftarrow B_L - 1$,Skip if $B_L = 0$

Test Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
TAM	6F	Skip if $A_{CC} = M$
TC	6E	Skip if C = 1
TM x	48 to 4B	Skip if Mi = 1 (i = 3 to 0)
TABL	6B	Skip if $A = B_L$
TPB x	4C to 4F	Skip if P (R) i = 1, ($i = I_1, I_0$)
TA	6C	Skip if IFA = 1 and (IFA ← 0)
TD	69 02	Skip if IFD = 1 and (IFT ← 0)

Bit Manipulation Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
SM x	44 to 47	Mi ← 1 (i = 3 to 0)
RM x	40 to 43	Mi ← 0 (i = 3 to 0)
SC	61	C ← 1
RC	60	C ← 0
IE	63	IME ← 1
ID	62	IME ← 0

I/O Control Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
INL	70	$A_{CC} \leftarrow$ P1i (i = 3 to 0)
OUTL	71	P0i $\leftarrow A_{CC}$ (i = 3 to 0)
ANP	72	Pj $\leftarrow$ Pj $\cap A_{CC}$ (j = 3 to 0)
ORP	73	Pj $\leftarrow$ Pj $\cup A_{CC}$ (j = 3 to 0)
IN	74	$A_{CC} \leftarrow$ Pj (j = 3, 2, 1)
OUT	75	Pj $\leftarrow A_{CC}$ (j = 3 to 0), Rj $\leftarrow A_{CC}$ (j = F to D)

Table Reference Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
PAT	6A 00 to FF	Push $P_U \leftarrow (0, 4)$, P_L (X_1, X_0, A_{CC}) (X, A_{CC}) $\leftarrow I_7 - I_0$ Pop

Divider Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
DR	69 03	DIV ($f_7 - f_0$) Reset
DTA	69 04	$A_{CC} \leftarrow$ Divider ($f_3 - f_0$)

Melody Control Instruction

MNE-MONIC	MACHINE CODE	OPERATIONS
PRE	6D	Melody ROM pointer preset Melody ROM pointer ← X, A

Special Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
STOP	76	Standby mode (STOP)
HALT	77	Standby mode (HALT)
NOP	00	No operation

SYSTEM CONFIGURATION EXAMPLES

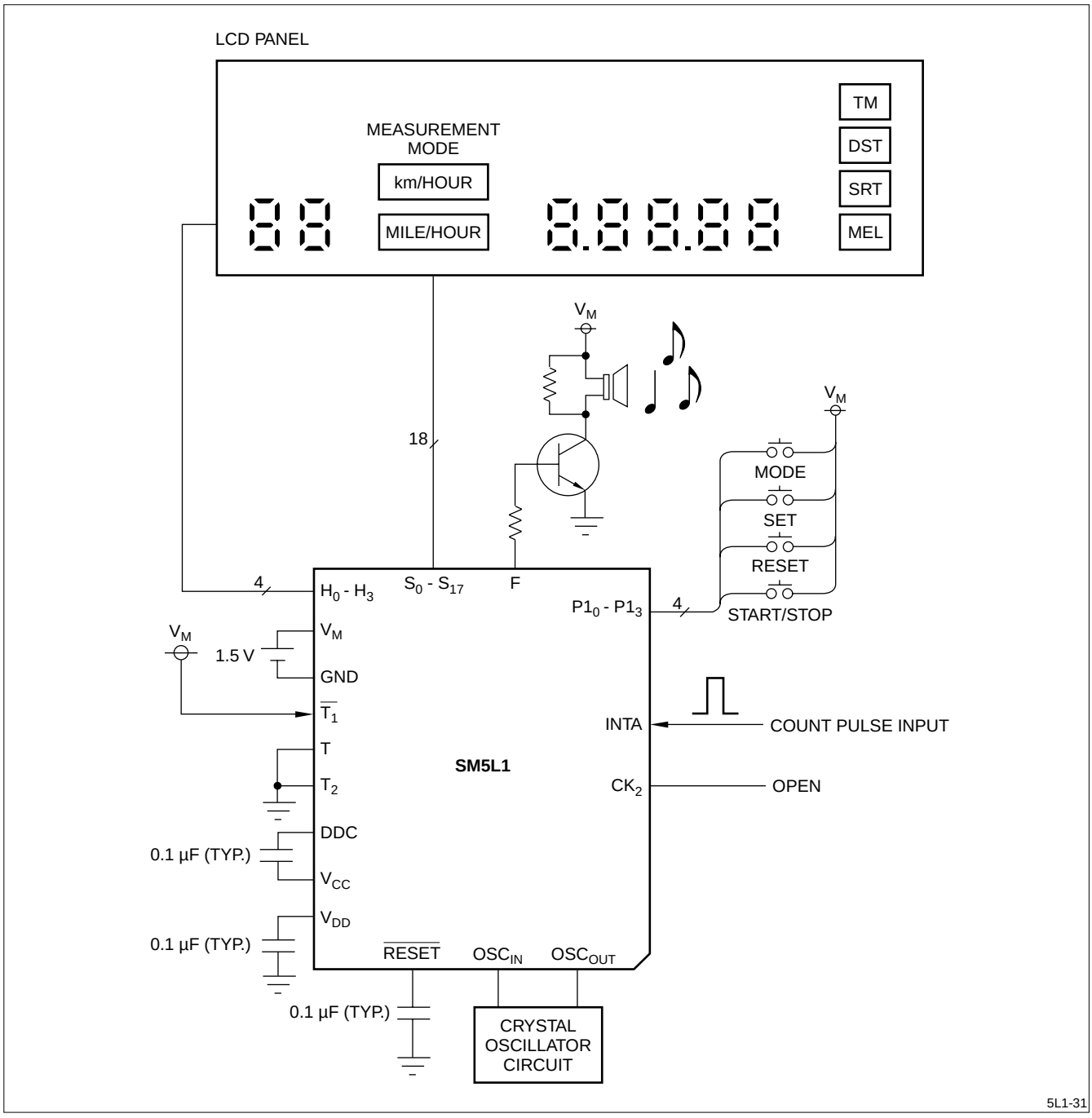


Figure 31. Sports Watch Example

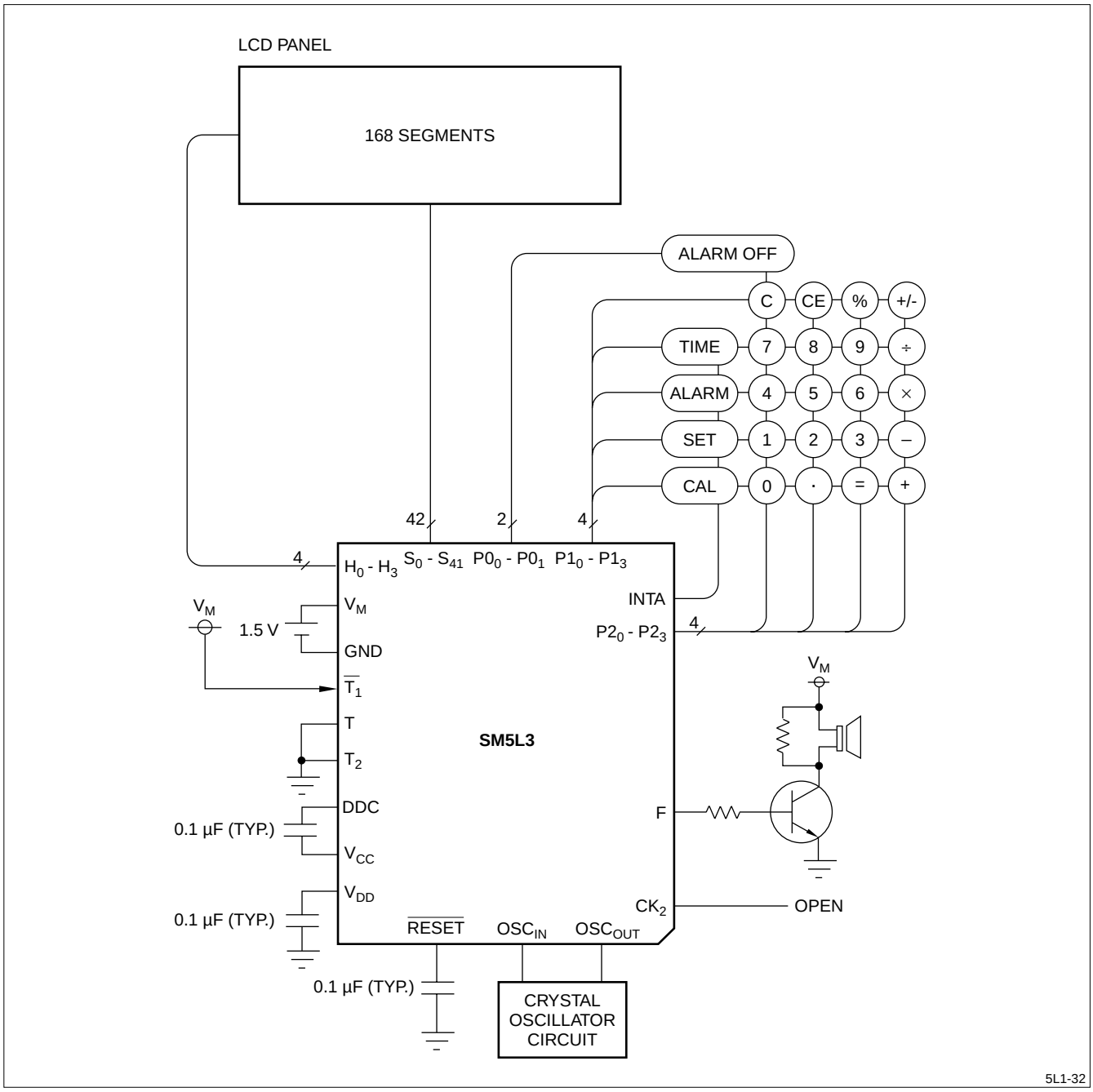


Figure 32. Watch and Calculator Example

LIFE SUPPORT POLICY

SHARP components should not be used in medical devices with life support functions or in safety equipment (or similiar applications where component failure would result in loss of life or physical harm) without the written approval of an officer of the SHARP Corporation.

LIMITED WARRANTY

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