



SM802110

ClockWorks™ CPRI 153.6MHz
Ultra-Low Jitter, LVPECL
Frequency Synthesizer

General Description

The SM802110 is a member of the ClockWorks™ family of devices from Micrel and provides an extremely low-noise timing solution for CPRI clock signals. It is based upon a unique patented RotaryWave® architecture that provides very low phase noise.

The device operates from a 3.3V or 2.5V power supply and synthesizes an LVPECL output clock at 153.6MHz. The SM802110 accepts a 30.72MHz LVCMOS reference clock.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

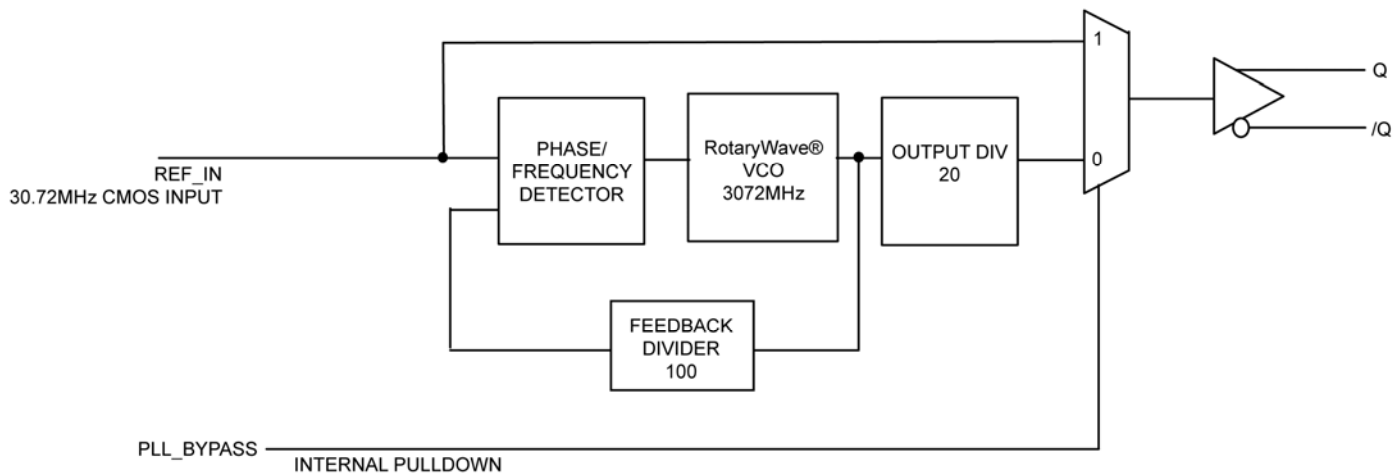
Features

- Generates an LVPECL clock outputs at 153.6MHz
- 2.5V or 3.3V operating range
- Typical phase jitter @ 153.6MHz (2MHz to 20MHz): 99fs (typical) at 3.3V
- Industrial temperature range
- Green, RoHS, and PFOS compliant
- Available in 24-pin 4x4mm QFN

Applications

- CPRI
- OBSAI

Block Diagram



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RotaryWave is a registered trademark of Multigig, Inc.

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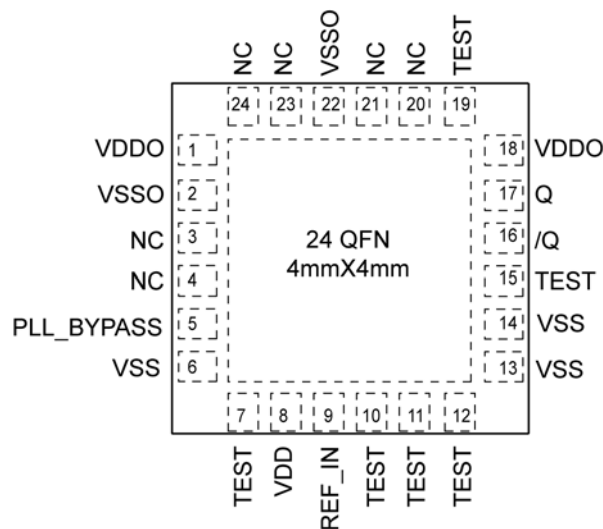
Ordering Information

| Part Number | Marking | Shipping | Junction Temperature Range ⁽¹⁾ | Package |
|--------------|---------|-------------|---|------------|
| SM802110UMG | 802110 | Tube | -40°C to +85°C | 24-Pin QFN |
| SM802110UMGR | 802110 | Tape & Reel | -40°C to +85°C | 24-Pin QFN |

Note:

1. Devices are Green, RoHS, and PFOS compliant.

Pin Configuration



**24-Pin QFN
(Top View)**

Pin Description

| Pin Number | Pin Name | Pin Type | Pin Level | Pin Function |
|-----------------------|------------|----------|-----------|--|
| 16, 17 | /Q, Q | O, (DIF) | LVPECL | Differential Clock Output |
| 1, 18 | VDDO | PWR | | Power Supply for Clock Output |
| 2, 22 | VSSO | PWR | | Power Supply Grounds for Clock Output |
| 3, 4, 20, 21, 23, 24 | NC | | | No Connect, Do not connect anything to these pins. |
| 5 | PLL_BYPASS | I, (SE) | LVC MOS | PLL Bypass, Selects Output Source 0 = Normal PLL Operation 1 = Output from Input Reference Clock 45KΩ pull-down |
| 7, 10, 11, 12, 15, 19 | TEST | | | Factory Test Pins. Do not connect anything to these pins. |
| 8 | VDD | PWR | | Core Power Supply |
| 9 | REF_IN | I, (SE) | LVC MOS | Reference Clock Input |
| 6, 13, 14 | VSS | PWR | | Core Power Supply Ground. |

Absolute Maximum Ratings⁽¹⁾

| | |
|---|---------------------------|
| Supply Voltage (V_{DD} , V_{DDO}) | +4.6V |
| Input Voltage (V_{IN}) | -0.50V to $V_{DD} + 0.5V$ |
| Lead Temperature (soldering, 20sec.) | 260°C |
| Case Temperature | 115°C |
| Storage Temperature | -65°C to +150°C |

Operating Ratings⁽²⁾

| | |
|--|--------------------|
| Supply Voltage (V_{DD} , V_{DDO}) | +2.375V to +3.465V |
| Ambient Temperature (T_A) | -40°C to +85°C |
| Junction Thermal Resistance ⁽³⁾ | |
| QFN (θ_{JA}) | |
| Still-Air | 50°C/W |
| QFN (ψ_{JA}) | |
| Junction-to-Board | 30°C/W |

DC Electrical Characteristics⁽⁴⁾

$V_{DD} = V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|----------------------|------------------------------------|--------------|-------|------|-------|-------|
| V_{DD} , V_{DDO} | 2.5V Operating Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{DD} , V_{DDO} | 3.3V Operating Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DD} | Supply current, $V_{DD} + V_{DDO}$ | Outputs open | | 77 | 98 | mA |

LVPECL DC Electrical Characteristics⁽⁴⁾

$V_{DD} = V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$. $R_L = 50\Omega$ to $V_{DDO} - 2V$

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|-------------|----------------------|-----------|-------------------|------------------|-------------------|-------|
| V_{OH} | Output High Voltage | | $V_{DDO} - 1.145$ | $V_{DDO} - 0.97$ | $V_{DDO} - 0.845$ | V |
| V_{OL} | Output Low Voltage | | $V_{DDO} - 1.945$ | $V_{DDO} - 1.77$ | $V_{DDO} - 1.645$ | V |
| V_{SWING} | Output Voltage Swing | | 0.6 | 0.8 | 1.0 | V |

Note:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.
4. The circuit is designed to meet the AC and DC specifications shown in the above table(s) after thermal equilibrium has been established.

LVC MOS (PLL_BYPASS) DC Electrical Characteristics⁽⁴⁾

$V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|----------|--------------------|--------------------------------|------|------|----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | $V_{DD} = V_{IN} = 3.465V$ | | | 150 | μA |
| I_{IL} | Input Low Current | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5 | | | μA |

REF_IN DC Electrical Characteristics⁽⁴⁾

$V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|----------|--------------------|--|------|------|----------------|---------|
| V_{IH} | Input High Voltage | | 1.1 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.6 | V |
| I_{IN} | Input Current | $V_{DD} = 3.465V, V_{IN} = 0V$ to V_{DD} | -5 | | 5 | μA |

AC Electrical Characteristics^(4, 5)

$V_{DD} = V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

$V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

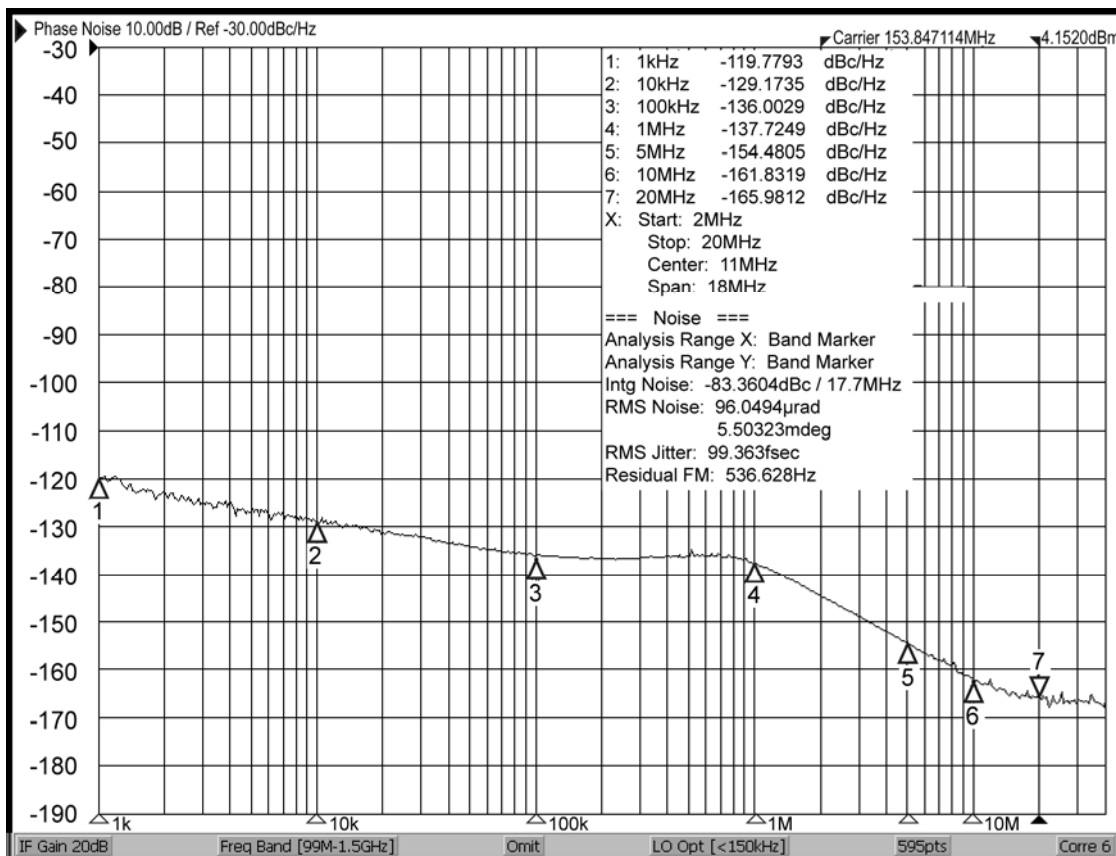
$T_A = -40^\circ C$ to $+85^\circ C$. $R_L = 50\Omega$ to $V_{DDO} - 2V$

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|----------------------|---------------------------------|---|------|-------|------|-------|
| F_{OUT} | Output Frequency | | | 153.6 | | MHz |
| F_{REF} | Reference Input Frequency | | | 30.72 | | MHz |
| T_R/T_F | LVPECL Output Rise/Fall Time | 20% – 80% | 80 | 175 | 350 | ps |
| ODC | Output Duty Cycle | | 48 | 50 | 52 | % |
| T_{LOCK} | PLL Lock Time | | | | 20 | ms |
| $T_{jit}(\emptyset)$ | RMS Phase Jitter ⁽⁶⁾ | Output = 153.6 MHz Integration Range (2MHz – 20MHz) | | 99 | | fs |
| | Spurious Noise Components | 30.72MHz | | -70 | | dBc |

Notes:

- All phase noise measurements were taken with an Agilent 5052B phase noise system.
- Ref_IN driven with a low noise source ClockWorks SM802001 programmed for a 30.77MHz CMOS output.

Phase Noise Plot



153.8MHz 2MHz-20MHz 99fS
Output is 153.85MHz with a 30.77MHz Input

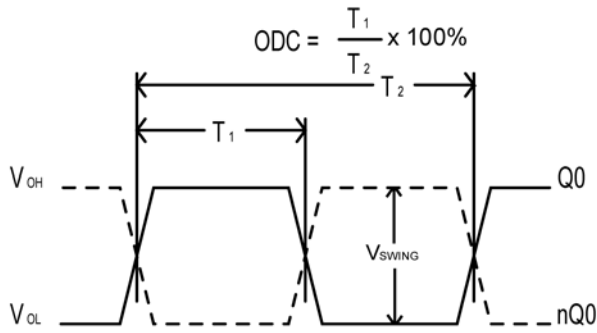


Figure 1. Duty Cycle Timing

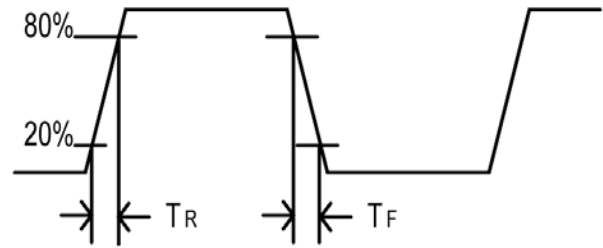


Figure 2. All Outputs Rise/Fall Time

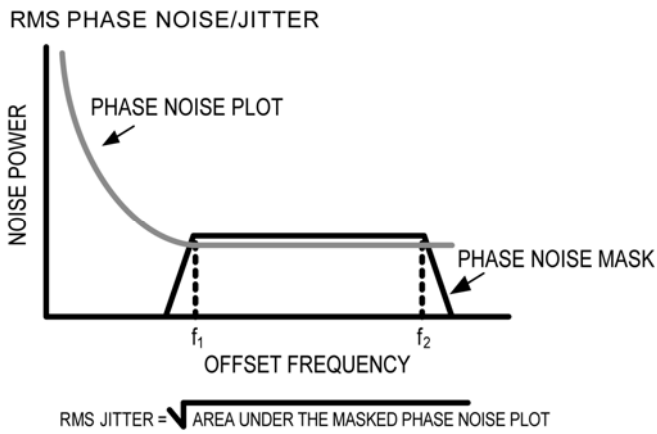


Figure 3. RMS Phase Noise/Jitter

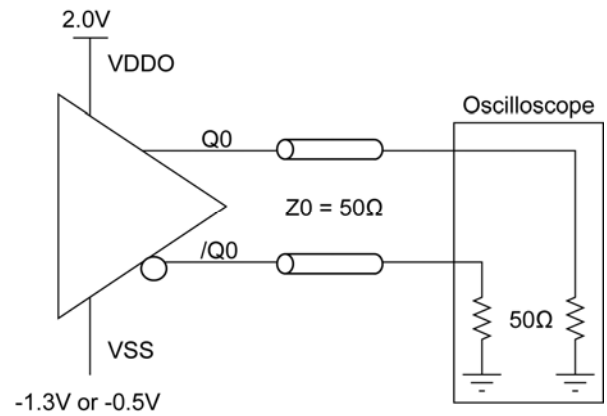
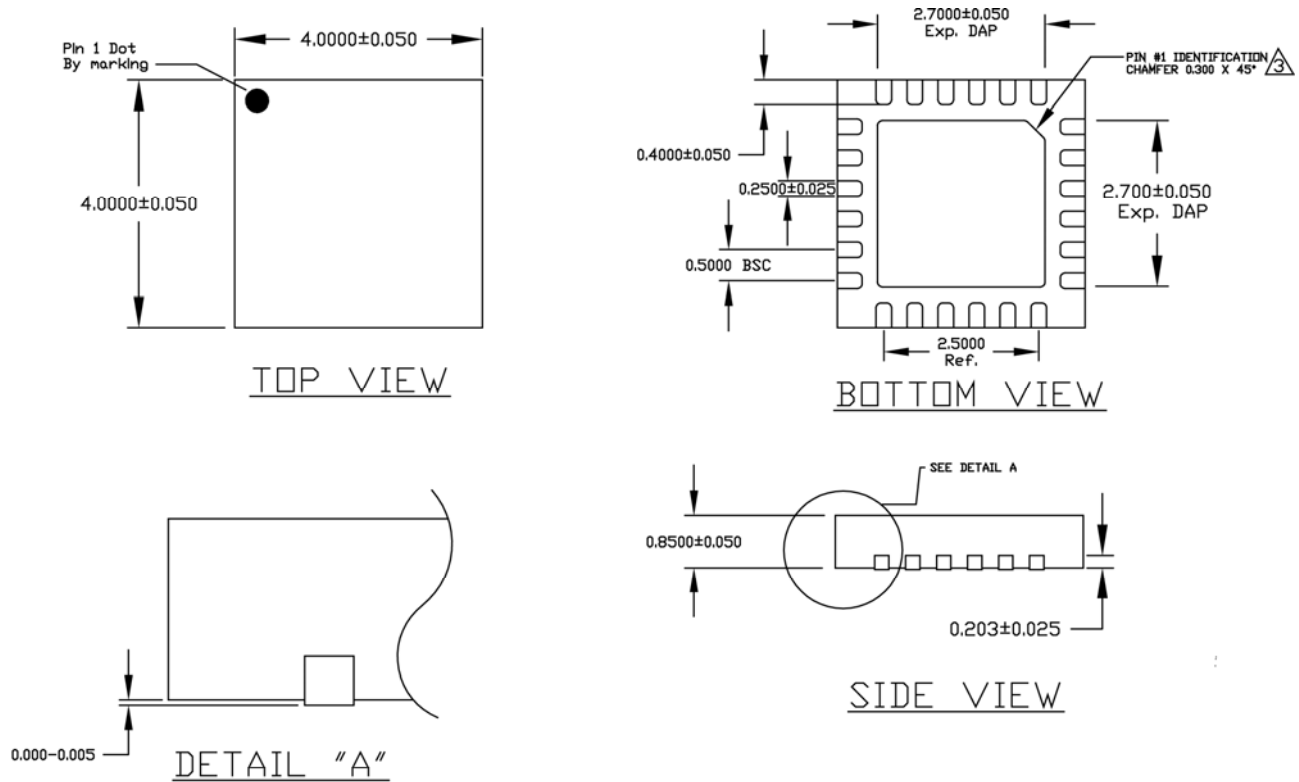


Figure 4. LVPECL Output Load and Test Circuit

Package Information



NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS (mm).
2. THE PIN#1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.

CHAMFER STYLE PIN 1 IDENTIFIER ON BOTTOM SIDE

24-Pin QFN

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