Product List

SM8951BL25, 25 MHz 4KB internal memory MCU
SM8951BC25, 25 MHz 4KB internal memory MCU
SM8951BC40, 40 MHz 4KB internal memory MCU

General Description

The SM8951B series product is an 8-bits single chip micro controller with 4KB flash embedded. It provides hardware features and a powerful instruction set, necessary to make it a versatile and cost effective controller for those applications demand up to 32 I/O pins or need up to 4KB flash memory either for program or for data or mixed. To program the flash block, a commercial programmer is cap-able to do it.

Ordering Information

SM8951BihhkL
yymmv

i: process identifier {L=3.0V~3.6V,C=4.5V~ 5.5V}
hh: working clock in MHz {25, 40}
k: package type postfix {as below table}
yy: year,
mm: month
v: version identifier {, A, B,...}
L:PB Free identifier
{No text is Non-PB Free，”P” is PB Free}

Feature

- Working voltage: 3.0V ~ 3.6V For L Version
- 4.5V ~ 5.5V For C Version
- General 8051 family compatible
- 12 clocks per machine cycle
- 4KB internal flash memory
- 128 bytes data RAM
- Two 16 bit timers/counters
- Four 8-bit I/O ports
- Full duplex serial channel
- Bit operation instruction
- Industrial Level
- 8-bit unsigned division
- 8-bit unsigned multiply
- BCD arithmetic
- Direct addressing
- Indirect addressing
- Nested interrupt
- Two priority level interrupt
- A serial I/O port
- Power save modes:
- Idle mode and power down mode
- Code protection function
- Strong Noise immunity
- One watch dog timer (WDT)
- Reduce EMI (inhibit ALE)

Postfix	Package	Pin / Pad Configuration
P	40L PDIP	Page 2
J	44L PLCC	Page 3
Q	44L QFP	Page 4

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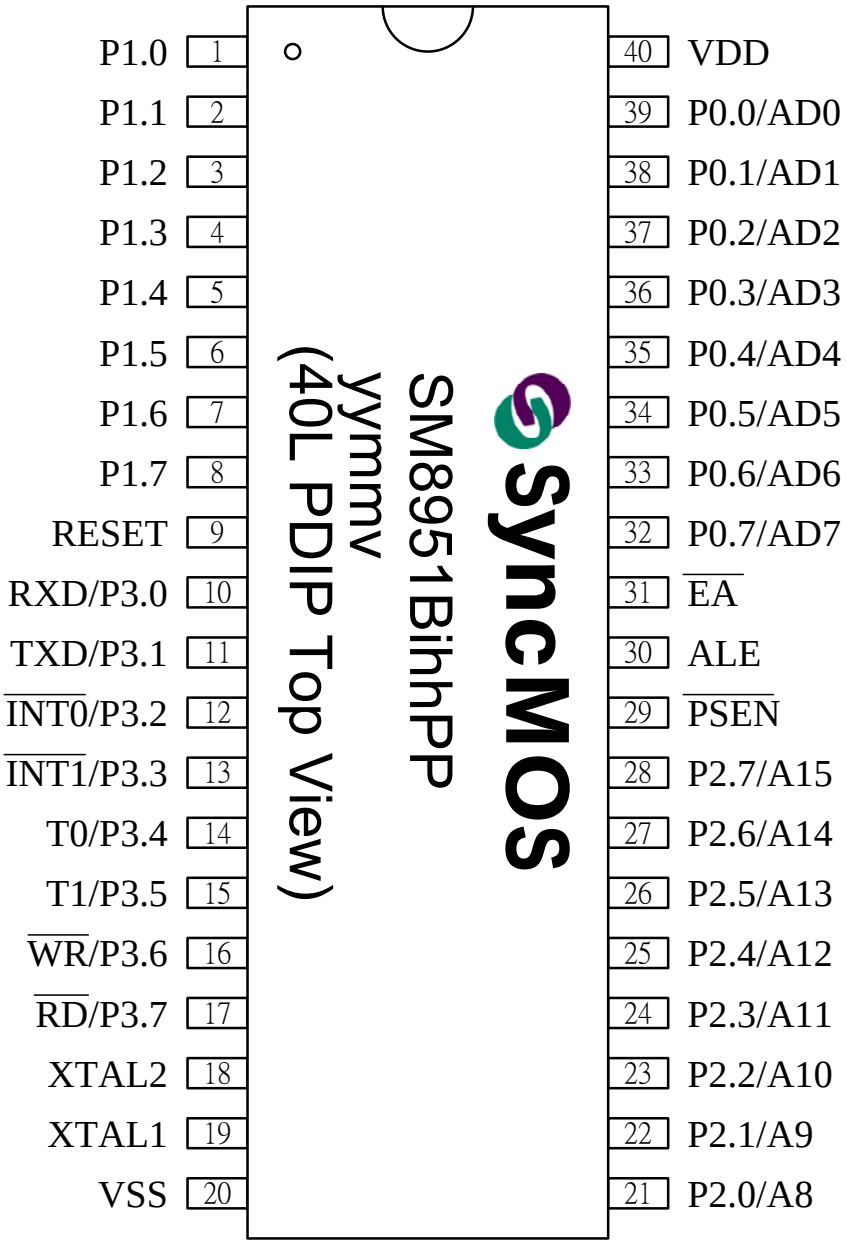
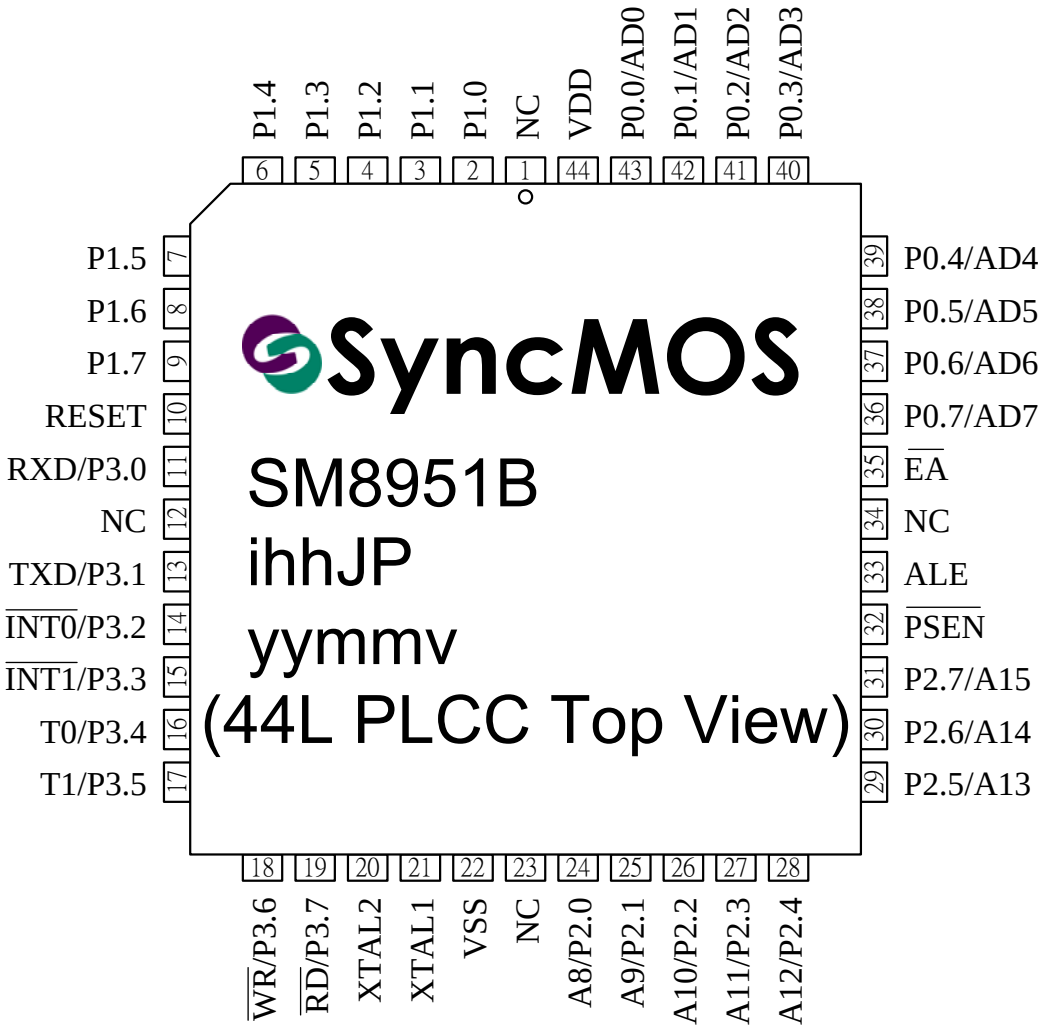
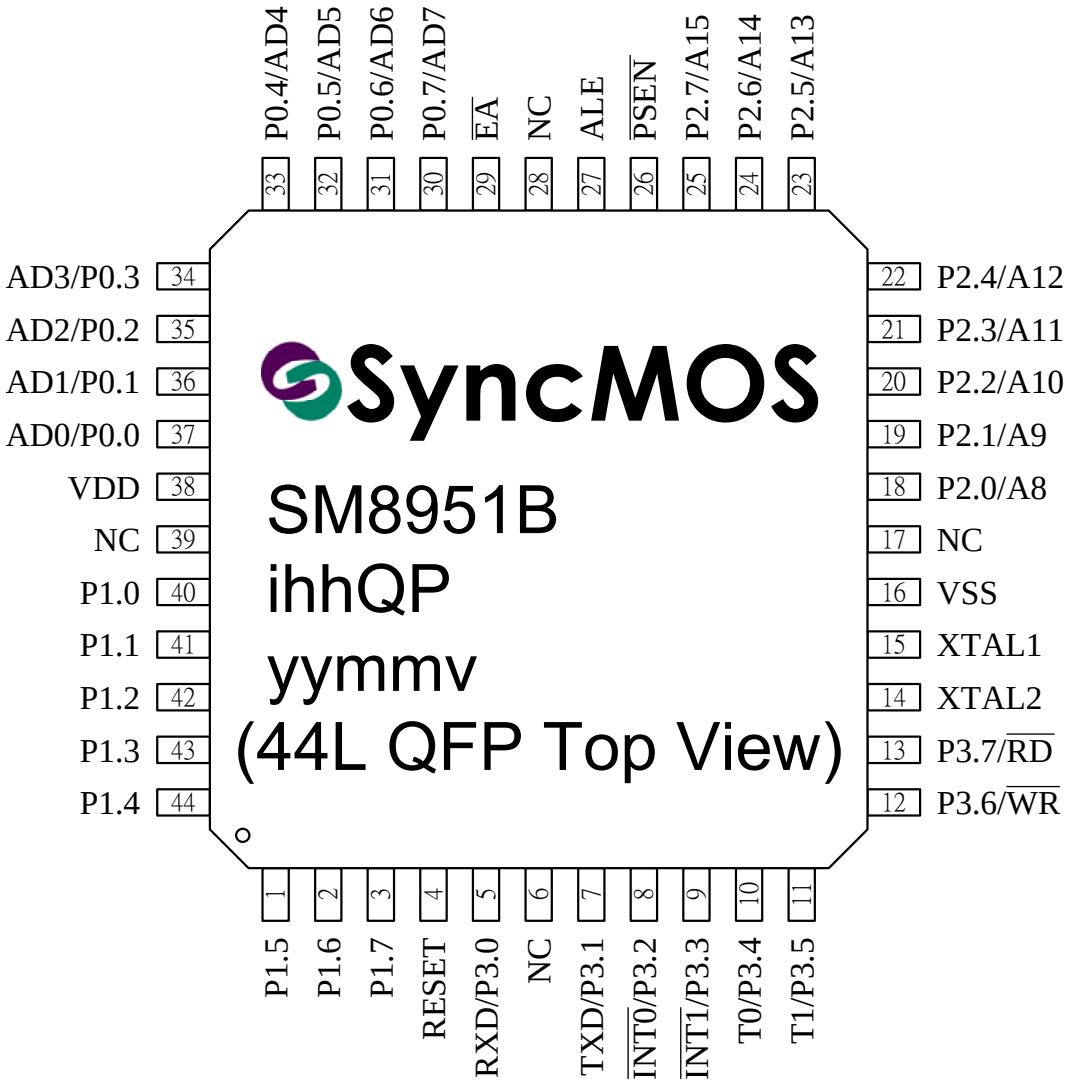
886-3-567-1894

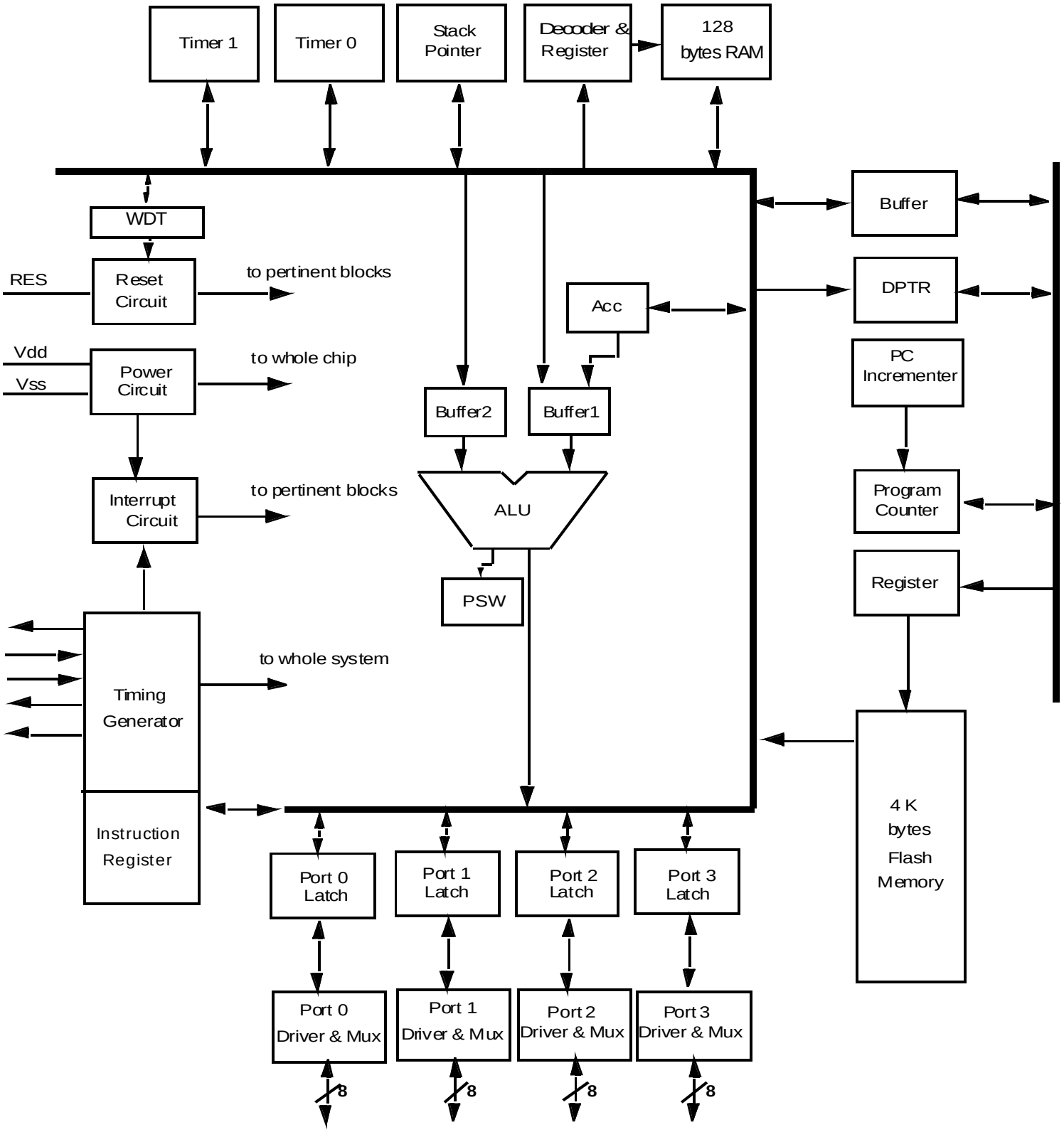
Pin Configuration




P1.4 6
P1.3 5
P1.2 4
P1.1 3
P1.0 2
NC 1
VDD 44
P0.0/AD0 43
P0.1/AD1 42
P0.2/AD2 41
P0.3/AD3 40
P1.5 7
P1.6 8
P1.7 9
RESET 10
RXD/P3.0 11
NC 12
TXD/P3.1 13
INT0/P3.2 14
INT1/P3.3 15
T0/P3.4 16
T1/P3.5 17
P0.4/AD4 39
P0.5/AD5 38
P0.6/AD6 37
P0.7/AD7 36
EA 35
NC 34
ALE 33
PSEN 32
P2.7/A15 31
P2.6/A14 30
P2.5/A13 29
WR/P3.6 18
RD/P3.7 19
XTAL2 20
XTAL1 21
VSS 22
NC 23
A8/P2.0 24
A9/P2.1 25
A10/P2.2 26
A11/P2.3 27
A12/P2.4 28
SyncMOS
SM8951B
ihhJP
yymmv
(44L PLCC Top View)


P0.4/AD4 33
P0.5/AD5 32
P0.6/AD6 31
P0.7/AD7 30
EA 29
NC 28
ALE 27
PSEN 26
P2.7/A15 25
P2.6/A14 24
P2.5/A13 23
AD3/P0.3 34
AD2/P0.2 35
AD1/P0.1 36
AD0/P0.0 37
VDD 38
NC 39
P1.0 40
P1.1 41
P1.2 42
P1.3 43
P1.4 44
SyncMOS
SM8951B
ihhQP
yymmv
(44L QFP Top View)
22 P2.4/A12
21 P2.3/A11
20 P2.2/A10
19 P2.1/A9
18 P2.0/A8
17 NC
16 VSS
15 XTAL1
14 XTAL2
13 P3.7/RD
12 P3.6/WR
1 P1.5
2 P1.6
3 P1.7
4 RESET
5 RXD/P3.0
6 NC
7 TXD/P3.1
8 INT0/P3.2
9 INT1/P3.3
10 T0/P3.4
11 T1/P3.5

Block Diagram



Pin Description

40L PDIP Pin	44L PQFP Pin	44L PLCC Pin	Symbol	Active	I/O	Names
1	40	2	P1.0		i/o	bit 0 of port 1
2	41	3	P1.1		i/o	bit 1 of port 1
3	42	4	P1.2		i/o	bit 2 of port 1
4	43	5	P1.3		i/o	bit 3 of port 1
5	44	6	P1.4		i/o	bit 4 of port 1
6	1	7	P1.5		i/o	bit 5 of port 1
7	2	8	P1.6		i/o	bit 6 of port 1
8	3	9	P1.7		i/o	bit 7 of port 1
9	4	10	RES	H	i	Reset
10	5	11	P3.0/RXD		i/o	bit 0 of port 3 & Receive data
11	6	13	P3.1/TXD		i/o	bit 1 of port 3 & Transmit data
12	7	14	P3.2/#INT0	L/ -	i/o	bit 2 of port 3 & low true interrupt 0
13	8	15	P3.3/#INT1	L/ -	i/o	bit 3 of port 3 & low true interrupt 1
14	9	16	P3.4/T0		i/o	bit 4 of port 3Timer 0
15	10	17	P3.5/T1		i/o	bit 5 of port 3 & Timer 1
16	11	18	P3.6/#WR	L/ -	i/o	bit 6 of port 3 & external memory write
17	12	19	P3.7/#RD	L/ -	i/o	bit 7 of port 3 & external memory read
18	13	20	XTAL2		o	Crystal out
19	14	21	XTAL1		i	Crystal in
20	15	22	VSS			Sink Voltage, Ground
21	16	24	P2.0/A8		i/o	bit 0 of port 2 & bit 8 of external memory address
22	19	25	P2.1/A9		i/o	bit 1 of port 2 & bit 9 of external memory address
23	20	26	P2.2/A10		i/o	bit 2 of port 2 & bit 10 of external memory address
24	21	27	P2.3/A11		i/o	bit 3 of port 2 & bit 11 of external memory address
25	22	28	P2.4/A12		i/o	bit 4 of port 2 & bit 12 of external memory address
26	23	29	P2.5/A13		i/o	bit 5 of port 2 & bit 13 of external memory address
27	24	30	P2.6/A14		i/o	bit 6 of port 2 & bit 14 of external memory address
28	25	31	P2.7/A15		i/o	bit 7 of port 2 & bit 15 of external memory address
29	26	32	#PSEN	L	o	Program Storage Enable
30	27	33	ALE	-	o	Address Latch Enable
31	29	35	#EA	L	i	External Access(If you are not using external memory, please keep this pin to VCC)
32	30	36	P0.7/AD7		i/o	bit 7 of port 0 & data/address bit 7 of external memory
33	31	37	P0.6/AD6		i/o	bit 6 of port 0 & data/address bit 6 of external memory
34	32	38	P0.5/AD5		i/o	bit 5 of port 0 & data/address bit 5 of external memory
35	33	39	P0.4/AD4		i/o	bit 4 of port 0 & data/address bit 4 of external memory
36	34	40	P0.3/AD3		i/o	bit 3 of port 0 & data/address bit 3 of external memory
37	35	41	P0.2/AD2		i/o	bit 2 of port 0 & data/address bit 2 of external memory
38	36	42	P0.1/AD1		i/o	bit 1 of port 0 & data/address bit 1 of external memory
39	37	43	P0.0/AD0		i/o	bit 0 of port 0 & data/address bit 0 of external memory
40	38	44	VDD			Drive Voltage, Vcc

Table 1 SFR Map

$F8									$FF
$F0	B 0000 0000								$F7
$E8									$EF
$E0	ACC 0000 0000								$E7
$D8									$DF
$D0	PSW 0000 0000								$D7
$C8									$CF
$C0									$C7
$B8	IP 0000 0000							**SCONF** 0000 0000	$BF
$B0	P3 1111 1111								$B7
$A8	IE 0000 0000								$AF
$A0	P2 1111 1111								$A7
$98	SCON 0000 0000	SBUF xxxx xxxx						**WDTC** 0000 0000	$9F
$90	P1 1111 1111								$97
$88	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000			$8F
$80	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000	(Reserved)			PCON 0000 0000	$87

Target Spec.

Absolute Rating

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	℃	Ambient temperature under bias
VCC5	Supply voltage	4.5	5.0	5.5	V	
VCC3.3	Supply voltage	3.0	3.3	3.6	V	
Fosc 25	Oscillator Frequency			25	MHz	For 3.3V application
Fosc 40	Oscillator Frequency			40	MHz	For 5.0V application

DC Characteristic

VCC = 5V (±10%), VSS=0V TA= -40℃ to 85℃

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
VCC	Supply Voltage		4.5	5.5	V
ICC	Supply current operating	See notes 1 f_{CLK} = 12MHz VCC = 5.5V		20	mA
IID	Supply current IDLE Mode	See note 2 f_{CLK} = 12MHz VCC = 5.5V		6.5	mA
IPD	Supply current Power-Down MODE	See note 3；VCC (= 5.5V)		30	μA
	INPUT				
VIL1	Input LOW voltage, P0, P1, P2, P3, /EA		-0.5	0.8	V
VIL2	Input LOW voltage, RES, XTAL1		0	0.8	V
VIH1	Input HIGH voltage, P0, P1, P2, P3, /EA		2.0	Vcc+0.5	V
VIH2	Input HIGH voltage, RES, XTAL1		70%VCC	Vcc+0.5	V
IIL	Input current LOW level Port 1,2,3	VIN = 0.45V		-75	μA
ITL	Transition current High to Low Port 1,2,3	VIN = 2.0 V		-650	μA
ILI	Input leakage current ,Port 0	0.45V < VIN < VCC-0.3V		±10	μA
	OUTPUT				
VOL1	Output LOW voltage, Port 0,ALE, /PSEN	IOL = 8mA，VCC=5.0V		0.45	V
VOL2	Output LOW voltage, Port 1, 2, 3	IOL = 6.5mA，VCC =5.0V		0.45	V
VOH1	Output High voltage Port0 ALE, /PSEN	IOH = -800uA，VCC =5.0V	2.4		V
VOH2	Output High voltage Port 1,2,3	IOH = -60μA，VCC =5.0V	2.4		V
RRST	Internal RESET pull-down resistor		50	300	kΩ
CIO	Pin capacitance	Test freq=1MHz, TA=25℃		10	pF

VCC = 3.3V (±10%), VSS=0V , TA= -40℃ to 85℃

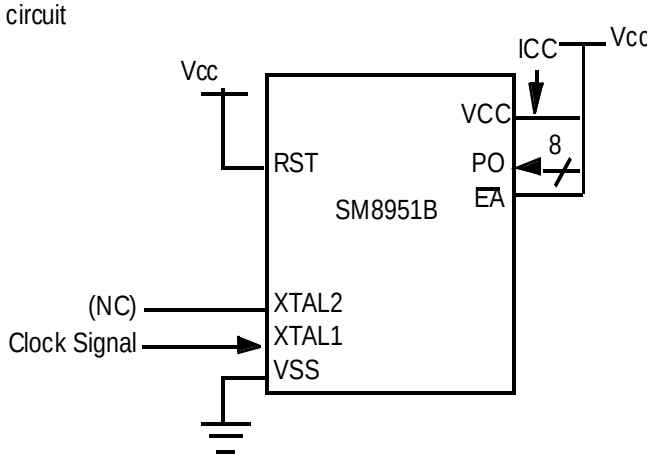
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
VCC	Supply Voltage		3.0	3.6	V
ICC	Supply current operating	See note 1 f_{CLK} = 12MHz VCC = 3.6V		10	mA
IID	Supply current IDLE Mode	See note 2 f_{CLK} = 12MHz VCC = 3.6V		5	mA
IPD	Supply current Power-Down MODE	See note 3；VCC (= 3.6V)		20	μA
	INPUT				
VIL1	Input LOW voltage, P0, P1, P2, P3, /EA	VCC = 3.6V	0	0.2 VCC -0.2	V
VIL2	Input LOW voltage, RST	VCC = 3.6V	0	0.2 VCC -0.2	V
VIL3	Input LOW voltage, XTAL1	VCC = 3.6V	0	0.2 VCC -0.2	V
VIH1	Input HIGH voltage, P0, P1, P2, P3, /EA	VCC = 3.6V	2.0	VCC + 0.2	V
VIH2	Input HIGH voltage, RST	VCC = 3.6V	2.0	VCC + 0.2	V
VIH3	Input HIGH voltage, XTAL1	VCC = 3.6V	0.8 VCC	VCC + 0.2	V
IIN1	Input current LOW level Port 1,2,3	VCC = 3.0V ~3.6V, VIN = 0.45V.	-10	50	μA

ITL	Transition current High to Low Port 1,2,3	See note 4 VCC = 3.6V, VIN = 2.0 V	-75	400	μA
ILI	Input leakage current P0, /EA	VCC = 3.0V ~3.6V, 0.45V<VIN<VCC	-10	10	μA
OUTPUT					
VOL1	Output LOW voltage, Port 0,ALE, /PSEN	IOL = 6mA，VCC =3.3V		0.4	V
VOL2	Output Low voltage Port 1,2,3	IOL = 5mA，VCC =3.3V		0.4	V
VOH1	Output High voltage Port0, ALE, /PSEN	IOH =-300uA，VCC =3.3V	2.4		V
VOH2	Output High voltage Port 1,2,3	IOH =-20μA，VCC =3.3V	2.4		V
ISK1	Sink Current Port 1, 2, 3	VCC = 3.3V, VIN = 0.4 V		6	mA
ISK2	Sink Current Port 0,ALE, /PSEN	VCC = 3.3V, VIN = 0.4 V		8	mA
ISR1	Source Current Port 1, 2, 3	VCC = 3.3V, VIN = 2.4 V		-80	uA
ISR2	Source Current Port 0,ALE, /PSEN	VCC = 3.3V, VIN = 2.4 V		-8	mA
RRST	Internal RESET pull-down resistor		50	300	kΩ
CIO	Pin capacitance	Test freq=1MHz, TA=25℃		10	pF

NOTES FOR DC ELECTRICAL CHARACTERISTICS

1. The operating supply current is measured with all output disconnected;
   XTAL1 driven with tr = tf = 5ns; VIL = VSS+0.5V; VIH=VCC-0.5V; XTAL2 not connect;
   /EA=RST=Port0=VDD;
2. The IDLE MODE supply current is measured with all output pins disconnected;
   XTAL1 driven with tr = tf = 5ns; VIL = VSS+0.5V; VIH=VCC-0.5V; XTAL2 not connect;
   /EA=Port0=VDD;
3. The POWER-DOWN MODE supply current is measured with all output pins disconnected;
   VIL = VSS+0.5V; VIH=VCC-0.5V; XTAL2 not connect; /EA= Port0=VDD;
4. Port 1, 2, 3, and 4 sources a transition current when they are being externally driven from HIGH to LOW. The transition current reaches its maximum value when VIN is approximately 2V.
5. Capacities loading on port 0 and 2 may cause spurious noise to be superimposed on VOL of ALE and port 1, 3, and 4. The noise is due to external bus capacitance discharging into port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt trigger STROBE input.

ICC Active mode test circuit



AC Characteristic

VCC=5.0V±10%, VSS=0V, tclk min = 1/ fmax(maximum operating frequency)
TA= -40℃ to +85℃
C_L=100pF for Port0, ALE and /PSEN; C_L=80pF for all other outputs unless otherwise specified.

Symbol	FIGURE	PARAMETER	MIN	MAX	UNIT
External Clock drive into XTAL1					
tCLK	4	Xtal1 Period	40(1)	-	ns
tCLKH	4	Xtal1 HIGH time	20	-	ns
tCLKL	4	Xtal1 LOW time	20	-	ns
tCLKR	4	XTAL1 rise time	-	10	ns
tLLIV	4	XTAL1 fall time	-	10	ns
tCYC	4	Controller cycle time = tCLK / 4	3.33	-	Ns

NOTES:
1. Operating at 25MHz.

Symbol	FIGURE	PARAMETER	MIN	MAX	UNIT
Program Memory					
1/tCLK	7	System clock frequency	3.0	25	MHz
tLHLL	7	ALE pulse width	2tCLK-40		ns
tAVLL	7	Address valid to ALE low	tCLK-40		ns
tLLAX	7	Address hold after ALE low	tCLK-30		ns
tLLIV	7	ALE LOW to valid instruction in		4tCLK-100	ns
tLLPL	7	ALE LOW to /PSEN LOW	tCLK-30		ns
tPLPH	7	/PSEN pulse width	3tCLK-45		ns
tPLIV	7	/PSEN LOW to valid instruction in		3tCLK-105	ns
tPXIX	7	Input instruction hold after /PSEN	0		ns
tPXIZ	7	Input instruction float after /PSEN		tCLK -25	ns
tAVIV	7	Address to valid instruction in		5tCLK-105	ns
tPLAZ	7	/PSEN low to address float		10	ns
Data Memory					
tAVLL	8,9	Address valid to ALE LOW	tCLK-40		ns
tLLAX	8,9	Address hold after ALE LOW	tCLK-35		ns
tRLRH	8	/RD pulse width	6tCLK-100		ns
tWLWH	9	/WR pulse width	6tCLK-100		ns
tRLDV	8	/RD LOW to valid data in		5tCLK-165	ns
tRHDX	8	Data hold after /RD	0		ns
tRHDZ	8	Data float after /RD		2tCLK-70	ns
tLLDV	8	ALE LOW to valid data in		8tCLK-150	ns
tAVDV	8	Address to valid data in		9tCLK-165	ns
tLLWL	8,9	ALE LOW to /RD or /WR LOW	3tCLK-50	3tCLK+50	ns
tAVWL	8,9	Address valid to /WR or /RD LOW	4tCLK-130		ns
tQVWX	9	Data valid to /WR transition	tCLK-50		ns
tQVWH	9	Data before /WR	7tCLK-150		ns
tWHQX	9	Data hold after /WR	tCLK-50		ns
tRLAZ	8	/RD LOW to address float		0	ns
tWHLH	8,9	/RD or /WR HIGH to ALE HIGH	tCLK-40	tCLK+40	ns
UART					
tXLXL	10	Serial port clock time	12tCLK		ns
tQVXH	10	Output data setup to clock rising edge	10tCLK-133		ns
tXHQX	10	Output data hold after clock rising edge	2tCLK-117		ns
tXHDX	10	Input data hold after clock rising edge	0		ns
tXHDV	10	Clock rising edge to input data valid		10tCLK-133	ns

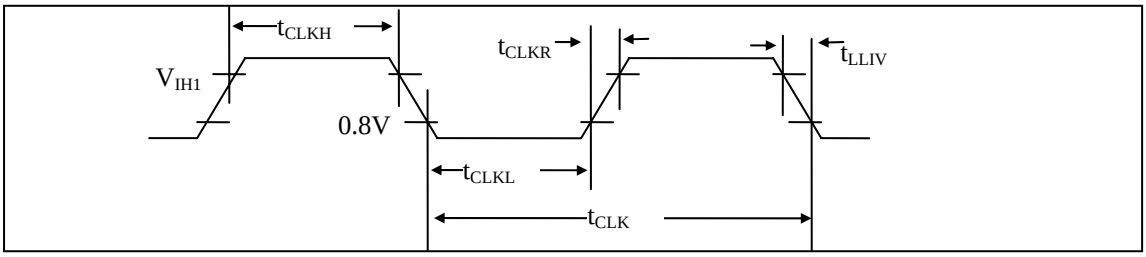


Figure 4 External Clock Drive waveform

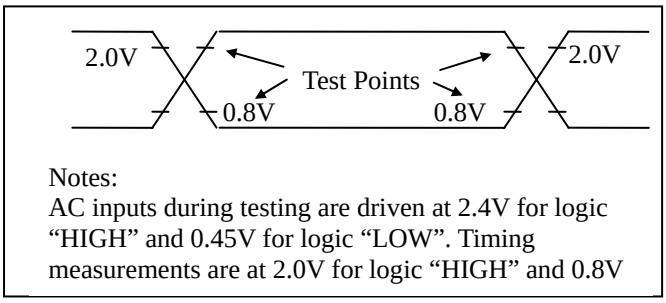


Figure 5 AC Testing Input/Output

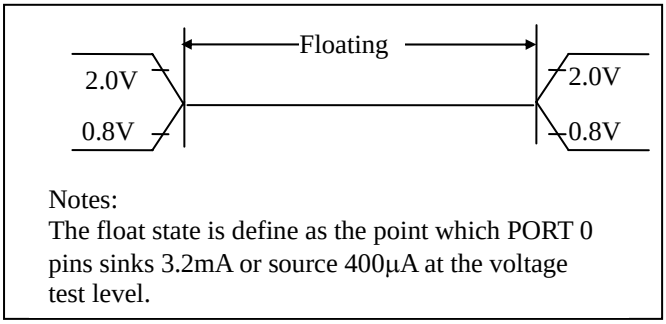


Figure 6 AC Testing, Floating Waveform

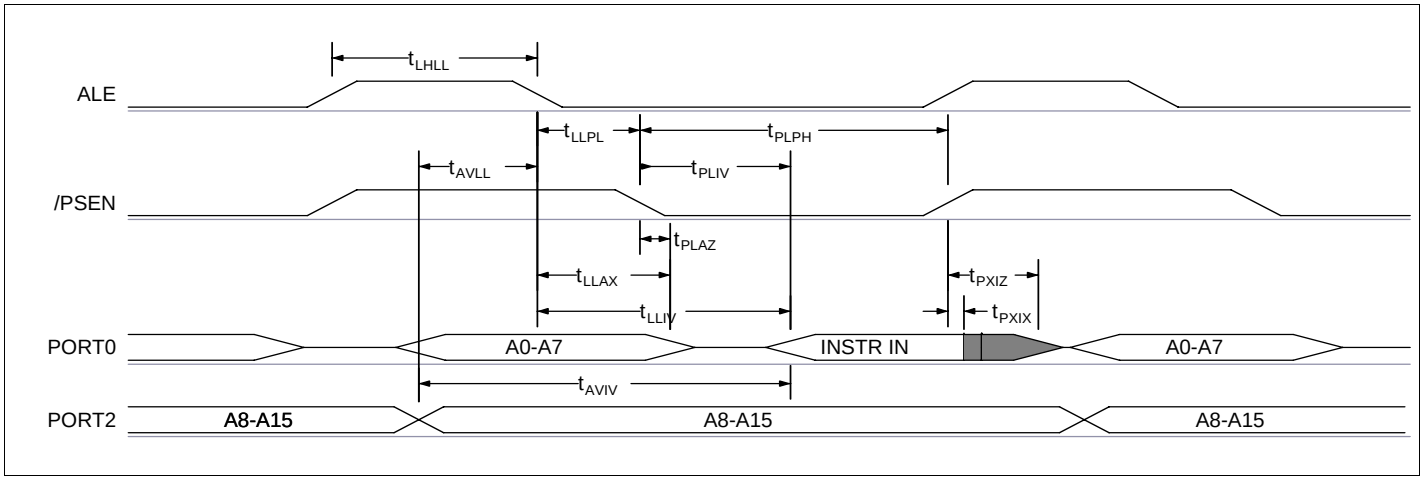


Figure 7 External Program Memory Read Cycle

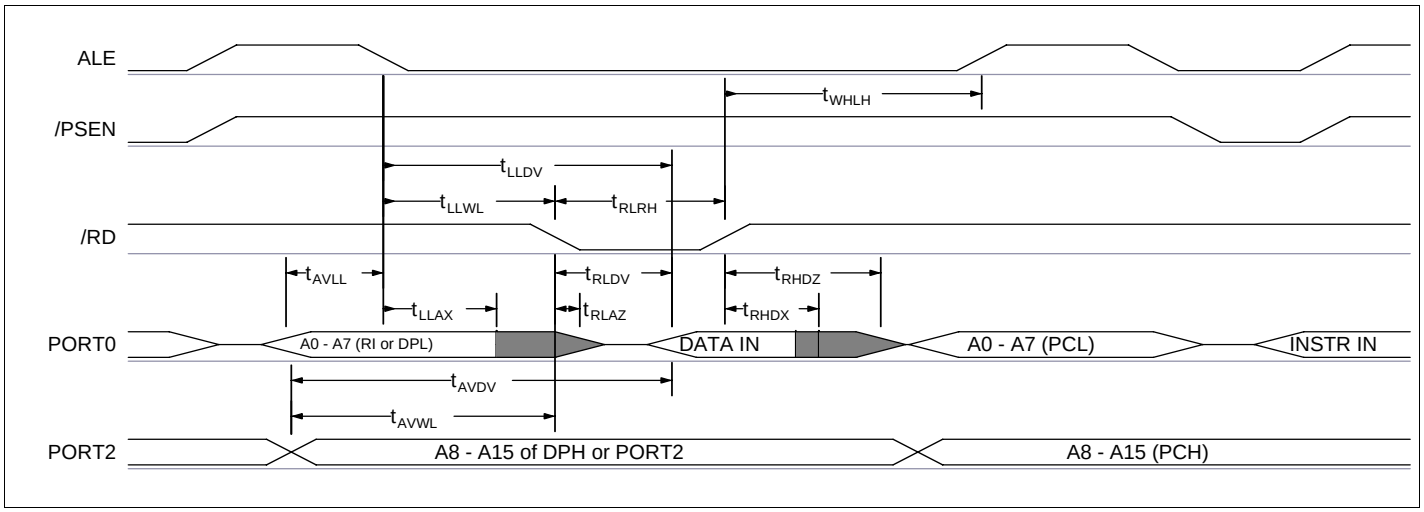


Figure 8 External Data Memory read cycle

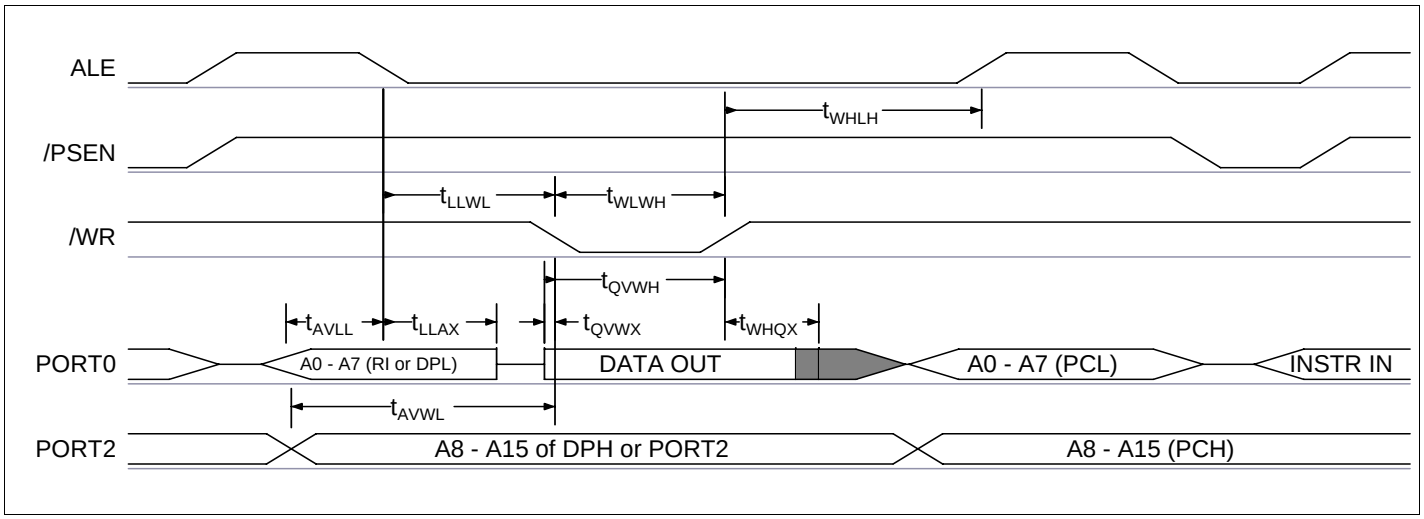


Figure 9 External Data Memory write cycle

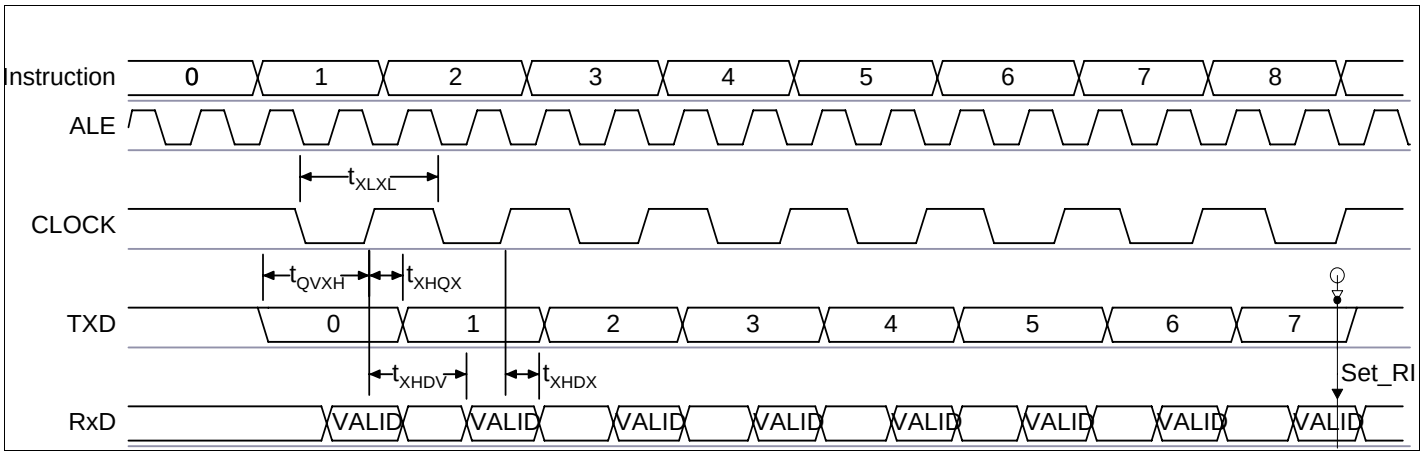


Figure10 UART waveform in Shift Register MODE

Instruction Set

The SM8951B uses the powerful instruction set of 80C51. It consists of 49 single-byte, 42 two-byte, and 15 three-byte instructions. Among them 63 instruction are executed in 1 machine-cycle, 46 instructions in 2 machine-cycles, and the multiply, 2 instructions in 4 machine-cycles.
A summary of the instruction set is given in Table 3.

Addressing Mode

Notes on instruction set and address modes:

Rn		Register R7-R0 of the currently selected register bank.
direct		8-bits internal data location's address. This could be internal DATA RAM location (0-127) or a SFR [i.e., I/O port, control register, status register, etc. (128-255)]
@Ri		8-bits RAM location addressed indirectly through register R1 or R0 of the actual register bank
#data		8-bits constant included in the instruction
#data16		16-bits constant included in the instruction
addr11		11-bits destination address. Used by ACALL and AJMP. The branch can be anywhere within the same 2 Kbytes page of program memory as the first byte of the following instruction.
rel		Signed (2's complement) 8-bits offset byte. Used by SJMP and all conditional jumps. Range is -128 to +127 bytes relative to first byte of the following instruction.
bit		Direct addressed bit in internal data RAM or SFR

Table 3: A Summary of the instruction set

Mnemonic		**OPERATION**	**BYTE**	**CYCLE**
Arithmetic Instructions				
ADD	A,Rn	A = A + Rn	1	1
ADD	A,direct	A = A + direct	2	1
ADD	A,@Ri	A = A + <@Ri>	1	1
ADD	A,#data	A = A + #data	2	1
ADDC	A,Rn	A = A + Rn + C	1	1
ADDC	A,direct	A = A + direct + C	2	1
ADDC	A,@Ri	A = A + @Ri + C	1	1
ADDC	A,#data	A = A + #data + C	2	1
SUBB	A,Rn	A = A – Rn – C	1	1
SUBB	A,direct	A = A – direct – C	2	1
SUBB	A,@Ri	A = A – <@Ri> – C	1	1
SUBB	A,#data	A = A – #data – C	2	1
INC	A	A = A + 1	1	1
INC	Rn	Rn = Rn + 1	1	1
INC	direct	direct = direct + 1	2	1
INC	@Ri	<@Ri> = <@Ri> + 1	1	1
DEC	A	A = A – 1	1	1
DEC	Rn	Rn = Rn – 1	1	1
DEC	direct	direct = direct – 1	2	1
DEC	@Ri	<@Ri> = <@Ri> – 1	1	1
INC	DPTR	DPTR = DPTR – 1	1	2
MUL	AB	B:A = A × B	1	4
DIV	AB	A = INT (A/B) B = MOD (A/B)	1	4
DA	A	Decimal adjust ACC	1	1
Logical Instructions				
ANL	A,Rn	A .AND. Rn	1	1
ANL	A,direct	A .AND. direct	2	1
ANL	A,@Ri	A .AND. <@Ri>	1	1
ANL	A,#data	A .AND. #data	2	1
ANL	direct,A	direct .AND. A	2	1
ANL	direct,#data	direct .AND. #data	3	2
ORL	A,Rn	A .OR. Rn	1	1
ORL	A,direct	A .OR. direct	2	1
ORL	A,@Ri	A .OR. <@Ri>	1	1

ORL	A,#data	A .OR. #data	2	1
ORL	direct,A	direct .OR. A	2	1
ORL	direct,#data	direct .OR. #data	3	2
XRL	A,Rn	A .XOR. Rn	1	1
XRL	A,direct	A .XOR. direct	2	1
XRL	A,@Ri	A .XOR. <@Ri>	1	1
XRL	A,#data	A .XOR. #data	2	1
XRL	direct,A	direct .XOR. A	2	1
XRL	direct,#data	direct .XOR. #data	3	2
CLR	A	A = 0	1	1
CPL	A	A = /A	1	1
RL	A	Rotate ACC Left 1 bit	1	1
RLC	A	Rotate Left through Carry	1	1
RR	A	Rotate ACC Right 1 bit	1	1
RRC	A	Rotate Right through Carry	1	1
SWAP	A	Swap Nibbles in A	1	1
Data Transfers Instructions				
MOV	A,Rn	A = Rn	1	1
MOV	A,direct	A = direct	2	1
MOV	A,@Ri	A = <@Ri>	1	1
MOV	A,#data	A = #data	2	1
MOV	Rn,A	Rn = A	1	1
MOV	Rn,direct	Rn = direct	2	2
MOV	Rn,#data	Rn = #data	2	1
MOV	direct,A	direct = A	2	1
MOV	direct,Rn	direct = Rn	2	2
MOV	direct,direct	direct = direct	3	2
MOV	direct,@Ri	direct = <@Ri>	2	2
MOV	direct,#data	direct = #data	2	1
MOV	@Ri,A	<@Ri> = A	1	1
MOV	@Ri,direct	<@Ri> = direct	2	2
MOV	@Ri,#data	<@Ri> = #data	2	1
MOV	DPTR,#data16	DPTR = #data16	3	2
MOVC	A,@A+DPTR	A = code memory[A+DPTR]	1	2
MOVC	A,@A+PC	A = code memory[A+PC]	1	2
MOVX	A,@Ri	A = external memory[Ri] (8-bits address)	1	2
MOVX	A,@DPTR	A = external memory[DPTR] (16-bits address)	1	2
MOVX	@Ri,A	external memory[Ri] = A (8-bits address)	1	2
MOVX	@DPTR,A	external memory[DPTR] = A (16-bits address)	1	2
PUSH	direct	INC SP: MOV “@’SP’, < direct >	2	2
POP	direct	MOV < direct >, “@SP”: DEC SP	2	2
XCH	A,Rn	ACC and < Rn > exchange data	1	1
XCH	A,direct	ACC and < direct > exchange data	2	1
XCH	A,@Ri	ACC and < Ri > exchange data	1	1
XCHD	A,@Ri	ACC and @Ri exchange low nibbles	1	1
Boolean Instructions				
CLR	C	C = 0	1	1
CLR	bit	bit = 0	2	1
SETB	C	C = 1	1	1
SETB	bit	bit = 1	2	1
CPL	C	C = /C	1	1
CPL	bit	bit = /bit	2	1
ANL	C,bit	C = C .AND. bit	2	2
ANL	C,/bit	C = C .AND. /bit	2	2
ORL	C,bit	C = C .OR. bit	2	2
ORL	C,/bit	C = C .OR. /bit	2	2
MOV	C,bit	C = bit	2	1
MOV	bit,C	bit = C	2	2
JC	rel	Jump if C= 1	2	2
JNC	rel	Jump if C= 0	2	2
JB	bit,rel	Jump if bit = 1	3	2
JNB	bit,rel	Jump if bit = 0	3	2
JBC	bit,rel	Jump if C = 1	3	2
Jump Instructions				
ACALL	addr11	Call Subroutine only at 2k bytes Address	2	2
LCALL	addr16	Call Subroutine in max 64K bytes Address	3	2

RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr11	Jump only at 2k bytes Address	2	2
LJMP	addr16	Jump to max 64K bytes Address	3	2
SJMP	rel	Jump on at 256 bytes	2	2
JMP	@A+DPTR	Jump to A+ DPTR	1	2
JZ	rel	Jump if A = 0	2	2
JNZ	rel	Jump if A ≠ 0	2	2
CJNE	A, direct,rel	Jump if A ≠ < direct >	3	2
CJNZ	A, #data,rel	Jump if A ≠ < #data >	3	2
CJNZ	Rn, #data,rel	Jump if Rn ≠ < #data >	3	2
CJNZ	@Ri, #data,rel	Jump if @Ri ≠ < #data >	3	2
DJNZ	Rn,rel	Decrement and jump if Rn not zero	2	2
DJNZ	direct,rel	Decrement and jump if direct not zero	3	2
NOP		No Operation	1	1

Extension Function Description

Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bits free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover form abnormal software condition. The WDT is different from Timer0, Timer1 of general 8051. To prevent a WDT reset can be done by software periodically clearing the WDT counter.

The SM8951B WDT has selectable divider input for the time base source clock. To select the divider input, the setting of bit2~bit0 (PS2~PS0) OF Watch Dog Timer Control Register (WDTC) should be set accordingly.

To enable the WDT is done by setting 1 to the bit 7 (WDTE) of WDTC. After WDTE set to 1, the 16-bits counter starts to count with the selected time base source clock which set by PS2~PS0. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when SM8951B been reset, either hardware reset or WDT reset.

To reset the WDT is done by setting 1 to the bit 5 (CLEAR) of WDTC. This will clear the content of the 16-bits counter and let the counter re-start to count from the beginning.

Watch Dog Timer Registers- WDT Control Register

WDTC ($9F)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTE	Unused	CLEAR	Unused	Unused	PS2	PS1	PS0

WDTE : Watch Dog Timer enable bit

CLEAR : Watch Dog Timer clear bit

If set the CLEAR bit, Watch Dog Timer will be re-start. then this bit will be clear automaticlly .

PS2~PS0: Clock sourer divider bit

PS [2:0]	Divider (OSC in)	Time Period (ms) @40MHZ
000	8	13.1
001	16	26.21
010	32	52.42
011	64	104.8
100	128	209.71
101	256	419.43
110	512	838.86
111	1024	1677.72

Watch Dog Timer Register - System Control Register

SCONF ($BFH)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDR	Unused	Unused	Unused	Unused	Unused	Unused	ALEI

WDR : Watch Dog Timer Reset Flag. When system reset by Watch Dog Timer overflow, WDR will be set to 1.
ALEI : ALE output inhibit bit. It can reduce EMI.
The bit 7(WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened.

Reduce EMI Function

The SM8951B allows user to reduce the EMI emission by setting 1 to the bit 0 (ALEI) of SCONF register. This function will inhibit the clock signal in Fosc/6 Hz output to the ALE pin. This function is available when there is no external program memory or no external data RAM in the system.

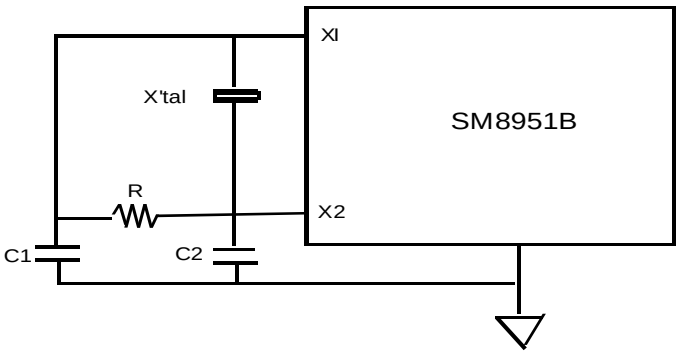
Application Reference

Valid for SM8951B				
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 pF	30 pF	30 pF	22 pF
C2	30 pF	30 pF	30 pF	22 pF
R	open	open	open	open
X'tal	16MHz	25MHz	33MHz	40MHz
C1	22 pF	15 pF	5 pF	2 pF
C2	22 pF	15 pF	5 pF	2 pF
R	open	62KΩ	6.8KΩ	4.7KΩ

Note:

Oscillation circuit may differs with different crystal or ceramic resonator in higher oscillation frequency which was due to each crystal or ceramic resonator has its own characteristics.

User should check with the crystal or ceramic resonator manufacturer for appropriate value of external components.



Power Saving Mode

The SM8951B has several features that help the user to control the power consumption of the device. The powers saving features are basically the Power Down mode, Economy mode and the Idle mode of operation.

Idle Mode:

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle Mode, the clock to the CPU is halted, but not to the Interrupt, Timer and Serial port blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The ALE and PSEN pins are held high during the idle state. The port pins hold the logical states they had at the time idle

was activated. The idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the idle bit, terminate the idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction that put the device into idle mode.

The Idle mode can also be exited by activating the reset. The device can be put into reset either applying a high on the external RST pin or a Power on reset condition. The external reset pin has to be held high for at least two machine cycles to be recognized as a valid reset. In the reset condition the program counter is reset to 0000H and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution start immediately.

When the SM8951B is exiting from an idle mode with a reset, the instruction following the one that put the device into idle mode is not executed. So there is no danger of unexpected writes.

Power Down Mode:

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. In this state the ALE and PSEN pins are pull low. The port pins output the values held by their respective SFRs.

The status of external pins during Idle and Power Down:

Mode	Program Memory	ALE	/PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

MCU writer list		
Company	Contact info	Programmer Model Number
Advantech 7F, No.98, Ming-Chung Rd., Shin-Tien City, Taipei, Taiwan, ROC Web site: http://www.aec.com.tw	Tel:02-22182325 Fax:02-22182435 E-mail: aecwebmaster@advantech.com.tw	Lab Tool - 48XP/UXP Lab Tool – 848/848XP
Hi-Lo 4F.,No.18,Lane 79,Rueiguang Rd.,Neihu,Taipei,Taiwan R.O.C. Web site: http://www.hilosystems.com.tw	Tel: 02-87923301 Fax:02-87923285 E-mail: support@hilosystems.com.tw	All - 100 series
Leap 6th F1-4, Lane 609, Chunghsin Rd., Sec. 5, Sanchung, Taipei , Taiwan, ROC Web site: http://www.leap.com.tw	Tel: 886-2-29991860 Fax:02-29990015 E-mail: service@leap.com.tw	Leap-48
Xeltek Electronic Co., Ltd Bldg 6-31 Meizhiguo garden, #2 Jiangjun Ave., Jiangning, Nanjing, China 211100 Web site: http://www.xeltek-cn.com	Tel: + 86-25-52765201, E-mail: f_l@xeltek.com.cn zxl@xeltek.com.cn	Superpro 280U Superpro 580U Superpro 3000U Superpro 9000U
Guangzhou Zhiyuan Electronic Co.,Ltd Floor 2,No.7 building,Huangzhou Industrial Estate,Chebei Road,Tianhe district,Guangzhou,China 510660 Web site: http://www.embedtools.com/	TEL: +86-20-28872449 E-mail: mcu@programtec.com	SmartPRO 5000U/X8
TianJin Weilei technology ltd Rm 357,Venturetech Center,12 Keyan West Road Nankai District,Tianjin,P.R.C, 300192 Web site: http://www.weilei.com.cn/	TEL: + 86-22-87891218#801 E-mail: weilong@weilei.com.cn cm@weilei.com.cn	VP-890;VP-980;VP-880;VP-680 VP-480;VP-380;VP-280;VP-190
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