UVEPROM SMJ27C040

Austin Semiconductor, Inc.

4 MEG UVEPROM

UV Erasable Programmable Read-Only Memory

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-91752
- MIL-STD-883

FEATURES

- Organized 524,288 x 8
- Single $+5V \pm 10\%$ power supply
- Industry standard 32-pin dual-in-line package
- All inputs/outputs fully TTL compatible
- Static Operation (no clocks, no refresh)
- 8-bit output for use in microprocessor-based systems
- · Power-saving CMOS technology
- 3-state output buffers
- 400-mV DC assured noise immunity with standarad TTL loads
- Latchup immunity of 250 mA on all input and output pins
- No pullup resistors required
- Low power dissipation (Vcc = 5.5V)
 - ✓Active 385 mW Worst Case
 - ✓ Standby 0.55 mW Worst Case (CMOS-input levels)

OPTIONS MARKING • Timing

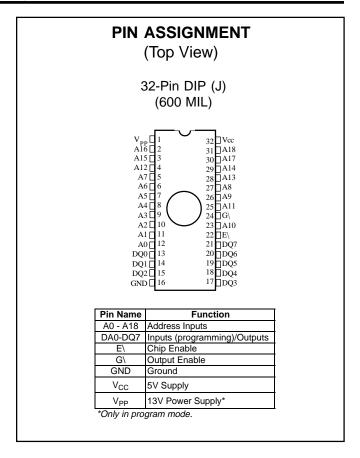
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120ns access	-12
150ns access	-15

• Package(s)

Ceramic DIP (600mils) No. 114

• Operating Temperature Ranges Military (-55°C to +125°C)

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GENERAL DESCRIPTION

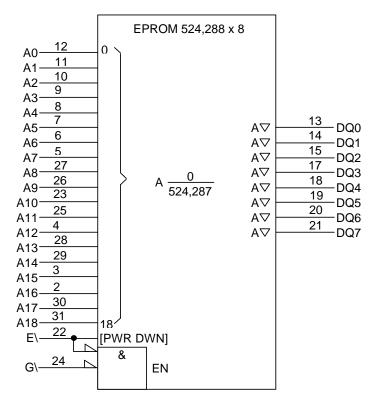
The SMJ27C040 is a set of 4,194,304-bit, ultraviolet-light erasable, electrically programmable read-only memories (EPROMs).

These devices are fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits. Each output can drive one Series 54 TTL circuit without external resistors. The data outputs are 3-state for connecting multiple devices to a common bus.

The SMJ27C040 is offered in a 32-pin 600-mil dual-in-line ceramic package (J suffix) rated for operation from -55°C to 125°C.

Since this EPROM operates from a single 5V supply (in the read mode), it is ideal for use in microprocessor-based systems. One other (13V) supply is needed for programming. All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

FUNCTIONAL BLOCK DIAGRAM*



^{*} This symbol is in accordance with ANSI/IEEE std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the J package.

OPERATION

The seven modes of operation are listed in Table 1. The read mode requires a single 5V supply. All inputs are TTL level except for V_{pp} during programming (13V), and V_{H} (12V) \S on A9 for signature mode.

TABLE 1. OPERATION MODES

		FUNCTION						
	E\	G\	V_{PP}	V _{CC}	A9	A0	DQ0-DQ7	
Read	V_{IL}	V_{IL}	V _{CC}	V _{CC}	Х	Х	Data Out	
Output Disable	V_{IL}	V_{IH}	V _{CC}	V _{CC}	Х	Х	High-Z	
Standby	V_{IH}	Χ	V _{CC}	V _{CC}	Х	Χ	High-Z	
Programming	V_{IL}	V_{IH}	V_{PP}	V _{CC}	Х	Х	Data In	
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V _{CC}	Х	Х	High-Z	
Verify	V_{IH}	V_{IL}	V_{PP}	V _{CC}	Х	X	Data Out	
Signature Mode	V_{IL}	V _{IL}	Vac	Vac	C V _{IH} *	V_{IL}	MFG Code 97	
Signature Mode	V IL	V IL	V _{CC}	V _{CC}		V_{IL}	Device Code 50	

^{*} \overline{X} can be \overline{V}_{IL} or \overline{V}_{IH} . $\S V_H = 12V \pm 0.5V$

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READ/OUTPUT DISABLE

When the outputs of two or more SMJ27C040s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low level signal is applied to the E\ and G\ pins. All other devices in the circuit should have their outputs disabled by applying a high level signal to one of these pins. Output data is accessed at pins Q0-Q7.

LATCHUP IMMUNITY

Latchup immunity on the SMJ27C040 is a minimum of 250mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

POWER DOWN

Active I_{CC} supply current can be reduced from 70mA to 1mA for a high TTL input on $E\setminus$ and to 100 μ A for a high CMOS input on $E\setminus$. In this mode all outputs are in the high-impedance state.

ERASURE

Before programming, the SMJ27C040 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet-light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity x exposure time) is 15-W·s/cm². A typical 12-mW/cm², filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the SMJ27C040, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

SNAP! PULSE PROGRAMMING

The SMJ27C040 is programmed by using the SNAP! Pulse programming algorithm. The programming sequence is shown in the SNAP! Pulse programming flow chart (Figure 1).

The initial setup is $V_{PP} = 13V$, $V_{CC} = 6.5V$, $E \setminus V_{IH}$, and $G \setminus V_{IL}$. Once the initial location is selected, the data is presented in parallel (eight bits) on pins DQ1 through DQ8. Once addresses and data are stable, the programming mode is achieved when $E \setminus V_{IL}$ with a pulse duration of $V_{W(PGM)}$. Every location is programmed only once before going to interactive mode.

In the interactive mode, the word is verified at $V_{PP} = 13V$, $V_{CC} = 6.5V$, $E \setminus = V_{IH}$, and $G \setminus = V_{IL}$. If the correct data is not read, the programming is performed by pulling $G \setminus high$, then $E \setminus low$ with a pulse duration of $t_{W(PGM)}$. This sequence of verification and programming is performed up to a maximum of 10 times. When the device is fully programmed, all bytes are verified with $V_{CC} = V_{PP} = 5V \pm 10\%$.

PROGRAM INHIBIT

Programming can be inhibited by maintaining high level inputs on the $E\setminus$ and $G\setminus$ pins.

PROGRAM VERIFY

Programmed bits can be verified with $V_{PP}=13V$ when $G \setminus = V_{II}$, and $E \setminus = V_{IH}$.

SIGNATURE MODE

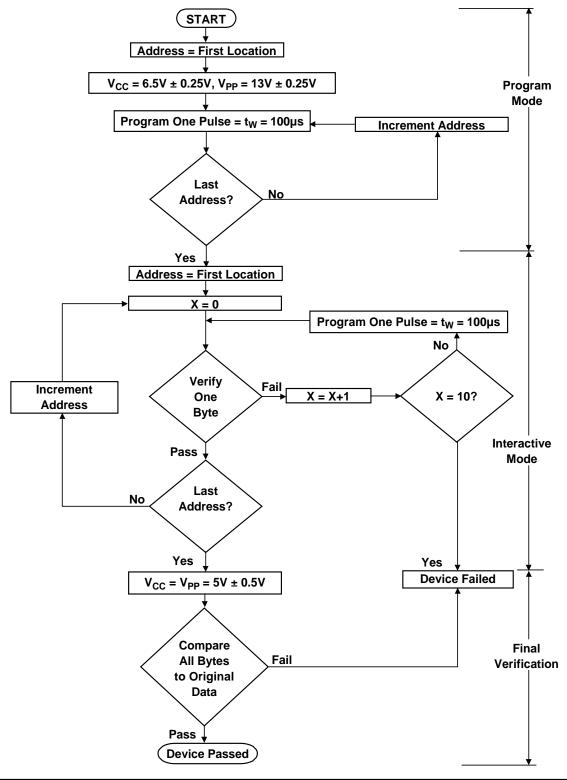
The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12V. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. The signature code for the SMJ27C040 is 9750. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code 50 (Hex), as shown in Table 2.

TABLE 2. SIGNATURE MODES

IDENTIFIER*					PII	NS				
IDENTIFIER	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	0	1	0	1	0	0	0	0	50

* $E = G = V_{IL}$, A1 - A8 = V_{IL} , A9 = V_{H} , A10 - A18 = V_{IL} , $V_{PP} = V_{CC}$.

FIGURE 1. SNAP! PULSE PROGRAMMING FLOW CHART





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ABSOLUTE MAXIMUM RATINGS*

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

** All voltage values are with respect to GND.

RECOMMENDED OPERATING CONDITIONS

				MIN	TYP	MAX	UNIT
V _{CC}	Supply Voltage	Read Mode ¹		4.5	5	5.5	V
• 66	Cuppiy Voltago	SNAP! Pulse programmi	ing algorithm	6.25	6.5	6.75	V
V_{PP}	Supply Voltage	Read Mode ²		V _{CC} -0.6		V _{CC} +0.6	V
* PP	Cuppiy Voltago	SNAP! Pulse programmi	SNAP! Pulse programming algorithm		13	13.25	V
V	I _{IH} High-level input voltage		TTL	2		V _{CC} +0.5	V
V_{IH}	I light-level input v	C		V _{CC} -0.2		V _{CC} +0.5	V
V	Low-level input v	oltago	TTL	-0.5		0.8	V
V IL	V _{IL} Low-level input voltage CMOS		CMOS	-0.5		0.2	V
T_A	Operating free-ai	Operating free-air temperature		-55			Ô
T _C	Operating case to	emperature				+125	°C

NOTES

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = -400 \mu A$	2.4		V
V _{OL}	Low-level output voltage		$I_{OL} = 2.1 \text{mA}$		0.4	V
I _I	Input current (leakage)		$V_I = 0V$ to 5.5V		±1	μA
Io	Output current (leakage)		$V_O = 0V$ to V_{CC}		±1	μA
I _{PP1}	V _{PP} supply current		$V_{PP} = V_{CC} = 5.5V$		10	μA
I _{PP2}	V _{PP} supply current (during prog	ram pulse) ¹	V _{PP} = 12.75V, T _A -25°C		50	mA
1	V _{CC} supply current (standby)	TTL-Input Level	V _{CC} = 5.5V, E\=V _{IH}		1	mA
I _{CC1}	VCC supply current (standby)	CMOS-Input Level	$V_{CC} = 5.5V, E = V_{CC}$		100	μA
			E\=V _{IL} , V _{CC} =5.5V			
I _{CC2}	V _{CC} supply current (active)		t _{cycle} = minimum cycle time,		50	mA
			outputs open ²			

NOTES:

^{1.} $V_{\rm CC}$ must be applied before or at the same time as $V_{\rm pp}$ and removed after or at the same time as $V_{\rm pp}$. The deivce must not be inserted into or removed from the board when $V_{\rm pp}$ or $V_{\rm CC}$ is applied.

^{2.} V_{pp} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{pp}$. During programming, V_{pp} must be maintained at 13V + 0.25V

^{1.} This parameter is only sampled and not 100% tested.

^{2.} Minimum cycle time = maximum access time.



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CAPACITANCE OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, f = 1MHz ($V_{\rm CC} = V_{\rm PP} = 5V \pm 0.5V$)*

F	ARAMETER	TEST CONDITIONS	TYP**	MAX	UNIT
C _i	Input capacitance	$V_I = 0V$	4	8	pF
Co	Output capacitance	$V_O = 0V$	8	12	pF

^{*} Capacitance is sampled only at initial design and after any major change.

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE^{1,2}

	PARAMETER	TEST	-12		-15		UNIT
	PARAMETER	CONDITIONS ^{2, 3}	MIN	MAX	MIN	MAX	UNIT
t _{a(A)}	Access time from address			120		150	ns
t _{a(E)}	Access time from chip enable			120		150	ns
t _{en(G)}	Output enable time from G\	(see Figure 2)		50		50	ns
t _{dis}	Output disable time from G\ or E whichever occurs first ¹	Input $t_r < 20$ ns Input $t_f < 20$ ns	0	50	0	50	ns
t _{v(A)}	Output data valid time after change of address, E or G whichever occurs first 1		0		0		ns

NOTES:

SWITCHING CHARACTERISTICS FOR PROGRAMMING: $V_{CC} = 6.5V$ and $V_{PP} = 13V$ (SNAP! Pulse), $T_A = 25^{\circ}C$

	PARAMETER	MIN	MAX	UNIT
t _{dis(G)}	Output disable time from G\	0	100	ns
t _{en(G)}	Output enable time from G\		150	ns

TIMING REQUIREMENTS FOR PROGRAMMING

			MIN	TYP	MAX	UNIT
t _{h(A)}	Hold Time, Address		0			μs
t _{h(D)}	Hold Time, Data		2			μs
t _{w(PGM)}	Pulse Duration, Program	SNAP! Pulse Programming Algorithm	95	100	105	μs
t _{su(A)}	Setup Time, Address		2			μs
t _{su(E)}	Setup Time, E\		2			μs
t _{su(G)}	Setup Time, G\		2			μs
t _{su(D)}	Setup Time, Data		2			μs
t _{su(Vpp)}	Setup Time, V _{PP}		2			μs
t _{su(Vcc)}	Setup Time, V _{CC}		2			μs

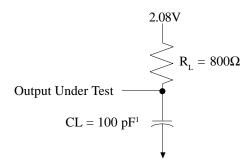
^{**} All typical values are at $T_{\Lambda} = 25^{\circ}$ C and nominal voltages.

 $^{1.\} Value\ calculated\ from\ 0.5V\ delta\ to\ measured\ output\ level.\ This\ parameter\ is\ only\ sampled\ and\ not\ 100\%\ tested.$

^{2.} Common test conditions apply for $\rm t_{\rm dis}$ except during programming.

^{3.} For all switching characteristics the input pulse levels are 0.4V to 2.4V. Timing measurements are made at 2V for logic high and 0.8V for logic low. (Figure 2)

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. C_L includes probe and fixture capacitance.

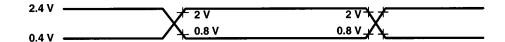


FIGURE 2. OUTPUT LOAD CIRCUIT AND INPUT/OUTPUT WAVE FORMS

FIGURE 3. READ-CYCLE TIMING

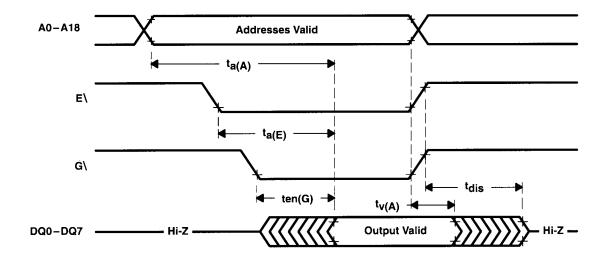
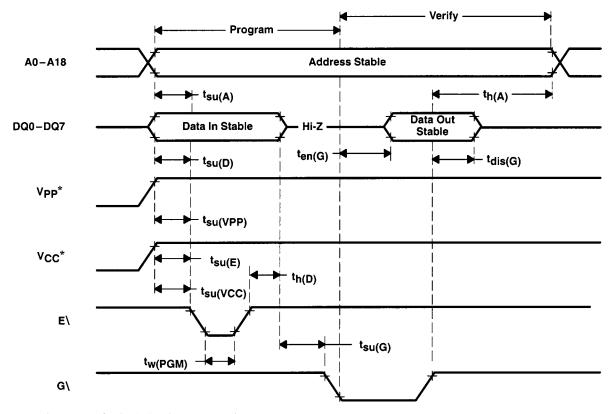


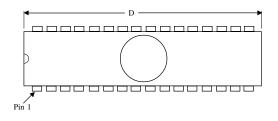
FIGURE 4. PROGRAM-CYCLE TIMING (SNAP! PULSE PROGRAMMING)

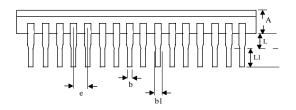


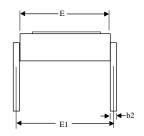
^{* 13}V V_{PP} and 6.5V V_{CC} for SNAP! Pulse programming.

MECHANICAL DEFINITION*

ASI Case #114 (Package Designator J) SMD 5962-91752, Case Outline X







	SMD Specifications				
SYMBOL	MIN	MAX			
Α		0.225			
b	0.014	0.026			
b1	0.045	0.065			
b2	0.008	0.018			
D		1.680			
E	0.510	0.620			
е	0.100) BSC			
E1	0.600) BSC			
L1	0.125	0.200			
L	0.015	0.070			

NOTE: These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.

ORDERING INFORMATION

EXAMPLE: SMJ27C040-15JM

Device Number	Speed ns	Package Type	Operating Temp.
SMJ27C040	-12	J	*
SMJ27C040	-15	J	*

*AVAILABLE PROCESSES

M = Extended Temperature Range

 -55° C to $+125^{\circ}$ C

ASI Austin Semiconductor, Inc.

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ASI TO DSCC PART NUMBER CROSS REFERENCE*

ASI Package Designator J

TI Part #** SMJ27C040-12JM SMJ27C040-15JM **SMD Part #** 5962-9175205MXA 5962-9175204MXA

^{*} ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.

^{**} Parts are listed on SMD under the old Texas Instruments part number. ASI purchased this product line in November of 1999.