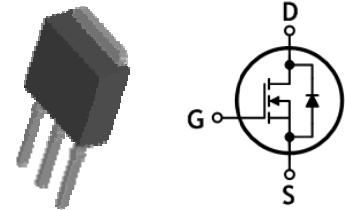


SWITCHING REGULATOR APPLICATION

Features

- Drain-source breakdown voltage: $BV_{DSS}=650V$
- Low gate charge: $Q_g=11.2nC$ (Typ.)
- Low drain-source On-resistance: $R_{DS(on)}=3\Omega$ (Max.)
- RoHS compliant device
- Halogen free package



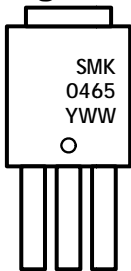
G D S

I-PAK (Short Lead)

Ordering Information

Part Number	Marking	Package
SMK0465IS	SMK0465	I-PAK (Short lead)

Marking Information



Column 1, 2: Device Code
 Column 3: Production Information
 e.g.) YWW
 - . YWW: Date Code (year, week)

Absolute maximum ratings ($T_C=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	V_{DSS}	650	V	
Gate-source voltage	V_{GSS}	± 30	V	
Drain current (DC) *	I_D	$T_C=25^\circ C$	4	A
		$T_C=100^\circ C$	2.5	A
Drain current (Pulsed) *	I_{DM}	16	A	
Single avalanche current ^(Note 2)	I_{AR}	4	A	
Single pulsed avalanche energy ^(Note 2)	E_{AS}	81.5	mJ	
Repetitive avalanche current ^(Note 1)	I_{AR}	4	A	
Repetitive avalanche energy ^(Note 1)	E_{AR}	3.4	mJ	
Power dissipation	P_D	48	W	
Junction temperature	T_J	150	$^\circ C$	
Storage temperature range	T_{stg}	-55~150	$^\circ C$	

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 2.6	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}, V_{GS}=0$	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}, V_{DS}=V_{GS}$	2	-	4	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=650\text{V}, V_{GS}=0\text{V}$	-	-	1	μA
		$V_{DS}=650\text{V}, T_C=125^\circ\text{C}$	-	-	100	μA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}, V_{GS}=\pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=2\text{A}$	-	2.4	3	Ω
Forward transfer conductance (Note 3)	g_{fs}	$V_{DS}=10\text{V}, I_D=2\text{A}$	-	4	-	S
Input capacitance	C_{iss}	$V_{DS}=25\text{V}, V_{GS}=0\text{V}, f=1.0\text{MHz}$	-	703	878	pF
Output capacitance	C_{oss}		-	54.6	68.2	
Reverse transfer capacitance	C_{rss}		-	5.6	7.0	
Turn-on delay time (Note 3,4)	$t_{d(on)}$		-	10	-	
Rise time (Note 3,4)	t_r	$V_{DD}=300\text{V}, I_D=4\text{A}, R_G=25\Omega$	-	42	-	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	38	-	
Fall time (Note 3,4)	t_f		-	46	-	
Total gate charge (Note 4,5)	Q_g		$V_{DS}=520\text{V}, V_{GS}=10\text{V}, I_D=4\text{A}$	-	11.2	14
Gate-source charge (Note 3,4)	Q_{gs}	-		3.9	-	
Gate-drain charge (Note 3,4)	Q_{gd}	-		2.5	-	

Source-Drain Diode Ratings and Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	4	A
Source current (Pulsed)	I_{SM}		-	-	16	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}, I_S=4\text{A}$	-	-	1.4	V
Reverse recovery time (Note 3, 4)	t_{rr}	$I_S=4\text{A}, V_{GS}=0\text{V}, di_F/dt=100\text{A}/\mu\text{s}$	-	300	-	ns
Reverse recovery charge (Note 4,5)	Q_{rr}		-	2.2	-	μC

Note:

1. Repeated rating: Pulse width limited by safe operating area
2. $L=9.4\text{mH}, I_{AS}=4\text{A}, V_{DD}=50\text{V}, R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
3. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

Electrical Characteristic Curves

Fig. 1 $I_D - V_{DS}$

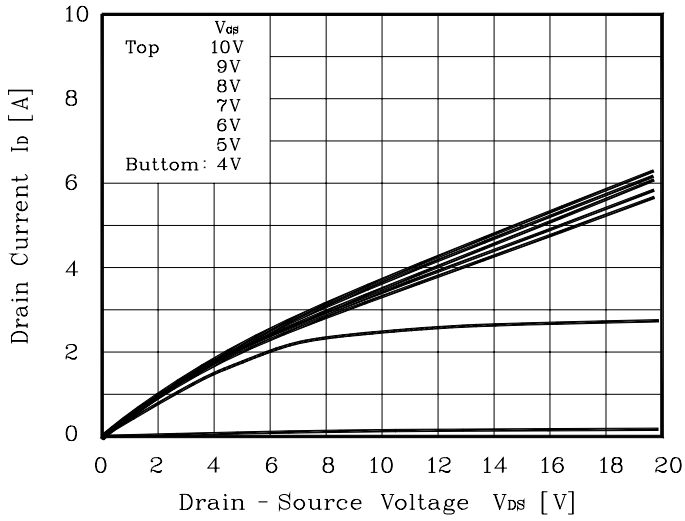


Fig. 2 $I_D - V_{GS}$

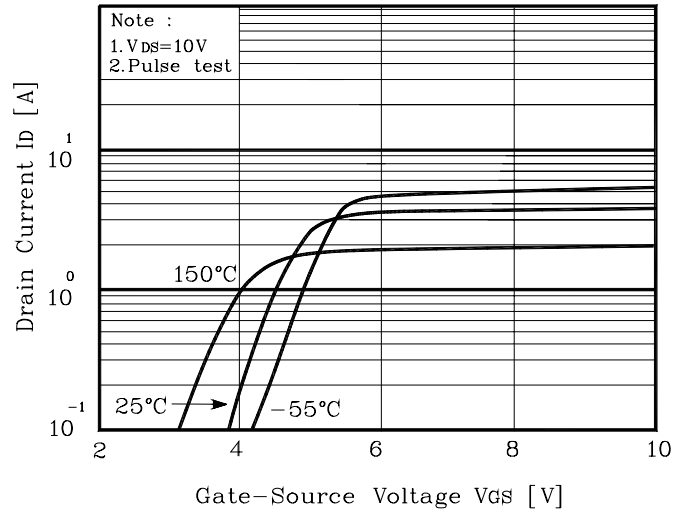


Fig. 3 $R_{DS(on)} - I_D$

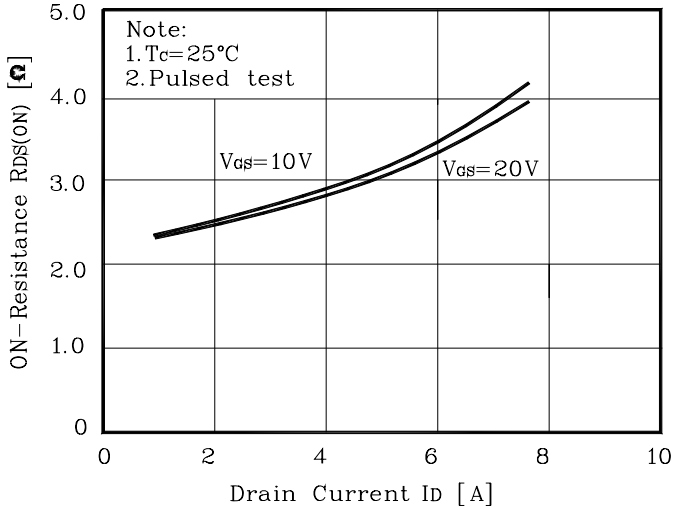


Fig. 4 $I_S - V_{SD}$

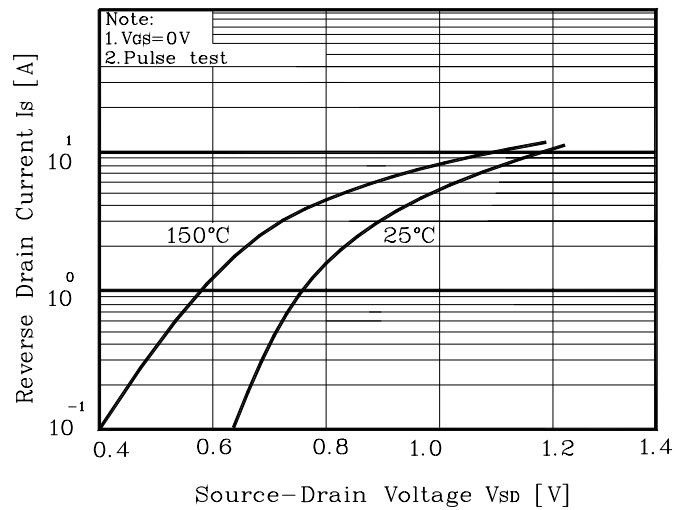


Fig. 5 Capacitance - V_{DS}

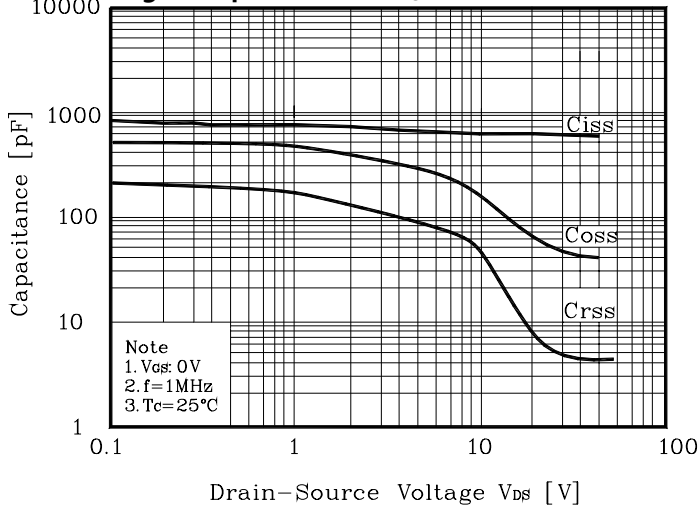
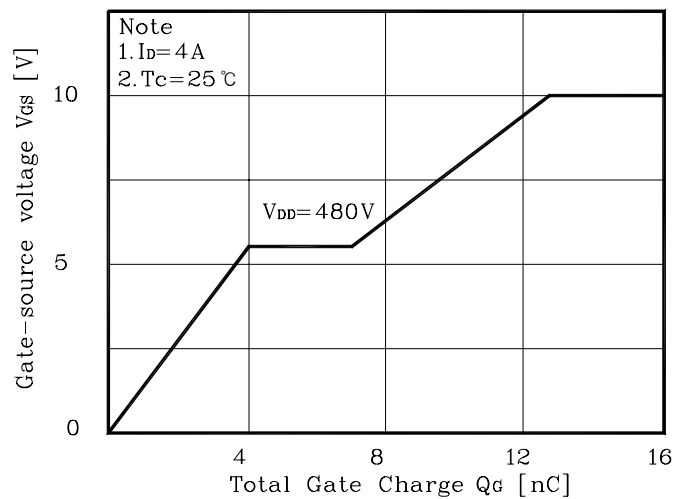


Fig. 6 $V_{GS} - Q_G$



Electrical Characteristic Curves (Continue)

Fig. 7 $V_{DSS} - T_J$

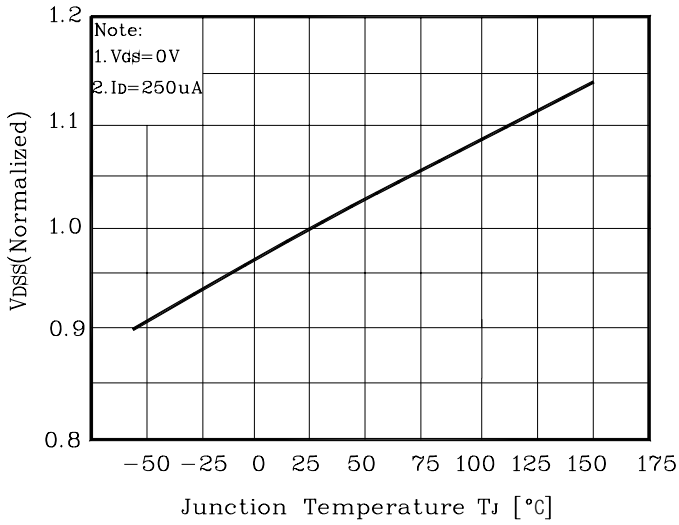


Fig. 8 $R_{DS(on)} - T_J$

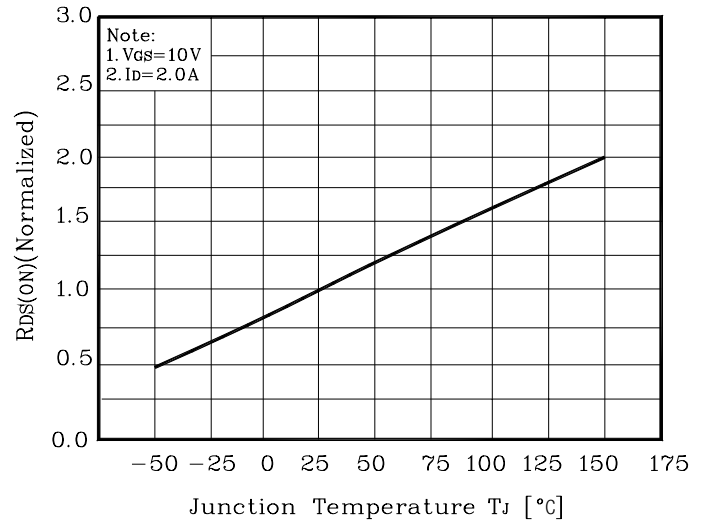


Fig. 9 $I_D - T_C$

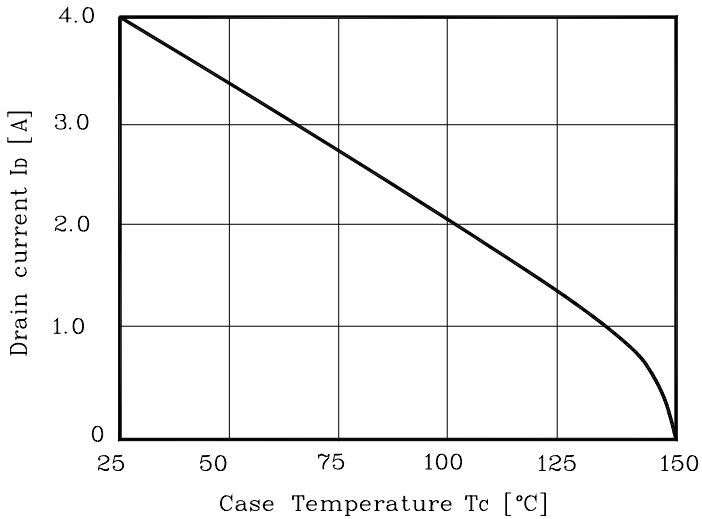


Fig. 10 Safe Operating Area

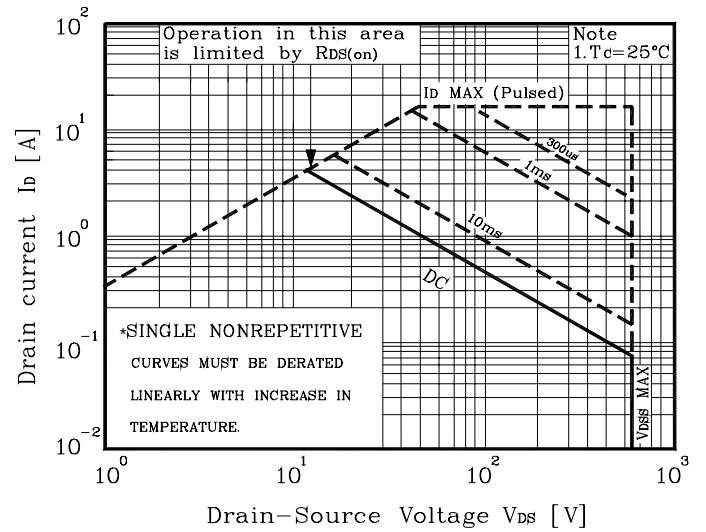


Fig. 11 Gate Charge Test Circuit & Waveform

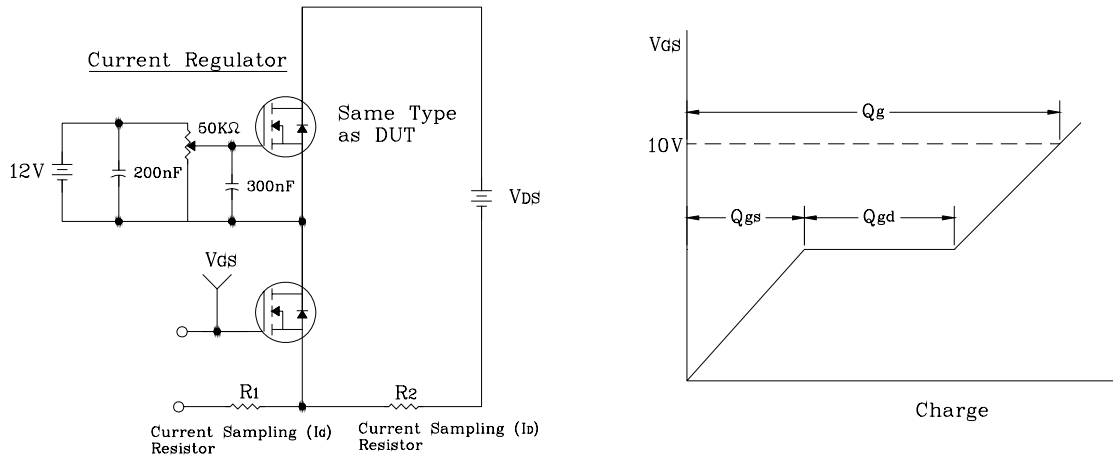


Fig. 12 Resistive Switching Test Circuit & Waveform

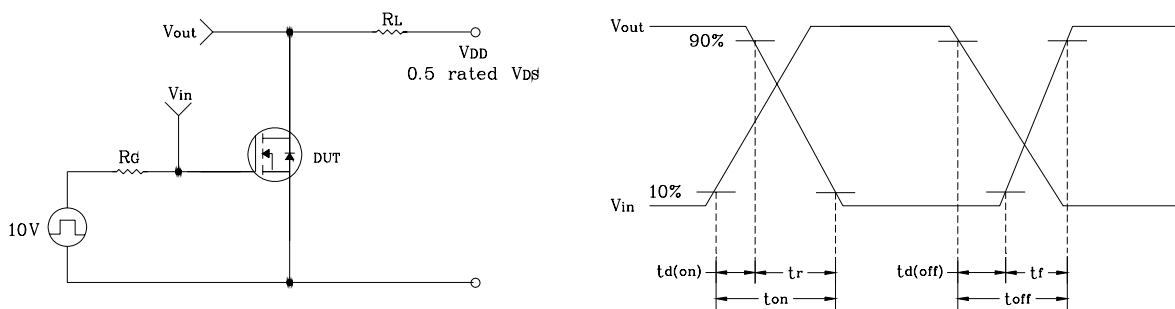


Fig. 13 E_{AS} Test Circuit & Waveform

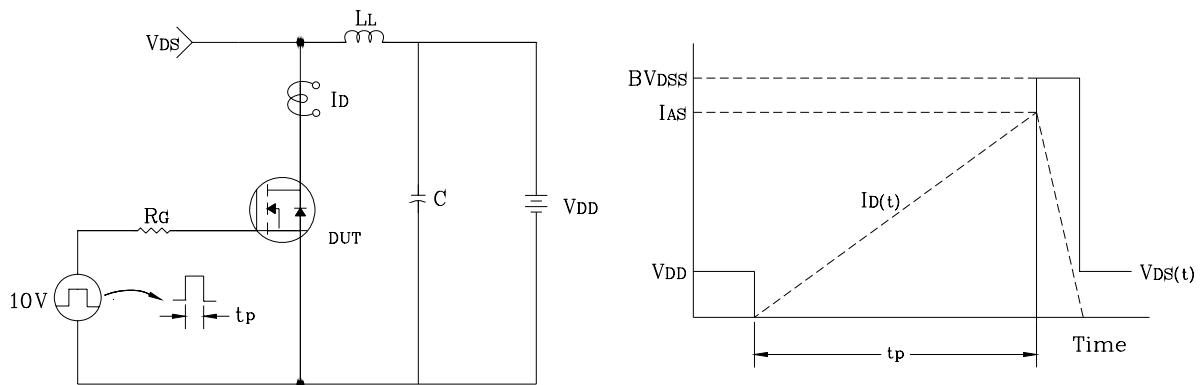
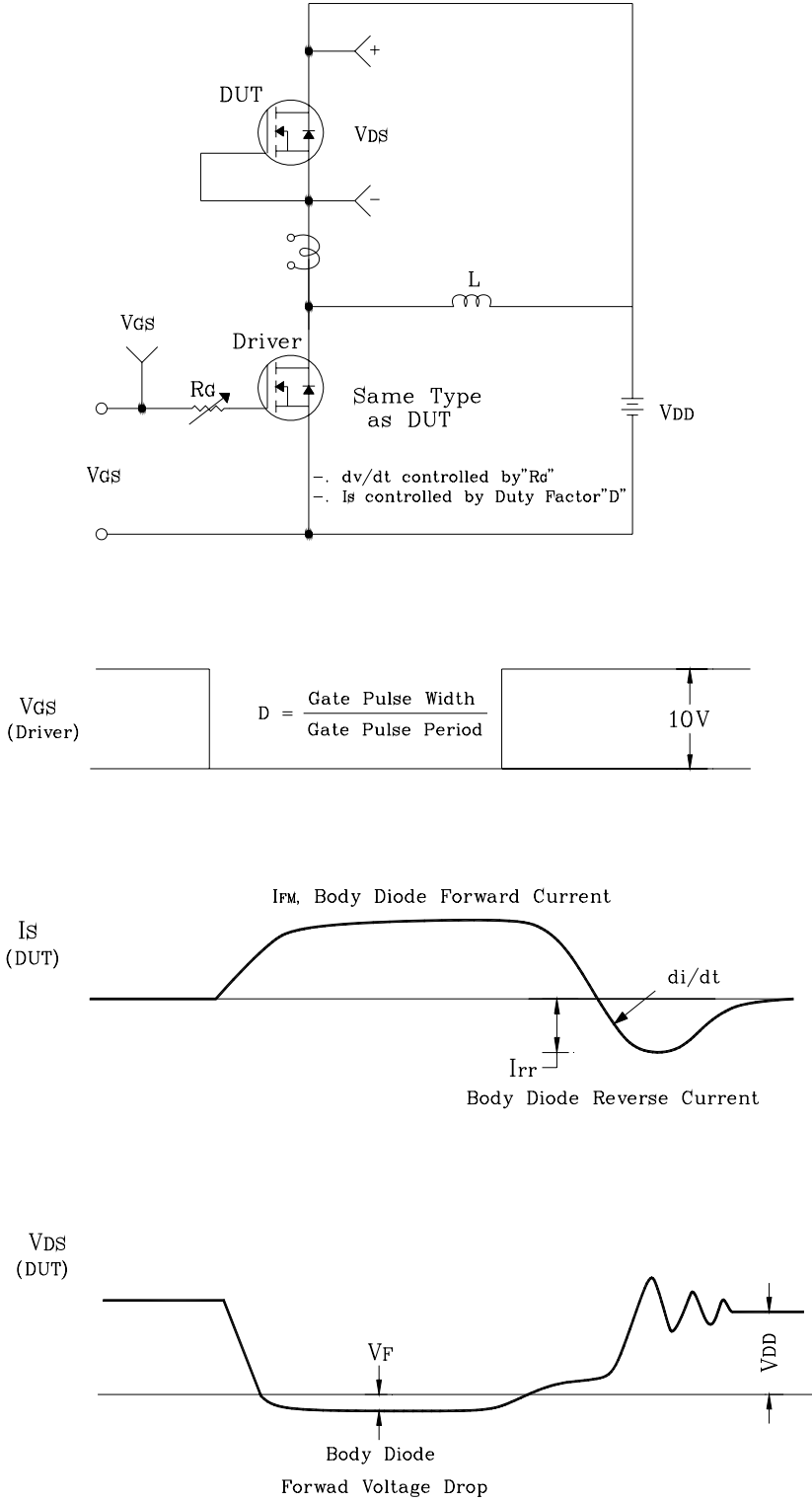
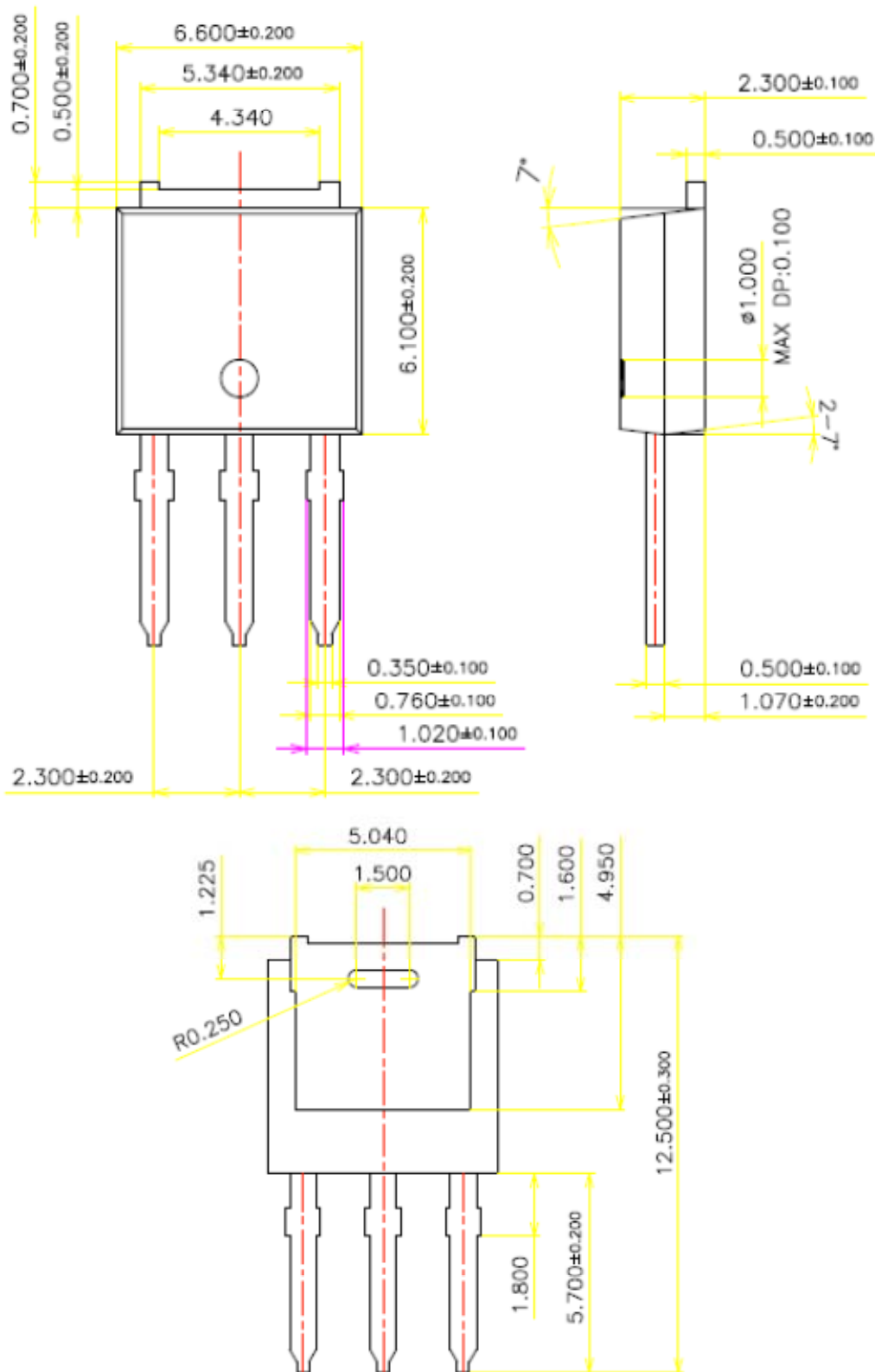


Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform



Package Outline Dimensions



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