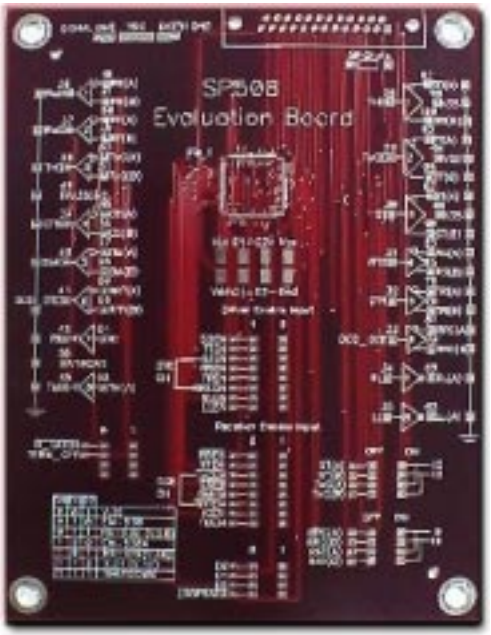
SP508
Evaluation Board Manual

FEATURES

- Easy Evaluation of SP508 Multi-Protocol Transceiver
- Eight (8) Drivers and Eight (8) Receivers
- Current Mode V.35 Drivers
- Internal Line or Digital Loopback
- Internal Transceiver Termination Resistors for V.11 and V.35
- Termination Network Disable Option
- Fast 20Mbps Differential Transmission Rates
- Adheres to CTR1/CTR2 Compliancy Requirements
- PCB Friendly Flow-Through Pinout
- Improved ESD Tolerance for Analog I/Os
- Interface modes:

RS-232 (V.28)	EIA-530 (V.10&V.11)
X.21 (V.11)	EIA-530A (V.10&V.11)
RS-449/V.36 (V.10&V.11)	V.35



DESCRIPTION

The SP508 Evaluation Board is designed to analyze the SP508 multi-protocol transceivers. The evaluation board provides access points to all of the driver and receiver I/O pins so that the user can measure electrical characteristics and waveforms of each signal. The SP508 Evaluation Board also includes a DB-25 serial port connector which is configured to a EIA-530 pinout. This allows easy connections to other DTE or DCE systems as well as network analyzers. The evaluation board also has dip switches to allow the user to select the mode of operation and test the data latch feature. The SP508 Evaluation Board Provides the means to test both local and remote driver/receiver Loopback as well as evaluate the SP508 in a DCE or DTE configuration.

This Manual is split into sections to give the user the information necessary to perform a thorough evaluation of the SP508. The Board Layout section describes the I/O pins, the Dip switches and the other components used on the evaluation board. The board schematic, layout diagram, list of materials and DB-25 connector are also covered in the Board Layout section. The Using the SP508 Evaluation Board details the configuration of the SP508 evaluation board for parametric testing.

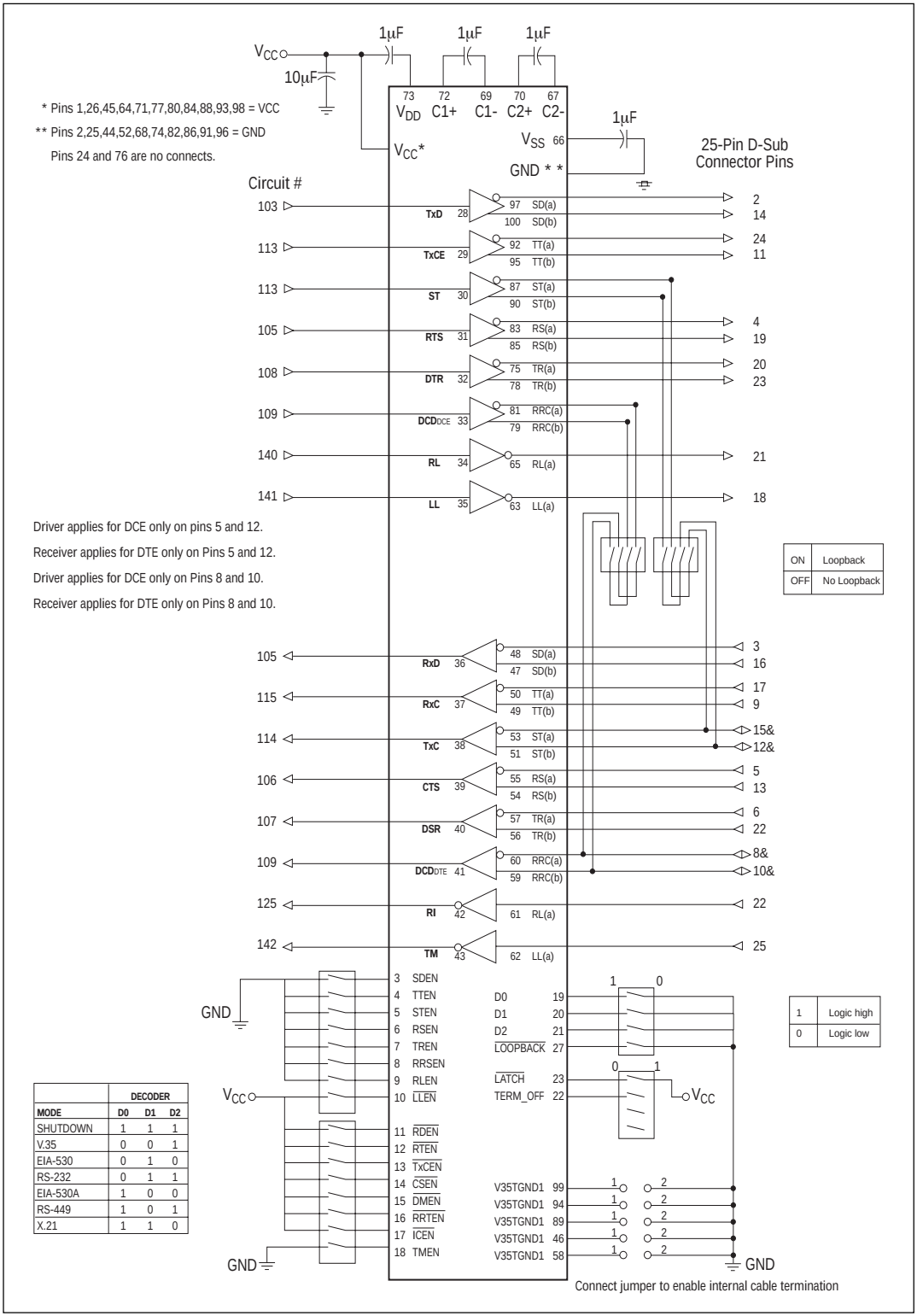


Figure 1

BOARD LAYOUT

1. The SP508 Evaluation board takes advantage of the products PCB friendly flow through pinout in its design as shown in Figure 1.

2. The SP508 Evaluation Board has been designed to easily and conveniently provide access to all inputs and outputs under test.

3. Figure 1 is a block diagram of the evaluation board showing the layout of the SP508 Evaluation Board. The block diagram shows the location of the driver and receiver access points as well as the DIP switches, V_{CC}, GND and the DB-25 Connector.

4. I/O Pinouts

The SP508 Evaluation Board has been designed to easily and conveniently provide access to all inputs and outputs to the device under test. Position the Board with the DB-25 connector at the top and the Dip switches at the bottom. From this orientation , all driver inputs and outputs are on the right-hand side and all receiver inputs and outputs are on the left-hand side eof the Board.

4.1. Each Driver has probe points for the input and outputs. There is a ground buss to the right of the drive outputs for the addition of loads to the driver outputs and to jumper the V.35 that is associated with the SD, TT, and ST driver. Each V.35 driver has a separate ground for the V.35 termination network internal to the device.

4.2. Each Receiver has probe points for the inputs and outputs. there is a ground buss to the left of the receiver outputs and a separate pin for the V.10 termination ground.

5. At the bottom of the board is a series of six(6) DIP switches. The DIP switch on the far left is for D_LATCH and TERM_OFF. Each driver and receiver has its own individual enable pin. The DIP switches to control the enable pins are located as the top center bank of switches for the driver and the middle center bank of switches for the receiver. The bottom center set of DIP switches is for the 3 bit decoder and the loopback control pin. The right hand DIP switches allow the user to tie the ST driver outputs to the TxC receiver inputs and the RRC driver outputs to the RRT receiver inputs.

6. Also located on the SP508 evaluation board are the four 10uf charge pump capacitors, a 10uf bypass capacitor for V_{CC} and a 50Ω termination resistor.

7. Table 1 shows the pinout of the DB-25 connector used to connect to a communication analyzer such as the TTC Firebird 6000.

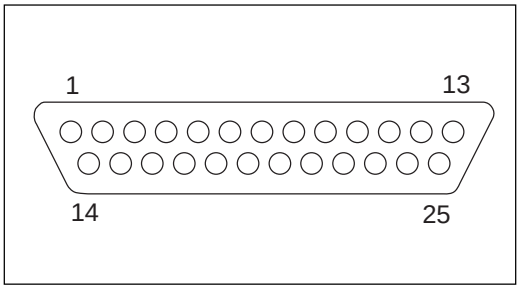


Figure 2: RS-232 & EIA530 Connector (ISO 2110), DTE Connector σ DB-25 Male, DCE Connector σ DB-25 Female

Table 1.

		EIA-232		EIA-530		EIA-449		V.35		X.21	
Signal Name	**source**	**Mnemonic**	**Pin**	**Mnemonic**	**Pin**	**Mnemonic**	**Pin**	**Mnemonic**	**Pin**	**Mnemonic**	**Pin**
Shield	—	—	1	—	1	—	1	—	A	—	1
Transmitted data	DTE	BA	2	BA(A)	2	SD(A)	4	103	P	Circuit T(A)	2
				BA(B)	14	SD(B)	22	103	S	Circuit T(B)	9
Received Data	DCE	BB	3	BB(A)	3	RD(A)	6	104	R	Circuit R(A)	4
				BB(B)	16	RD(B)	24	104	T	Circuit R(B)	11
Request To Send	DTE	CA	4	CA(A)	4	RS(A)	7	105	C	Circuit C(A)	3
				CA(B)	19	RS(B)	25			Circuit C(B)	10
Clear To Send	DCE	CB	5	CB(A)	5	CS(A)	9	106	D	Circuit I(A)	5
				CB(B)	13	CS(B)	27			Circuit I(B)	12
DCE Ready (DSR)	DCE	CC	6	CC(A)	6	DM(A)	11	107	E		
				CC(B)	22	DM(B)	29				
DTE Ready (DTR)	DTE	CD	20	CD(A)	20	TR(A)	12	108	H*		
				CD(B)	23	TR(B)	30				
Signal Ground	—	AB	7	AB	7	SG	19	102	B	Circuit G	8
Recv. Line Sig. Det. (DCD)	DCE	CF	8	CF(A)	8	RR(A)	13	109	F		
				CF(B)	10	RR(B)	31				
Trans. Sig. Elemt. Timing	DCE	DB	15	DB(A)	15	ST(A)	5	114	Y	Circuit S(A)	6
				DB(B)	12	ST(B)	23	114	AA	Circuit S(B)	13
Recv. Sig.	DTE	RL	17	DD(A)	17	RT(A)	8	115	V	Circuit B(A)**	7
Elemt. Timing				DD(B)	9	RT(B)	26	115	X	Circuit B(B)**	14
Local Loopback	DCE	DD	18	LL	18	LL	10	141	L*		
Remote Loopback	DTE	LL	21	RL	21	RL	14	140	N*		
Ring Indicator	DCE	CE	22	—	—	—	—	125	J*		
Trans. Sig. Elemt. Timing	DTE	DA	24	DA(A)	24	TT(A)	17	113	U*	Circuit X(A)**	7
				DA(B)	11	TT(B)	35	113	W*	Circuit X(B)**	14
Test Mode	DCE	TM	25	TM	25	TM	18	142	NN*		

* Optional signals
** Only one of the two x.21 signals, Circuit B or X, can be implemented and active at one time.

Table 2

Driver Output Pin	V.35 Mode	EIA-530 Mode	RS-232 Mode (V.28)	EIA-530A Mode	RS-449 Mode (v.36)	X.21 Mode (v.11)	Shutdown	Suggested Signal
MODE (D0,D1,D2)	001	010	011	100	101	110	111	
T1OUT(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxD(a)
T1OUT(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxD(b)
T2OUT(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxCE(a)
T2OUT(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxCE(b)
T3OUT(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxC_DCE(a)
T3OUT(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxC_DCE(b)
T4OUT(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	RTS(a)
T4OUT(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	RTS(b)
T5OUT(a)	V.28	V.11	V.28	V.10	V.11	V.11	High-Z	DTR(a)
T5OUT(b)	High-Z	V.11	High-Z	V.10	V.11	V.11	High-Z	DTR(b)
T6OUT(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	DCD_DCE(a)
T6OUT(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	DCD_DCE(b)
T7OUT(a)	V.28	V.10	V.28	V.1	V.10	High-Z	High-Z	RL
T8OUT(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	LL

TABLE 3

Receiver Input Pin	V.35 Mode	EIA-530 Mode	RS-232 Mode (V.28)	EIA-530A Mode	RS-449 mode (v.36)	X.21 Mode (v.11)	Shutdown	Suggested Signal
MODE (D0,D1,D2)	001	010	011	100	101	110	111	
R1IN(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	RxD(a)
R1IN(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	RxD(b)
R2IN(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	RxC(a)
R2IN(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	RxC(b)
R3IN(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxC_DTE(a)
R3IN(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxC_DTE(b)
R4IN(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	CTS(a)
R4IN(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	CTS(b)
R5IN(a)	V.28	V.11	V.28	V.10	V.11	V.11	High-Z	DSR(a)
R5IN(b)	High-Z	V.11	High-Z	V.10	V.11	V.11	High-Z	DSR(b)
R6IN(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	DCD_DTE(a)
R6IN(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	DCD_DTE(b)
R7IN(a)	V.28	V.10	V.28	V.1	V.10	High-Z	High-Z	RI
R8IN(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	TM

Recommended Equipment

- Oscilloscope
- Digital multimeter
- Signal Generator capable of >40MHz
- Communications Analyzer (such as Firebird 6000)

Parametric Evaluation

Located on the board are two pins identified as V_{CC} and SIGNAL GND. Connect V_{CC} to a +5V DC supply. If possible limit the supply current to 0.5 to 1.0 Amps. Be sure to have power off when connecting the supply to the board.

SP508 Decoder

The SP508 uses a 3 bit decoder to designate the protocol selected. There is also a decoder latch pin available. Table 2 and Table 3 show the decoder modes for the driver and receiver. Upon power up the latch pin needs to be in a transparent state (logic low or floating) or the SP508 will be in an unknown state. Note that D0, D1, and D2 set as logic high will put the device shutdown overriding all individual enable/disable lines and the drivers outputs and receiver inputs will tri-state. In shutdown mode the termination resistors also disconnect.

Driver Evaluation

Each driver has an internal pull-up so that it is in a defined state when the input is open.

Connect a system clock or a signal generator with a TTL-level output and the appropriate frequency within the acceptable range of the driver under test to driver input you wish to evaluate. There is an individual enable line for each driver that can be used to tri-state the driver. Each enable line has an internal pull up or pull down insure the driver is enabled if the enable pin is not connected or floating. Set the appropriate DIP switch to the “OFF” position to enable the driver under test. Once the power is on and the driver input receives a signal, the driver outputs can be analyzed with an oscilloscope or a digital multimeter. Mode selection can be performed at any time by changing the state of the DIP switches for the 3 bit decoder. The appropriate termination for the driver under test can be added to driver output and tied to the ground buss.

Receiver Evaluation

The SP508 receivers have internal termination appropriate for V.35 and RS-422 modes (refer to the SP508 data sheet for more detail on the receiver termination). The is activated when the receiver is set to act as a V.11 receiver (see Table 3) and the TERM_OFF pin is logic “0”. Each receiver has a fail-safe feature than outputs a logic “1” when the receiver in open, terminated but open, or shorted together. There is an individual enable line for each receiver that can be used to tri-state the driver. Each enable line has an internal pull up or pull down to insure the receiver is enabled if the enable pin is not connected or floating. Set the appropriate DIP switch to the “OFF” position to enable the receiver under test. As with the drivers the mode selection can be performed at any time after power up by changing the state of the 3 bit decoder. To evaluate the receiver the appropriate input signal needs to be applied. To accomplish this provide a signal from an external source or use the SP508 driver output and jumper it to the receiver input. For single ended receivers tie the active driver output to the active receiver input. For differential drivers tie the “A” driver output to the “A” receiver input and the “B” driver output to the “B” receiver input. Using the TTL signal on the driver input will allow the analysis receiver levels and timing characteristics. The DIP switches on the right hand side also provide a means of evaluating the TxC and RRT receivers by tying the ST and RRC drivers to the appropriate receivers eliminating the need for jumper wires.

Driver Receiver Remote Loopback.

The following example uses the ST driver looped back into the TxC receiver, using the 3 bit decoder configure the SP508 for the desired protocol. Connect a jumper cable between the ST(a) pin and the TxC(a) pin. If your mode select is for a differential driver/ receiver, then also connect a jumper cable between the ST(b) pin and the TxC(b) pin. next connect a signal generator to the ST input pin. The signal generator output must be a TTL-level output at a frequency within the acceptable range of the driver mode under test. Be sure that the STEN and the TxCEN DIP switches are set to enable the ST driver and TxC receiver and that the DIP switches tying the ST driver to the TxC receiver are off (refer to section 5.0 Dip switch guide). The driver outputs are now connected back to the receiver inputs so that the driver input to receiver output can be examined. This configuration is similar for the other drivers.

Driver Receiver Local Loopback

The SP508 has the ability to provide an internal loopback. This feature is invoked by a logic “0” on the LOOPBACK pin. The driver input and receiver output characteristics adhere to the appropriate specifications outlined in the data sheet under loopback conditions. The LOOPBACK pin has in internal pull-up resistor so that the SP508 defaults to normal operation during power-up or if the pin is left floating.

DCE DTE selectable configuration

- Configure the decoder for the desired mode.
- The SP508 evaluation board has dip switches setup to allow for the evaluation of a selectable DCE DTE configuration.
- Switch the STEN and RRCEN to the ON position. This will disable the ST and RRC driver outputs. (Refer to the DIP switch guide on Page 8)
- Switch the <TxCEN> and <RRTEN> switches to the ON position. This will disable the TxC and RRT receiver inputs. (Refer to the DIP switch guide on Page 8)
- Switch the ST(A), ST(B), TxC(A), and TxC(B) switches to the ON position. This ties the ST driver outputs to the TxC Receiver inputs.
- Switch the RRC(A), RRC(B), RRT(A), and RRT(B) switches to the ON position. This ties the RRC driver outputs to the RRC receiver inputs.
- To enable a DTE configuration switch the STEN and RRCEN switch to the OFF position. Be sure the TxC and RRT receivers are disabled by switching the TxCEN and RRTEN switches to the ON position. (Refer to the DIP switch guide on Page 8)
- To enable a DCE configuration switch the TxCEN and RRTEN to the OFF position. Be sure to disable the ST and RRC driver outputs by switching the STEN and RRCEN switches to the ON position. (Refer to the DIP switch guide on Page 8)

System Level Evaluation

- The DB-25 Connect if configured as a DTE for EIA-530 pinout. In order to connect other DCE equipment or network analyzers (i.e. the TTC Firebird 6000A), the RxC receiver output must looped back into the TxCE driver input. The RxD output can also be looped back to the TxD input.
- If connecting the evaluation board to a microcontroller such as the Motorola MC68360, jumper wires of the driver inputs and receiver outputs must connect to the μC’s appropriate pins.

DIP SWITCH USERS GUIDE

Driver Enable Dip Switch (off = logic 1, on = logic 0)

The individual switches in the off position leaves the individual enable pin floating (internally pulled up or down?) which enables the driver. The switch in the on position ties the high true enable pins to ground and the low true enable pin (LLEN) to V_{CC} thereby disabling the individual drivers.

Receiver Enable Dip Switch (off = logic 0, on = logic 1)

The individual switches in the off position leaves the individual enable pins floating (internally pulled down or up?) which enables the receiver. The switch in the on position ties all of the enable pins to V_{CC} even the high true TMEN. The TMEN pin is always high no matter what position the dip switch is in. To disable the TM receiver the DIP switch *must be off* and the external pin labeled TMEN is to be jumped to ground.

Decoder DIP Switch (off = logic 1, on = logic 0)

The decoder DIP switch is configured such that the switch in the off position allows the decoder pins to float as well as the notLOOPBACK pin. (all of these pins are assumed to have internal pull-ups.) The dip switch in the on position grounds each of these pins.

DCE_DTE Selectable Switches

- Switch bank 1 ON = ST driver outputs tied to TxC receiver inputs and also tied to D-SUB connector for remote evaluation.
- Switch bank 2 ON = RRC driver outputs tied to RRT receiver inputs and also tied to D-SUB connector for remote evaluation.

SP508 DIP SWITCH TRUTH TABLE

Switch	ON LOGIC	OFF LOGIC	
D0	0	1	DECODER
D1	0	1	DECODER
D2	0	1	DECODER
LOOPBACK	0	1	Logic 0 indicates SP508 is in LOOPBACK mode
TERM_OFF	1	0	Logic 1 internal termination is disables
D_LATCH	1	0	Logic 0 Latch is disabled
SDEN	0	1	Logic 1 TXD driver is enabled
TTEN	0	1	Logic 1 TXCE driver is enabled
STEN	0	1	Logic 1 ST driver is enabled
RSEN	0	1	Logic 1 RTS driver is enabled
TREN	0	1	Logic 1 DTR driver is enabled
RRCEN	0	1	Logic 1 DCD_DCE driver is enabled
RLEN	0	1	Logic 1 SD driver is enabled
LLEN	1	0	Logic 0 LL driver is enabled
RDEN	1	0	Logic 0 RXD receiver is enabled
RTEN	1	0	Logic 0 RXT receiver is enabled
TXCEN	1	0	Logic 0 TXC receiver is enabled
CSEN	1	0	Logic 0 CTS receiver is enabled
DMEN	1	0	Logic 0 DSR receiver is enabled
RRTEN	1	0	Logic 0 DCD_DTE receiver is enabled
ICEN	1	0	Logic 0 RI receiver is enabled
TMEN	0	1	Logic 1 TM receiver is enabled

SP508 PIN ASSIGNMENTS

PIN	Symbol	Description		PIN	Symbol	Description
1	V_{CC}	+5V Power Supply Input		51	TXC(b)	TXC Non-Inverting Input
2	GND	Signal Ground		52	GND	Signal Ground
3	SDEN	TxD Driver Enable input		53	TXC(a)	TXC Inverting Input
4	TTEN	TXCE Driver Enable Input		54	CS(b)	CTS Non-Inverting Input
5	STEN	ST Driver Enable Input		55	CS(a)	CTS Inverting Input
6	RSEN	RTS Driver Enable Input		56	DM(b)	DSR Non-Inverting Input
7	TREN	DTR Driver Enable Input		57	DM(a)	DSR Inverting Input
8	RRCEN	DCDDCE Driver Enable Input		58	V10GND	V.10 Rx Reference Node
9	RLEN	RL Driver Enable Input		59	RRT(b)	DCDDTE Non-Inverting Input
10	LLEN*	LL Driver Enable Input		60	RRT(a)	DCDDTE Inverting Input
11	RDEN*	RxD Receiver Enable Input		61	IC(a)	RI Receiver Input
12	RTEN*	RxT Receiver Enable Input		62	TM(a)	TM Receiver Input
13	TxCEN*	TxC Receiver Enable Input		63	LL(a)	LL Driver Output
14	CSEN*	CTS Receiver Enable Input		64	V_{CC}	+5V Power Supply Input'
15	DMEN*	DSR Receiver Enable Input		65	RL(a)	RL Driver Output
16	RRTEN*	DCDDTE Receiver Enable Input		66	Vss	-2xV_{CC} Charge pump Output
17	ICEN*	RI Receiver Enable Input		67	C2-	Charge pump Capacitor
18	TMEN	TM Receiver Enable Input		68	GND	Signal Ground
19	D0	Mode Select Input		69	C1-	Charge pump Capacitor
20	D1	Mode Select Input		70	C2+	Charge pump Capacitor
21	D2	Mode Select Input		71	V_{CC}	+5V Power Supply Input
22	TERM_OFF	Termination Disable Input		72	C1+	Charge pump Capacitor
23	D_LATCH*	Decoder Latch Input		73	Vdd	2xVxx Charge Pump Output
24	N/C	No Connection		74	GND	Signal Ground
25	GND	Signal Ground		75	TR(a)	DTR Inverting Output
26	V_{CC}	+5V Power Supply Input		76	N/C	No Connection
27	LOOPBACK*	Loopback Mode Enable Input		77	V_{CC}	+5V Power Supply Input
28	TXD	TXD Driver TTL Input		78	TR(b)	DTR Non-Inverting Output
29	TxCE	TXCE Driver TTL Input		79	RRC(b)	DCDDCE Non-Inverting Output
30	ST	ST Driver TTL Input		80	V_{CC}	+5V Power Supply Input
31	DTR	RTS Driver TTL Input		81	RRC(a)	DCDDCE Inverting Output
32	RTS	DTR Driver TTL Input		82	GND	Signal Ground
33	DCD_DCE	DCDDCE Driver TTL Input		83	RS(a)	RTS Inverting Output
34	RL	RL Driver TTL Input		84	V_{CC}	+5V Power Supply Input
35	LL	LL Driver TTL Input		85	RS(b)	RTS Non-Inverting Output
36	RXD	RXD Receiver TTL Output		86	GND	Signal Ground
37	RXC	RXC Receiver TTL Output		87	ST(a)	ST Inverting Output
38	TXC	TXC Receiver TL Output		88	V_{CC}	+5V Power Supply Input
39	CTS	CTS Receiver TTL Output		89	V35TGND3	ST Termination Reference
40	DSR	DSR Receiver TTL Output		90	ST(b)	ST Non-Inverting Output
41	DCD_DTE	DCDDTE Receiver TTL Output		91	GND	Signal Ground
42	RI	RI Receiver TTL Output		92	TT(a)	TXCE Inverting Output
43	TM	TM Receiver TTL Output		93	V_{CC}	+5V Power Supply Input
44	GND	Signal Ground		94	V35TGND2	TXCE Termination Reference
45	V_{CC}	+5V Power Supply Input		95	TT(b)	TXCE Non-Inverting Output
46	V35RGND	Receiver Termination Reference		96	GND	Signal Ground
47	RD(b)	RXD Non-inverting Input		97	SD(a)	TXD Inverting Output
48	RD(a)	RXD Inverting Input		98	V_{CC}	+5V Power Supply Input
49	RT(b)	RXT Non-Inverting Input		99	V35TGND1	TXD Termination Reference
50	RT(a)	RXT Inverting Input		100	SD(b)	TXD Non-Inverting Output

Note:N/C Pins should be left floating as internal signals may be present.
Ensure all V_{CC} and ground connections are made before operating device.

ORDERING INFORMATION

Model	Package
SP508CF	100-pin JEDEC LQFP
SP508CB	132-pin BGA
SP508CEB	SP508 Evaluation Board

SIGNAL PROCESSING EXCELLENCE

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