

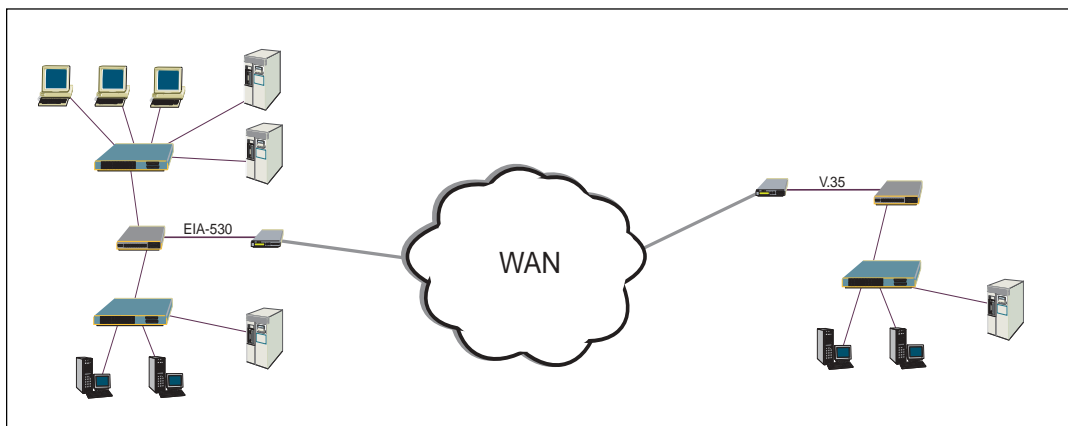
WAN Multi-Mode Serial Transceiver

- +5V Only
- Seven (7) Drivers and Seven (7) Receivers
- Driver and Receiver Tri-State Control
- Reduced V.35 Termination Network
- Pin Compatible with the SP504
- Improved Propagation Delays
- Software Selectable Interface Modes:
 - RS-232E (V.28)
 - RS-422A (V.11, X.21)
 - RS-449 (V.11 & V.10)
 - RS-485
 - V.35
 - EIA-530 (V.11 & V.10)
 - EIA-530A (V.11 & V.10)
 - V.36



DESCRIPTION

The **SP514** is a single chip devices that supports eight (8) physical serial interface standards for Wide Area Network connectivity. The product is fabricated using a low power BiCMOS process technology, and incorporates a **Sipex** patented (5,306,954) charge pump allowing +5V only operation. The **SP514** is 100% compatible with the SP504 multi-protocol serial transceiver IC. All applications using the SP504 can also use the **SP514**. The **SP514** has slightly improved AC performance for its V.35 and V.11 drivers and receivers.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V _{CC}	+7V
Input Voltages:	
Logic.....	-0.3V to (V _{CC} +0.5V)
Drivers.....	-0.3V to (V _{CC} +0.5V)
Receivers.....	±15.5V
Output Voltages:	
Logic.....	-0.3V to (V _{CC} +0.5V)
Drivers.....	±15V
Receivers.....	-0.3V to (V _{CC} +0.5V)
Storage Temperature.....	-65°C to +150°C
Power Dissipation.....	2000mW
Package Derating:	
θ _{JA}	46°C/W
θ _{JC}	16°C/W

STORAGE CONSIDERATIONS

Due to the relatively large package size of the 80-pin quad flat-pack, storage in a low humidity environment is preferred. Large high density plastic packages are moisture sensitive and should be stored in Dry Vapor Barrier Bags. Prior to usage, the parts should remain bagged and stored below 40°C and 60%RH. If the parts are removed from the bag, they should be used within 48 hours or stored in an environment at or below 20%RH. If the above conditions cannot be followed, the parts should be baked for four hours at 125°C in order to remove moisture prior to soldering. Sipex ships the 80-pin QFP in Dry Vapor Barrier Bags with a humidity indicator card and desiccant pack. The humidity indicator should be below 30%RH.

SPECIFICATIONS

T_A = +25°C and V_{CC} = +4.75V to +5.25V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
LOGIC INPUTS					
V _{IL} V _{IH}	2.0		0.8	Volts Volts	
LOGIC OUTPUTS					
V _{OL} V _{OH}	2.4		0.4	Volts Volts	I _{OUT} = -3.2mA I _{OUT} = 1.0mA
V.28 DRIVER					
DC Parameters					
Outputs					
Open Circuit Voltage			±15	Volts	per Figure 1
Loaded Voltage	±5.0		±15	Volts	per Figure 2
Short-Circuit Current			±100	mA	per Figure 4
Power-Off Impedance	300			Ω	per Figure 5
AC Parameters					V _{CC} = +5V & T _A = +25°C for AC parameters
Outputs					
Transition Time			1.5	μs	per Figure 6; +3V to -3V
Instantaneous Slew Rate			30	V/μs	per Figure 3
Propagation Delay					
t _{PHL}	0.5	1	5	μs	
t _{PLH}	0.5	1	5	μs	
Max. Transmission Rate	120	230		kbps	
V.28 RECEIVER					
DC Parameters					
Inputs					
Input Impedance	3		7	kΩ	per Figure 7
Open-Circuit Bias			+2.0	Volts	per Figure 8
HIGH Threshold		1.7	3.0	Volts	
LOW Threshold	0.8	1.2		Volts	
AC Parameters					V _{CC} = +5V & T _A = +25°C for AC parameters
Propagation Delay					
t _{PHL}	50	100	500	ns	
t _{PLH}	50	100	500	ns	

SPECIFICATIONS

T_A = +25°C and V_{CC} = +4.75V to +5.25V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.28 RECEIVER (continued) AC Parameters (cont.) Max. Transmission Rate	120	230		kbps	
V.10 DRIVER DC Parameters Outputs Open Circuit Voltage Test-Terminated Voltage Short-Circuit Current Power-Off Current AC Parameters Outputs Transition Time Propagation Delay t _{PHL} t _{PLH} Max. Transmission Rate	±4.0 0.9V _{OC}		±6.0 ±150 ±100	Volts Volts mA µA ns ns kbps	per Figure 9 per Figure 10 per Figure 11 per Figure 12 V _{CC} = +5V & T _A = +25°C for AC parameters per Figure 13; 10% to 90%
V.10 RECEIVER DC Parameters Inputs Input Current Input Impedance Sensitivity AC Parameters Propagation Delay t _{PHL} t _{PLH} Max. Transmission Rate	-3.25 4		+3.25 ±0.3	mA kΩ Volts ns ns kbps	per Figures 14 and 15 V _{CC} = +5V & T _A = +25°C for AC parameters
V.11 DRIVER DC Parameters Outputs Open Circuit Voltage Test Terminated Voltage Balance Offset Short-Circuit Current Power-Off Current AC Parameters Outputs Transition Time Propagation Delay t _{PHL} t _{PLH} Differential Skew Max. Transmission Rate	±2.0 0.5V _{OC}		±6.0 0.67V _{OC} ±0.4 +3.0 ±150 ±100	Volts Volts Volts Volts mA µA ns ns ns ns Mbps	per Figure 16 per Figure 17 per Figure 17 per Figure 17 per Figure 18 per Figure 19 V _{CC} = +5V & T _A = +25°C for AC parameters per Figures 21 and 36; 10% to 90% Using R _L = 100Ω and C _L = 50pF; per Figures 32 and 36 per Figures 32 and 36 per Figures 32 and 36
V.11 RECEIVER DC Parameters Inputs Common Mode Range Sensitivity	-7		+7 ±0.3	Volts Volts	

SPECIFICATIONS

T_A = +25°C and V_{CC} = +4.75V to +5.25V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.11 RECEIVER (continued)					
DC Parameters (cont.)					
Input Current	-3.25		±3.25	mA	per Figure 20 and 22
Current w/ 100Ω Termination			±60.75	mA	per Figure 23 and 24
Input Impedance	4			kΩ	
AC Parameters					
Propagation Delay					V _{CC} = +5V & T _A = +25°C for AC parameters Using R _L = 100Ω and C _L = 50pF;
t _{PHL}	60	100	125	ns	per Figures 32 and 38
t _{PLH}	60	100	125	ns	per Figures 32 and 38
Differential Skew		20		ns	per Figure 32
Max. Transmission Rate	10			Mbps	
V.35 DRIVER					
DC Parameters					
Outputs					
Test Terminated Voltage	±0.44		±0.66	Volts	per Figure 25
Offset			±0.6	Volts	per Figure 26
Source Impedance	50		150	Ω	per Figure 27
Short-Circuit Impedance	135		165	Ω	per Figure 28
AC Parameters					
Outputs					
Transition Time		30	60	ns	per Figure 29; 10% to 90%
Propagation Delay					
t _{PHL}	50	75	95	ns	per Figures 33 and 36
t _{PLH}	50	75	95	ns	per Figures 33 and 36
Differential Skew		20	40	ns	per Figures 33 and 36
Max. Transmission Rate	10			Mbps	
V.35 RECEIVER					
DC Parameters					
Inputs					
Sensitivity		80		mV	
Source Impedance	90		110	Ω	per Figure 30
Short-Circuit Impedance	135		165	Ω	per Figure 31
AC Parameters					
Propagation Delay					V _{CC} = +5V & T _A = +25°C for AC parameters
t _{PHL}	60	115	125	ns	per Figures 33 and 38
t _{PLH}	60	115	125	ns	per Figures 33 and 38
Differential Skew		20		ns	per Figure 33
Max. Transmission Rate	10			Mbps	
POWER REQUIREMENTS					
V _{CC}	4.75	5.00	5.25	Volts	
I _{CC} (No Mode Selected)		30		mA	All I _{CC} values are with V _{CC} = +5V f _{IN} = 120kbps; Drivers active & loaded. f _{IN} = 2.1Mbps; Drivers active & loaded. f _{IN} = 2.1Mbps; Drivers active & loaded. V.35 @ f _{IN} = 2.1Mbps, V.28 @ 20kbps; Drivers active & loaded.
(V.28/RS-232)		130		mA	
(V.11/RS-422)		280		mA	
(EIA-530 & RS-449)		250		mA	
(V.35)		180		mA	
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature Range	0		+70	°C	
Storage Temperature Range	-65		+150	°C	

OTHER AC CHARACTERISTICS

$T_A = +25^\circ\text{C}$ and $V_{CC} = +5.0\text{V}$ unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE					
RS-232/V.28 MODE					
t_{PZL} : Tri-state to Output LOW		0.70	5.0	μs	$C_L = 100\text{pF}$, Fig. 34 ; S_1 closed
t_{PZH} : Tri-state to Output HIGH		0.40	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 ; S_2 closed
t_{PLZ} : Output LOW to Tri-state		0.20	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 ; S_1 closed
t_{PHZ} : Output HIGH to Tri-state		0.40	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 ; S_2 closed
RS-423/V.10 MODE					
t_{PZL} : Tri-state to Output LOW		0.15	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 ; S_1 closed
t_{PZH} : Tri-state to Output HIGH		0.20	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 ; S_2 closed
t_{PLZ} : Output LOW to Tri-state		0.20	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 ; S_1 closed
t_{PHZ} : Output HIGH to Tri-state		0.15	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 ; S_2 closed
RS-422/V.11 MODE					
t_{PZL} : Tri-state to Output LOW		2.80	10.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 37; S_1 closed
t_{PZH} : Tri-state to Output HIGH		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 37; S_2 closed
t_{PLZ} : Output LOW to Tri-state		0.10	2.0	μs	$C_L = 15\text{pF}$, Fig. 34 & 37; S_1 closed
t_{PHZ} : Output HIGH to Tri-state		0.10	2.0	μs	$C_L = 15\text{pF}$, Fig. 34 & 37; S_2 closed
V.35 MODE					
t_{PZL} : Tri-state to Output LOW		2.60	10.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 37; S_1 closed
t_{PZH} : Tri-state to Output HIGH		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 37; S_2 closed
t_{PLZ} : Output LOW to Tri-state		0.10	2.0	μs	$C_L = 15\text{pF}$, Fig. 34 & 37; S_1 closed
t_{PHZ} : Output HIGH to Tri-state		0.15	2.0	μs	$C_L = 15\text{pF}$, Fig. 34 & 37; S_2 closed
RECEIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE					
RS-232 MODE					
t_{PZL} : Tri-state to Output LOW		0.12	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 ; S_1 closed
t_{PZH} : Tri-state to Output HIGH		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 ; S_2 closed
t_{PLZ} : Output LOW to Tri-state		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 ; S_1 closed
t_{PHZ} : Output HIGH to Tri-state		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 ; S_2 closed
RS-423 MODE					
t_{PZL} : Tri-state to Output LOW		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 ; S_1 closed
t_{PZH} : Tri-state to Output HIGH		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 ; S_2 closed
t_{PLZ} : Output LOW to Tri-state		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 ; S_1 closed
t_{PHZ} : Output HIGH to Tri-state		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 ; S_2 closed
RS-422/RS-485 MODES					
t_{PZL} : Tri-state to Output LOW		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 39; S_1 closed
t_{PZH} : Tri-state to Output HIGH		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 39; S_2 closed
t_{PLZ} : Output LOW to Tri-state		0.10	2.0	μs	$C_L = 15\text{pF}$, Fig. 35 & 39; S_1 closed
t_{PHZ} : Output HIGH to Tri-state		0.10	2.0	μs	$C_L = 15\text{pF}$, Fig. 35 & 39; S_2 closed
V.35 MODE					
t_{PZL} : Tri-state to Output LOW		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 39; S_1 closed
t_{PZH} : Tri-state to Output HIGH		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 39; S_2 closed
t_{PLZ} : Output LOW to Tri-state		0.10	2.0	μs	$C_L = 15\text{pF}$, Fig. 35 & 39; S_1 closed
t_{PHZ} : Output HIGH to Tri-state		0.10	2.0	μs	$C_L = 15\text{pF}$, Fig. 35 & 39; S_2 closed

OTHER AC CHARACTERISTICS (Continued)

$T_A = +25^\circ\text{C}$ and $V_{CC} = +5.0\text{V}$ unless otherwise noted.

TRANSCIVER TO TRANSCIVER SKEW				(PER FIGURES 32, 33, 36, 38)	
RS-232 Driver		100		ns	$[(t_{\text{phl}})_{\text{Tx1}} - (t_{\text{phl}})_{\text{Tx6,7}}]$
		100		ns	$[(t_{\text{plh}})_{\text{Tx1}} - (t_{\text{plh}})_{\text{Tx6,7}}]$
RS-232 Receiver		20		ns	$[(t_{\text{phl}})_{\text{Rx1}} - (t_{\text{phl}})_{\text{Rx2,7}}]$
		20		ns	$[(t_{\text{plh}})_{\text{Rx1}} - (t_{\text{plh}})_{\text{Rx2,7}}]$
RS-422 Driver		2		ns	$[(t_{\text{phl}})_{\text{Tx1}} - (t_{\text{phl}})_{\text{Tx6,7}}]$
		2		ns	$[(t_{\text{plh}})_{\text{Tx1}} - (t_{\text{plh}})_{\text{Tx6,7}}]$
RS-422 Receiver		3		ns	$[(t_{\text{phl}})_{\text{Rx1}} - (t_{\text{phl}})_{\text{Rx2,7}}]$
		3		ns	$[(t_{\text{plh}})_{\text{Rx1}} - (t_{\text{plh}})_{\text{Rx2,7}}]$
RS-423 Driver		5		ns	$[(t_{\text{phl}})_{\text{Tx2}} - (t_{\text{phl}})_{\text{Tx3,4,5}}]$
		5		ns	$[(t_{\text{plh}})_{\text{Tx2}} - (t_{\text{plh}})_{\text{Tx3,4,5}}]$
RS-423 Receiver		5		ns	$[(t_{\text{phl}})_{\text{Rx2}} - (t_{\text{phl}})_{\text{Rx3,4,5}}]$
		5		ns	$[(t_{\text{plh}})_{\text{Rx2}} - (t_{\text{plh}})_{\text{Rx3,4,5}}]$
V.35 Driver		4		ns	$[(t_{\text{phl}})_{\text{Tx1}} - (t_{\text{phl}})_{\text{Tx6,7}}]$
		4		ns	$[(t_{\text{plh}})_{\text{Tx1}} - (t_{\text{plh}})_{\text{Tx6,7}}]$
V.35 Receiver		6		ns	$[(t_{\text{phl}})_{\text{Rx1}} - (t_{\text{phl}})_{\text{Rx2,7}}]$
		6		ns	$[(t_{\text{plh}})_{\text{Rx1}} - (t_{\text{plh}})_{\text{Rx2,7}}]$

TEST CIRCUITS...

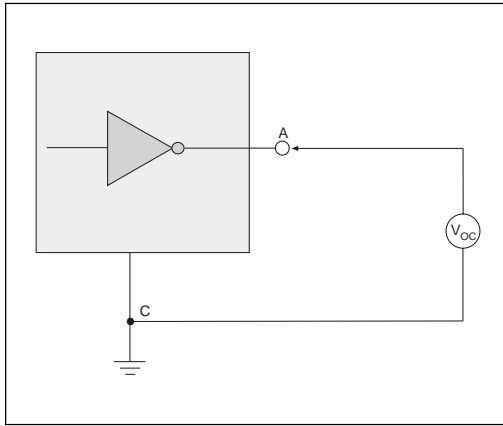


Figure 1. V.28 Driver Output Open Circuit Voltage

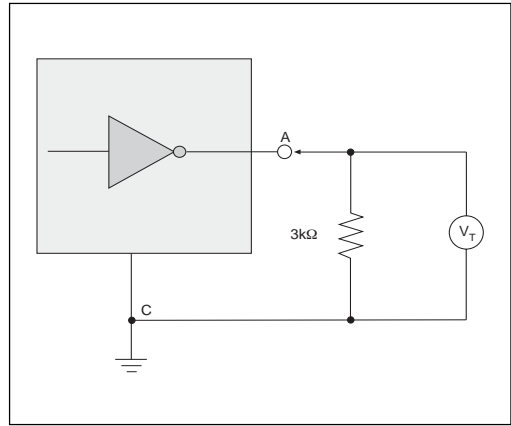


Figure 2. V.28 Driver Output Loaded Voltage

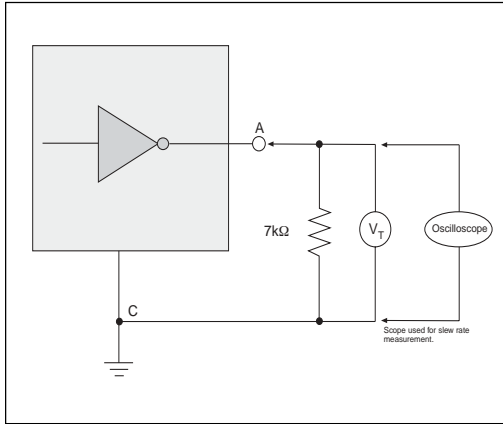


Figure 3. V.28 Driver Output Slew Rate

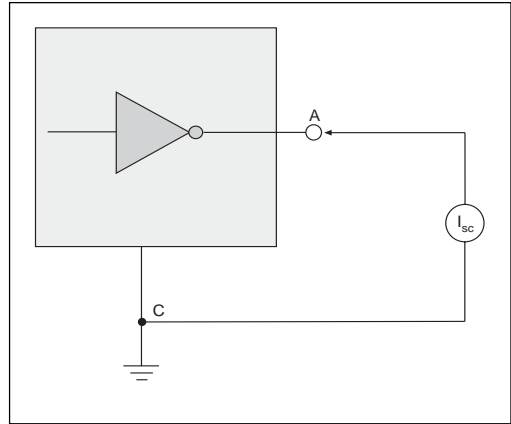


Figure 4. V.28 Driver Output Short-Circuit Current

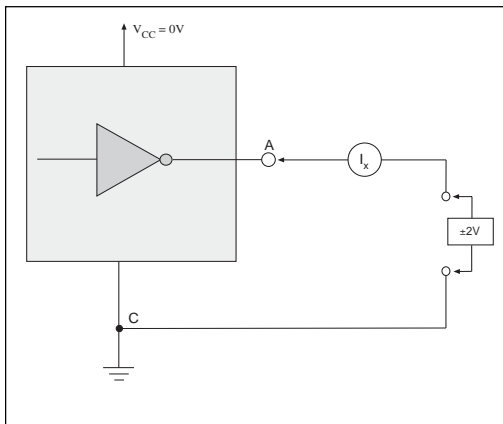


Figure 5. V.28 Driver Output Power-Off Impedance

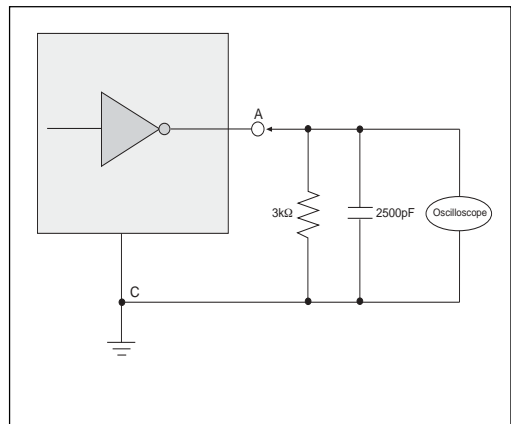


Figure 6. Driver Output Rise/Fall Times

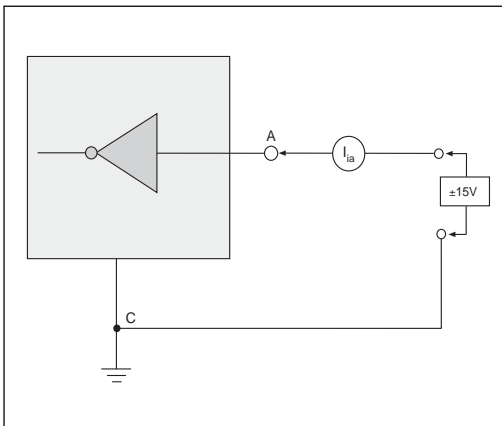


Figure 7. V.28 Receiver Input Impedance

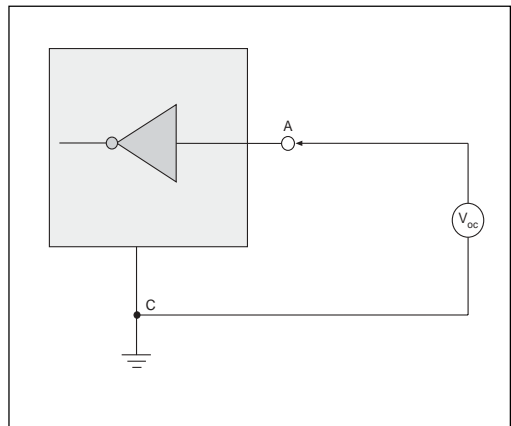


Figure 8. V.28 Receiver Input Open Circuit Bias

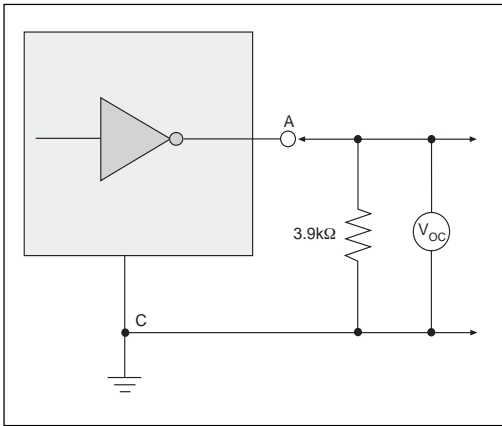


Figure 9. V.10 Driver Output Open-Circuit Voltage

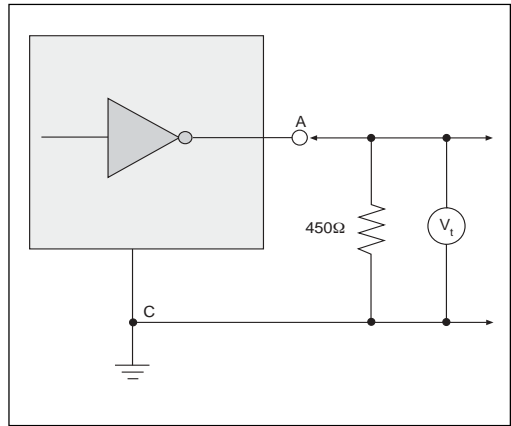


Figure 10. V.10 Driver Output Test Terminated Voltage

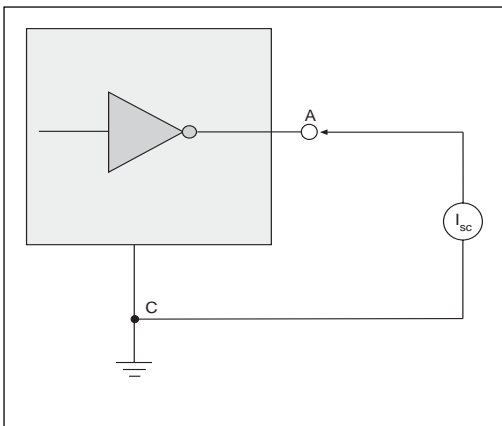


Figure 11. V.10 Driver Output Short-Circuit Current

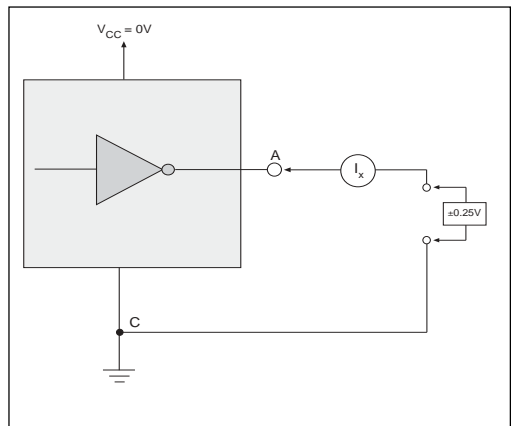


Figure 12. V.10 Driver Output Power-Off Current

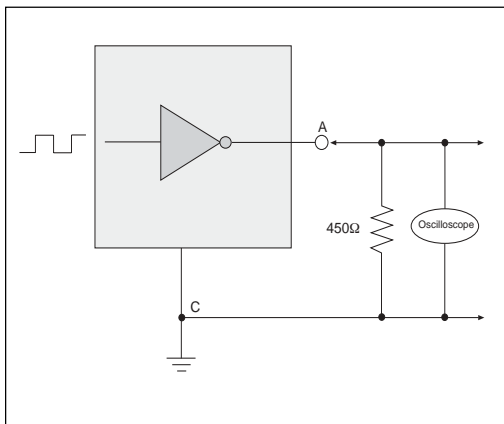


Figure 13. V.10 Driver Output Transition Time

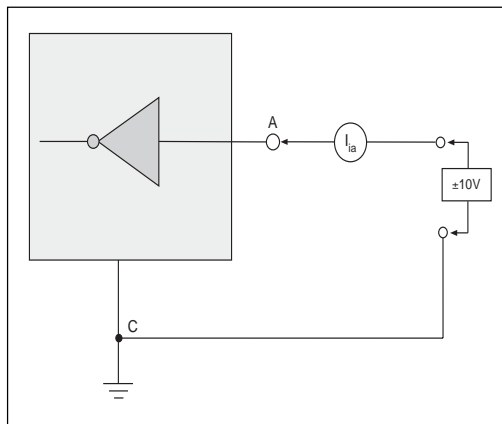


Figure 14. V.10 Receiver Input Current

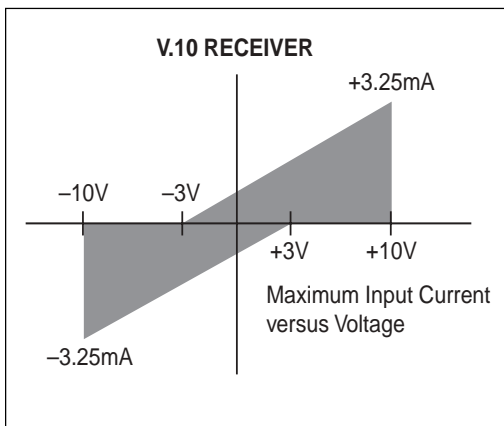


Figure 15. V.10 Receiver Input IV Graph

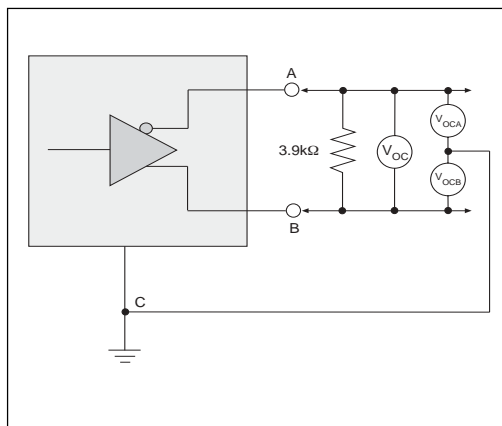


Figure 16. V.11 Driver Output Open-Circuit Voltage

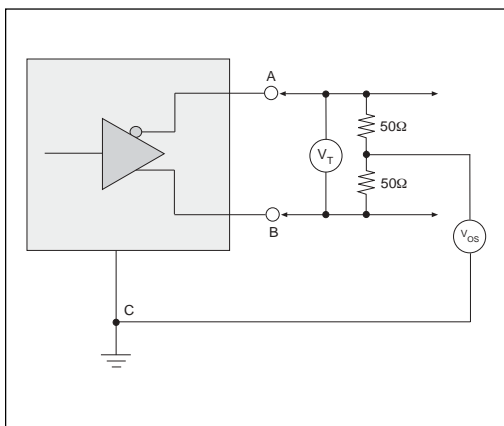


Figure 17. V.11 Driver Output Test Terminated Voltage

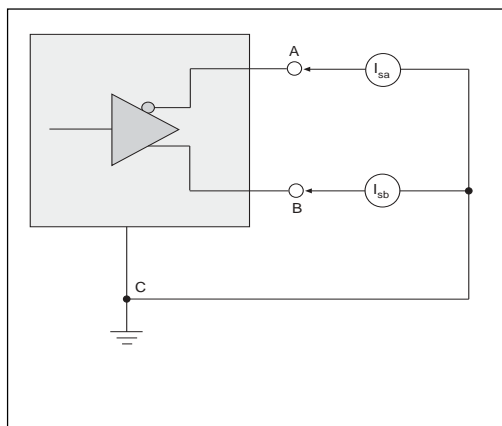


Figure 18. V.11 Driver Output Short-Circuit Current

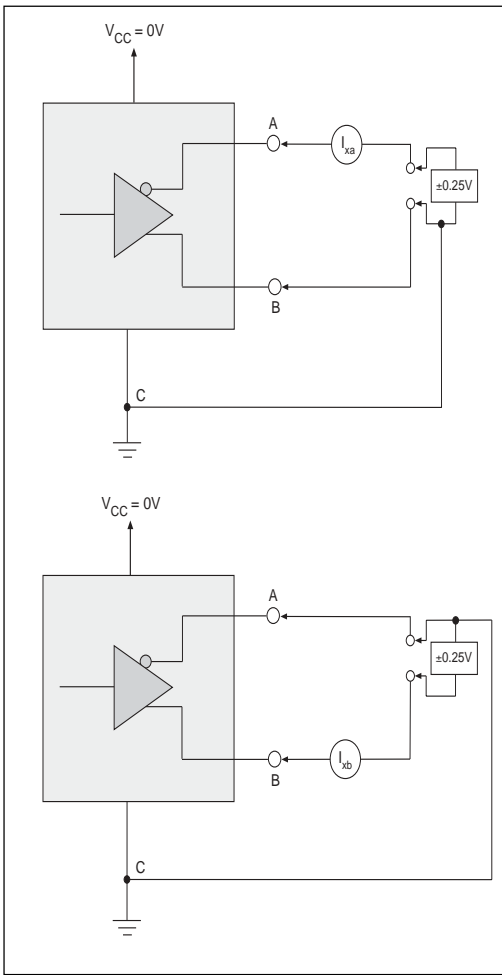


Figure 19. V.11 Driver Output Power-Off Current

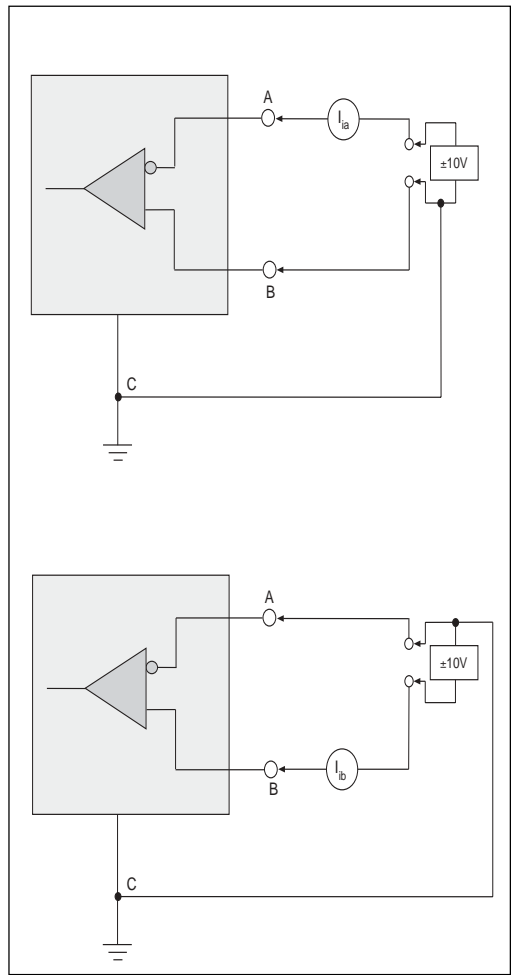


Figure 20. V.11 Receiver Input Current

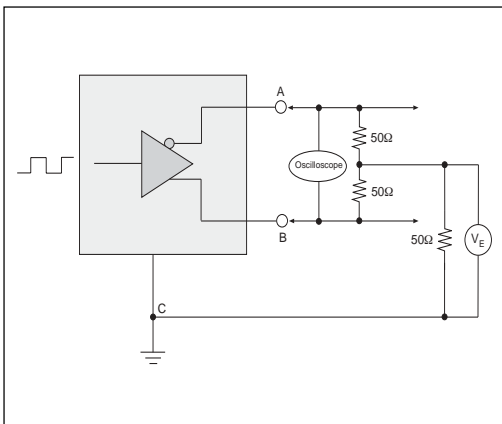


Figure 21. V.11 Driver Output Rise/Fall Time

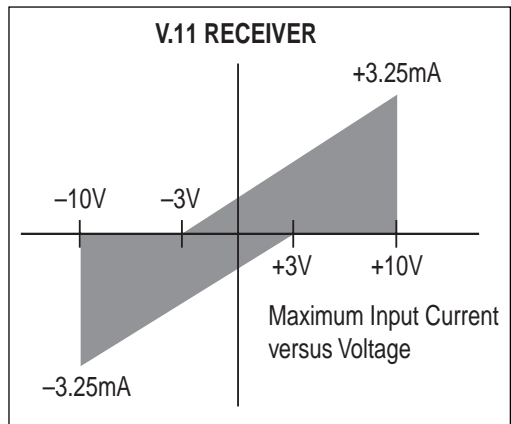


Figure 22. V.11 Receiver Input IV Graph

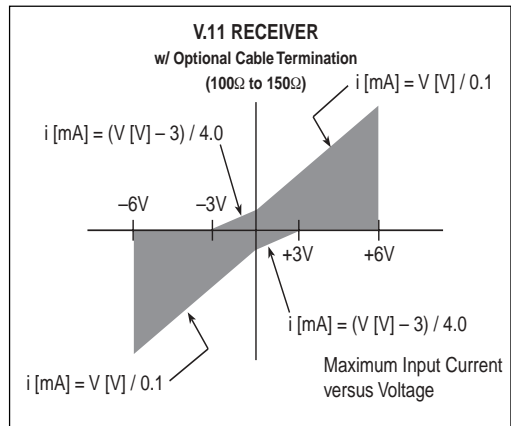
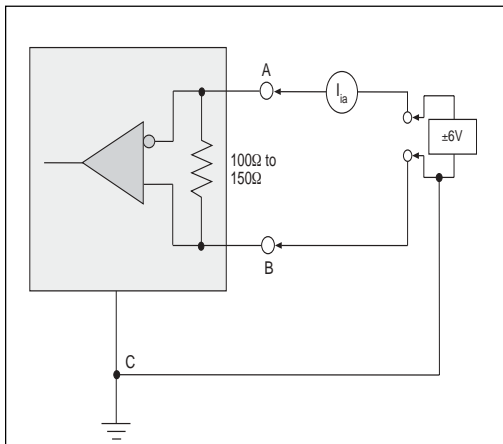


Figure 24. V.11 Receiver Input Graph w/ Termination

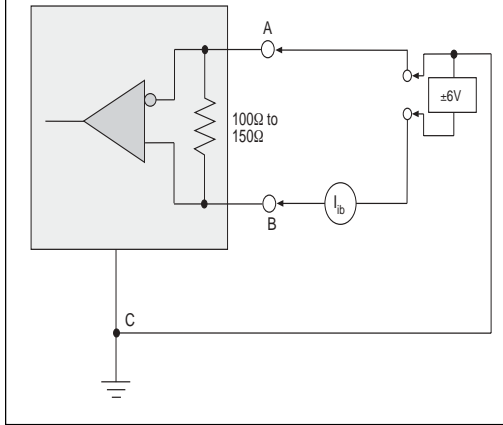


Figure 23. V.11 Receiver Input Current w/ Termination

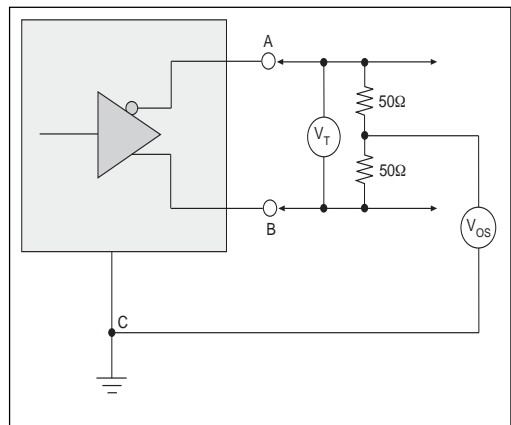


Figure 25. V.35 Driver Output Test Terminated Voltage

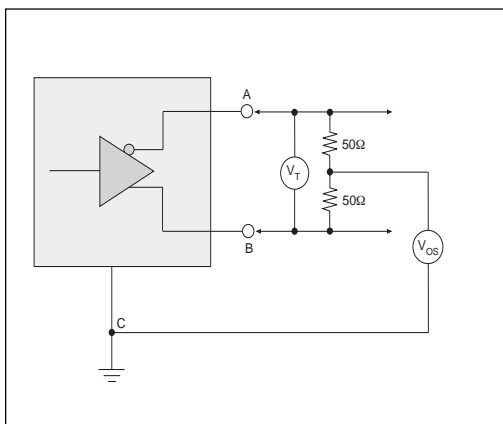


Figure 26. V.35 Driver Output Offset Voltage

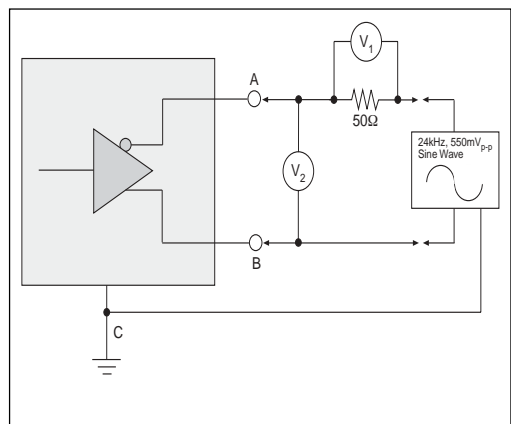


Figure 27. V.35 Driver Output Source Impedance

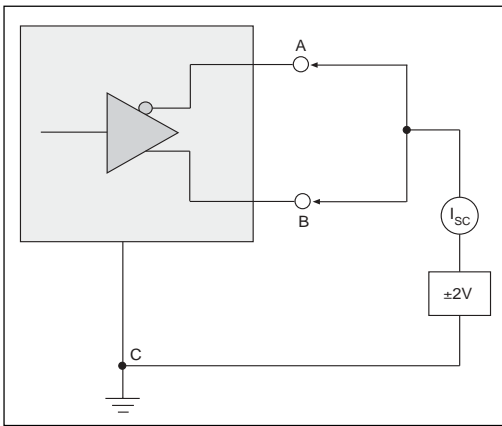


Figure 28. V.35 Driver Output Short-Circuit Impedance

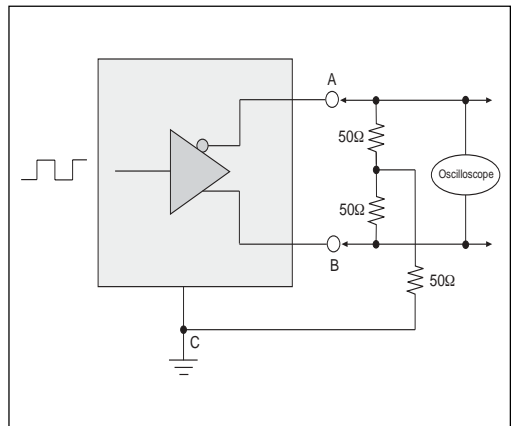


Figure 29. V.35 Driver Output Rise/Fall Time

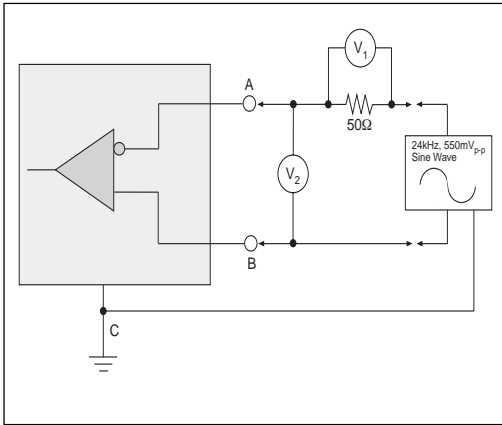


Figure 30. V.35 Receiver Input Source Impedance

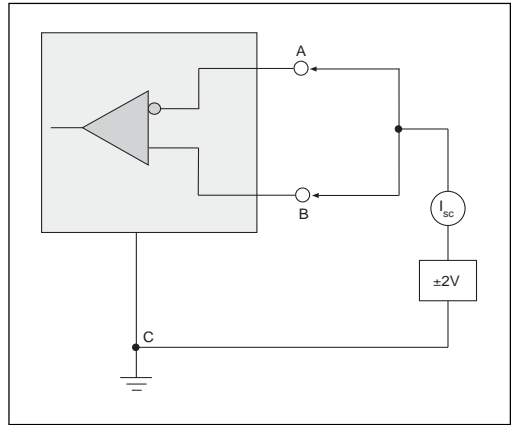


Figure 31. V.35 Receiver Input Short-Circuit Impedance

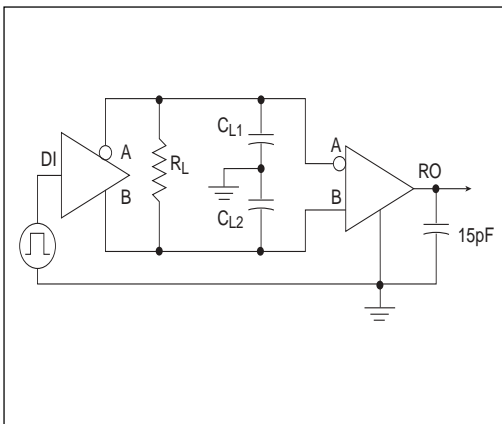


Figure 32. Driver/Receiver Timing Test Circuit

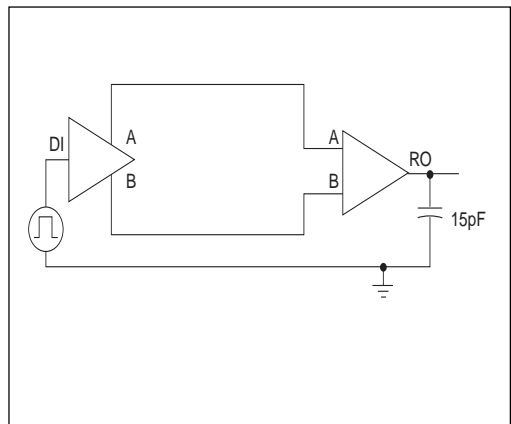


Figure 33. Timing Test Ckt. (V.35 mode only for SP514)

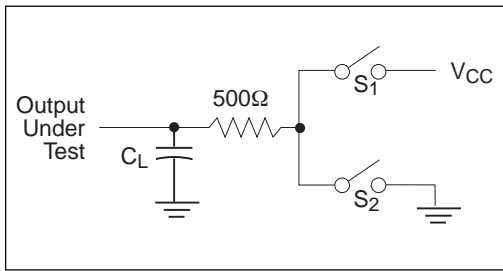


Figure 34. Driver Timing Test Load Circuit

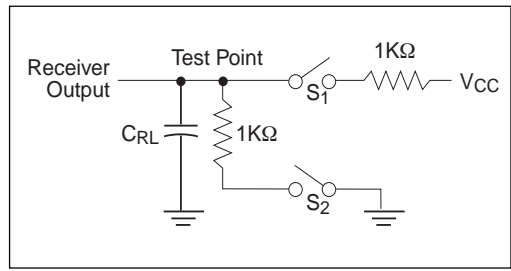


Figure 35. Receiver Timing Test Load Circuit

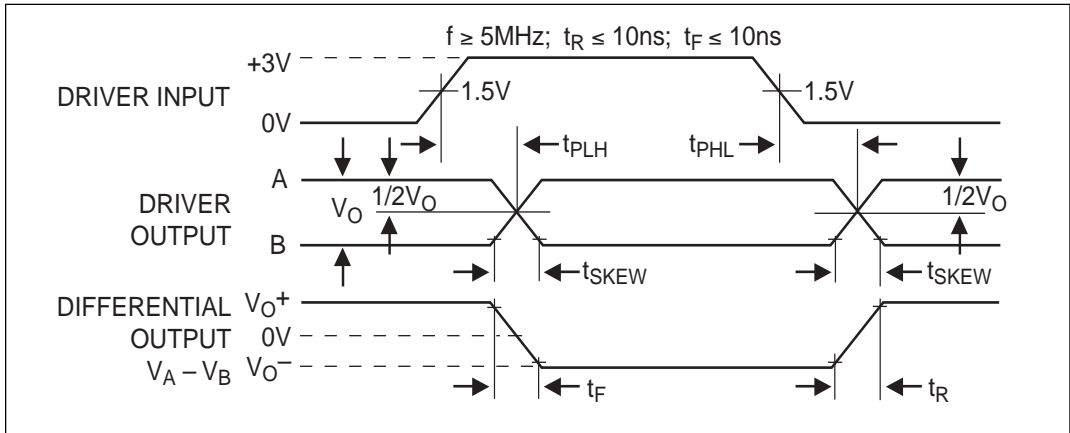


Figure 36. Driver Propagation Delays

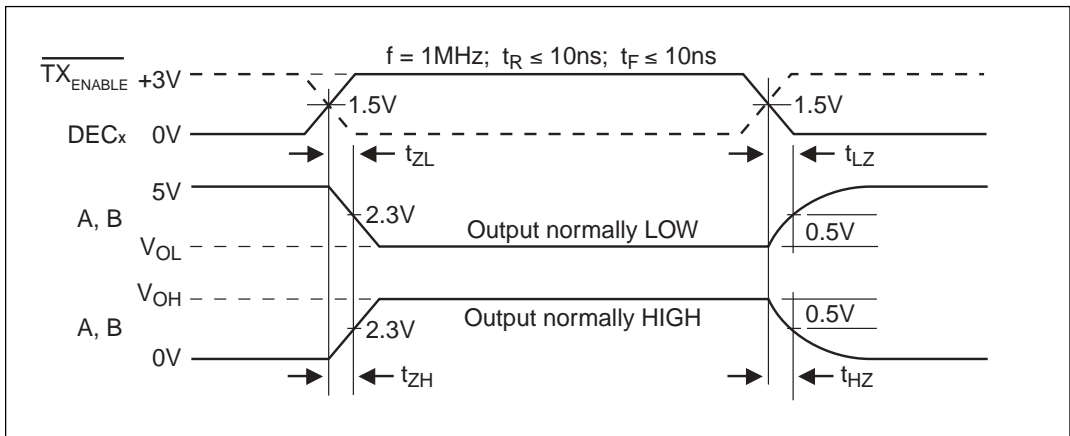


Figure 37. Driver Enable and Disable Times

Note: Figure 36 shown above is corrected from Figure 5 in SP504 Datasheet. Figure 5 in the SP504 Datasheet is incorrect where A and B are reversed and the $V_A - V_B$ output should be inverted.

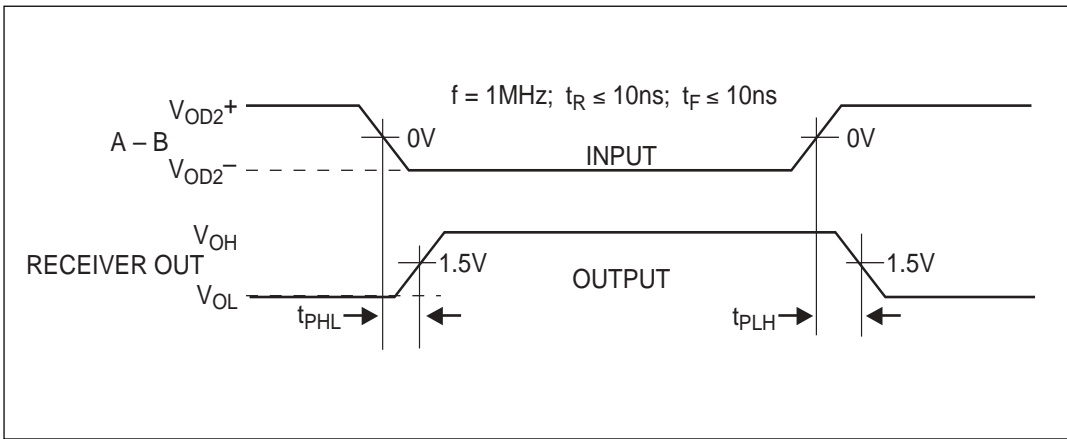


Figure 38. Receiver Propagation Delays

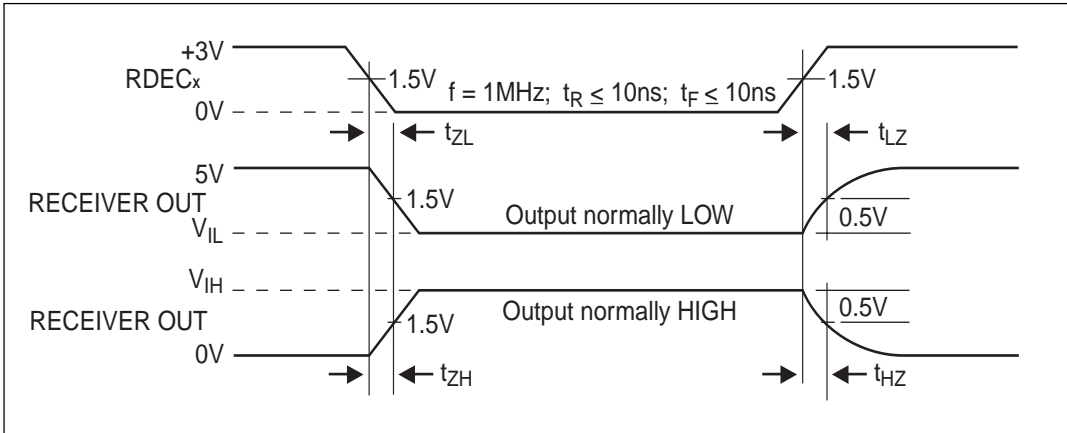
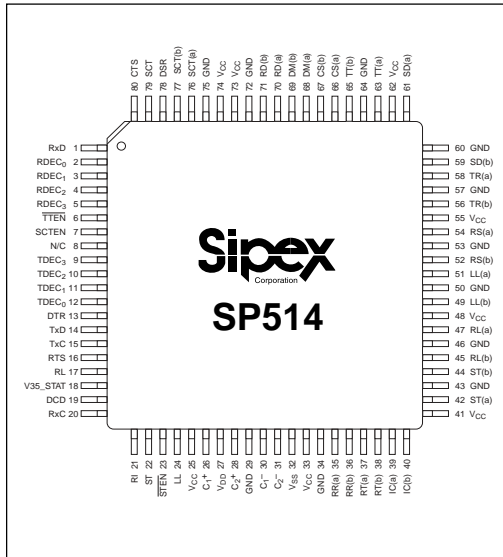


Figure 39. Receiver Enable and Disable Times

Note: Figure 38 shown above is corrected from Figure 7 in the original SP504 Datasheet. Figure 7 in the original SP504 Datasheet is incorrect where the RECEIVER OUTPUT should be inverted.

PINOUT...



PIN ASSIGNMENTS...

CLOCK AND DATA GROUP

Pin 1 — RxD — Receive Data; TTL output, sourced from RD(a) and RD(b) inputs.

Pin 14 — TxD — TTL input ; transmit data source for SD(a) and SD(b) outputs.

Pin 15 — TxC — Transmit Clock; TTL input for TT driver outputs.

Pin 20 — RxC — Receive Clock; TTL output sourced from RT(a) and RT(b) inputs.

Pin 22 — ST — Send Timing; TTL input; source for ST(a) and ST(b) outputs.

Pin 37 — RT(a) — Receive Timing; analog input, inverted; source for RxC.

Pin 38 — RT(b) — Receive Timing; analog input, non-inverted; source for RxC.

Pin 42 — ST(a) — Send Timing; analog output, inverted; sourced from ST.

Pin 44 — ST(b) — Send Timing; analog output, non-inverted; sourced from ST.

Pin 59 — SD(b) — Analog Out — Send data, non-inverted; sourced from TxD.

Pin 61 — SD(a) — Analog Out — Send data, inverted; sourced from TxD.

Pin 63 — TT(a) — Analog Out — Terminal Timing, inverted; sourced from TxC

Pin 65 — TT(b) — Analog Out — Terminal Timing, non-inverted; sourced from TxC.

Pin 70 — RD(a) — Receive Data, analog input; inverted; source for RxD.

Pin 71 — RD(b) — Receive Data; analog input; non-inverted; source for RxD.

Pin 76 — SCT(a) — Serial Clock Transmit; analog input, inverted; source for SCT.

Pin 77 — SCT(b) — Serial Clock Transmit; analog input, non-inverted; source for SCT

Pin 79 — SCT — Serial Clock Transmit; TTL output; sources from SCT(a) and SCT(b) inputs.

CONTROL LINE GROUP

Pin 13 — DTR — Data Terminal Ready; TTL input; source for TR(a) and TR(b) outputs.

Pin 16 — RTS — Ready To Send; TTL input; source for RS(a) and RS(b) outputs.

Pin 17 — RL — Remote Loopback; TTL input; source for RL(a) and RL(b) outputs.

Pin 18 — V35_STAT — V.35 Status; TTL output; outputs logic high when in V.35 mode.

Pin 19 — DCD — Data Carrier Detect; TTL output; sourced from RR(a) and RR(b) inputs.

Pin 21 — RI — Ring Indicate; TTL output; sourced from IC(a) and IC(b) inputs.

Pin 24 — LL — Local Loopback; TTL input; source for LL(a) and LL(b) outputs.

Pin 35 — RR(a) — Receiver Ready; analog input, inverted; source for DCD.

Pin 36 — RR(b) — Receiver Ready; analog input, non-inverted; source for DCD.

Pin 39 — IC(a) — Incoming Call; analog input, inverted; source for RI.

Pin 40 — IC(b)— Incoming Call; analog input, non-inverted; source for RI.

Pin 45 — RL(b) — Remote Loopback; analog output, non-inverted; sourced from RL.

Pin 47 — RL(a) — Remote Loopback; analog output inverted; sourced from RL.

Pin 49— LL(b) — Local Loopback; analog output, non-inverted; sourced from LL.

Pin 51 — LL(a) — Local Loopback; analog output, inverted; sourced from LL.

Pin 52 — RS(b) — Ready To Send; analog output, non-inverted; sourced from RTS.

Pin 54 — RS(a) — Ready To Send; analog output, inverted; sourced from RTS.

Pin 56 — TR(b) — Terminal Ready; analog output, non-inverted; sourced from DTR.

Pin 58 — TR(a) — Terminal Ready; analog output, inverted; sourced from DTR.

Pin 66 — CS(a)— Clear To Send; analog input, inverted; source for CTS.

Pin 67 — CS(b)— Clear To Send; analog input, non-inverted; source for CTS.

Pin 68 — DM(a)— Data Mode; analog input, inverted; source for DSR.

Pin 69 — DM(b)— Data Mode; analog input, non-inverted; source for DSR

Pin 78 — DSR— Data Set Ready; TTL output; sourced from DM(a), DM(b) inputs.

Pin 80 — CTS— Clear To Send; TTL output; sourced from CS(a) and CS(b) inputs.

CONTROL REGISTERS

Pins 2–5 — RDEC₀ – RDEC₃ — Receiver decode register; configures receiver modes; TTL inputs.

Pin 6 — $\overline{\text{TEN}}$ — Enables TT driver, active low; TTL input.

Pin 7 — SCTEN — Enables SCT receiver; active high; TTL input.

Pins 12–9 — TDEC₀ – TDEC₃ — Transmitter decode register; configures transmitter modes; TTL inputs.

Pin 23 — $\overline{\text{STEN}}$ — Enables ST driver; active low; TTL input.

POWER SUPPLIES

Pins 25, 33, 41, 48, 55, 62, 73, 74 — V_{CC}— +5V input.

Pins 29, 34, 43, 46, 50, 53, 57, 60, 64, 72, 75 — GND — Ground.

Pin 27 — V_{DD} +10V Charge Pump Capacitor — Connects from V_{DD} to V_{CC}. Suggested capacitor size is 22μF, 16V.

Pin 32 — V_{SS} –10V Charge Pump Capacitor — Connects from ground to V_{SS}. Suggested capacitor size is 22μF, 16V.

Pins 26 and 30 — C₁⁺ and C₁⁻ — Charge Pump Capacitor — Connects from C₁⁺ to C₁⁻. Suggested capacitor size is 22μF, 16V.

Pins 28 and 31 — C₂⁺ and C₂⁻ — Charge Pump Capacitor — Connects from C₂⁺ to C₂⁻. Suggested capacitor size is 22μF, 16V.

NOTE: NC pins should be left floating; internal signals may be present.

SP514 Driver Mode Selection

Pin Label	Mode:	RS232	V.35	RS422	RS485	RS449	EIA530	EIA-530A	V.36
TDEC ₃ -TDEC ₀	0000	0010	1110	0100	0101	1100	1101	1111	0110
SD(a)	tri-state	V.28	V.35-	V.11-	RS485-	V.11-	V.11-	V.11-	V.11-
SD(b)	tri-state	tri-state	V.35+	V.11+	RS485+	V.11+	V.11+	V.11+	V.11+
TR(a)	tri-state	V.28	V.28	V.11-	RS485-	V.11-	V.11-	V.10	V.10
TR(b)	tri-state	tri-state	tri-state	V.11+	RS485+	V.11+	V.11+	tri-state	tri-state
RS(a)	tri-state	V.28	V.28	V.11-	RS485-	V.11-	V.11-	V.11-	V.10
RS(b)	tri-state	tri-state	tri-state	V.11+	RS485+	V.11+	V.11+	V.11+	tri-state
RL(a)	tri-state	V.28	V.28	V.11-	RS485-	V.10	V.10	V.11-	V.10
RL(b)	tri-state	tri-state	tri-state	V.11+	RS485+	tri-state	tri-state	V.11+	tri-state
LL(a)	tri-state	V.28	V.28	V.11-	RS485-	V.10	V.10	V.10	V.10
LL(b)	tri-state	tri-state	tri-state	V.11+	RS485+	tri-state	tri-state	tri-state	tri-state
ST(a)	tri-state	V.28	V.35-	V.11-	RS485-	V.11-	V.11-	V.11-	V.11-
ST(b)	tri-state	tri-state	V.35+	V.11+	RS485+	V.11+	V.11+	V.11+	V.11+
TT(a)	tri-state	V.28	V.35-	V.11-	RS485-	V.11-	V.11-	V.11-	V.11-
TT(b)	tri-state	tri-state	V.35+	V.11+	RS485+	V.11+	V.11+	V.11+	V.11+

SP514 Receiver Mode Selection

Pin Label	Mode:	RS232	V.35	RS422	RS485	RS449	EIA530	EIA-530A	V.36
RDEC ₃ -RDEC ₀	0000	0010	1110	0100	0101	1100	1101	1111	0110
RD(a)	>12kΩ to GND	V.28	V.35-	V.11-	RS485-	V.11-	V.11-	V.11-	V.11-
RD(b)	>12kΩ to GND	>12kΩ to GND	V.35+	V.11+	RS485+	V.11+	V.11+	V.11+	V.11+
RT(a)	>12kΩ to GND	V.28	V.35-	V.11-	RS485-	V.11-	V.11-	V.11-	V.11-
RT(b)	>12kΩ to GND	>12kΩ to GND	V.35+	V.11+	RS485+	V.11+	V.11+	V.11+	V.11+
CS(a)	>12kΩ to GND	V.28	V.28	V.11-	RS485-	V.11-	V.11-	V.11-	V.10
CS(b)	>12kΩ to GND	>12kΩ to GND	>12kΩ to GND	V.11+	RS485+	V.11+	V.11+	V.11+	>12kΩ to GND
DM(a)	>12kΩ to GND	V.28	V.28	V.11-	RS485-	V.11-	V.11-	V.10	V.10
DM(b)	>12kΩ to GND	>12kΩ to GND	>12kΩ to GND	V.11+	RS485+	V.11+	V.11+	>12kΩ to GND	>12kΩ to GND
RR(a)	>12kΩ to GND	V.28	V.28	V.11-	RS485-	V.11-	V.11-	V.11-	V.10
RR(b)	>12kΩ to GND	>12kΩ to GND	>12kΩ to GND	V.11+	RS485+	V.11+	V.11+	V.11+	>12kΩ to GND
IC(a)	>12kΩ to GND	V.28	V.28	V.11-	RS485-	V.10	V.10	V.10	V.10
IC(b)	>12kΩ to GND	>12kΩ to GND	>12kΩ to GND	V.11+	RS485+	>12kΩ to GND	>12kΩ to GND	>12kΩ to GND	>12kΩ to GND
SCT(a)	>12kΩ to GND	V.28	V.35-	V.11-	RS485-	V.11-	V.11-	V.11-	V.11-
SCT(b)	>12kΩ to GND	>12kΩ to GND	V.35+	V.11+	RS485+	V.11+	V.11+	V.11+	V.11+

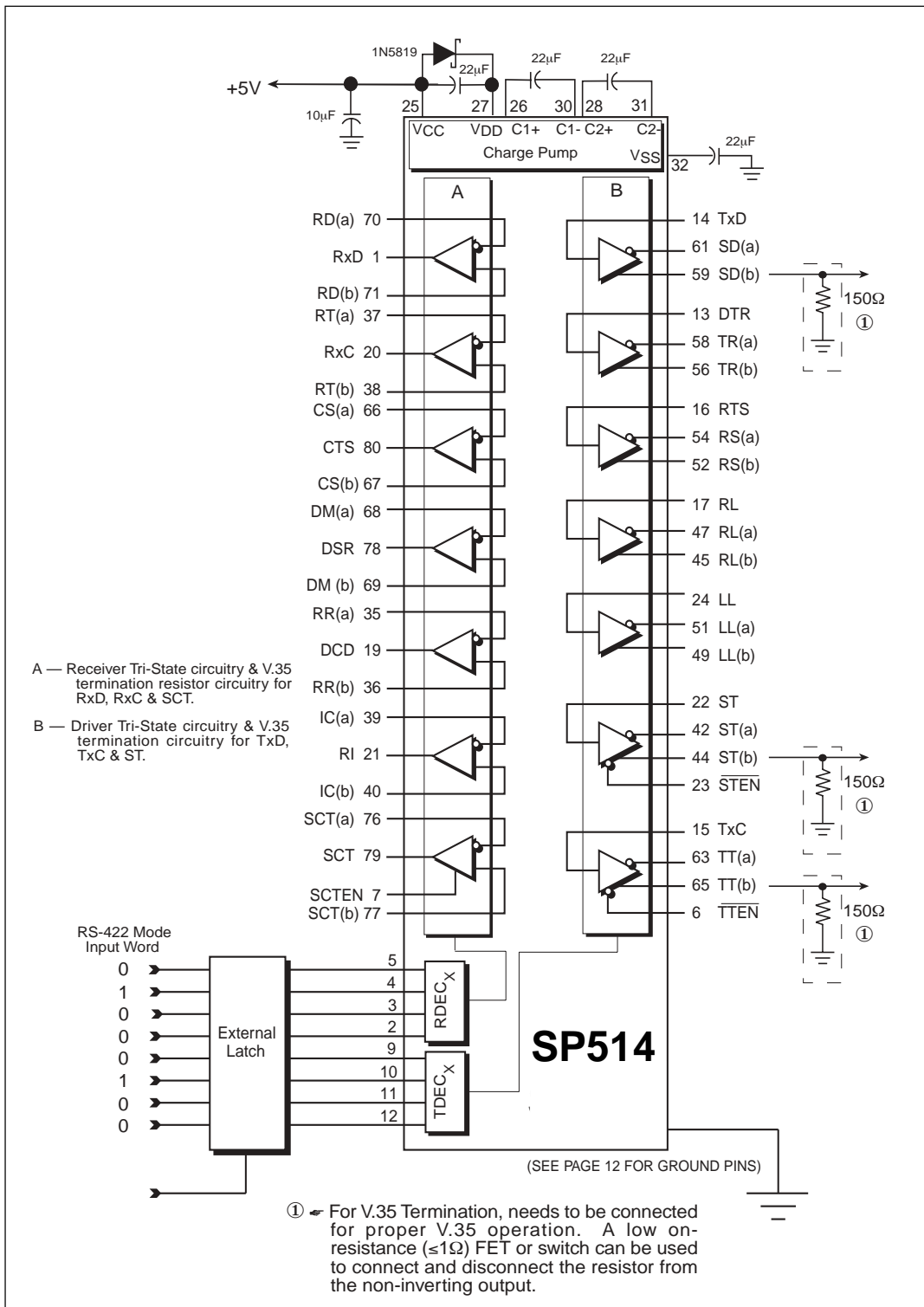
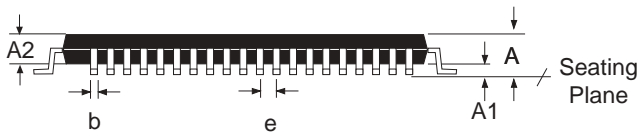
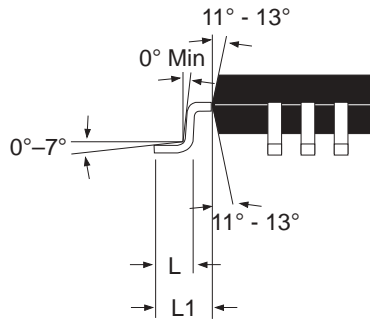
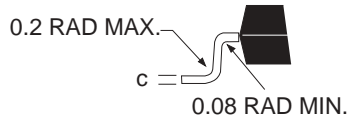
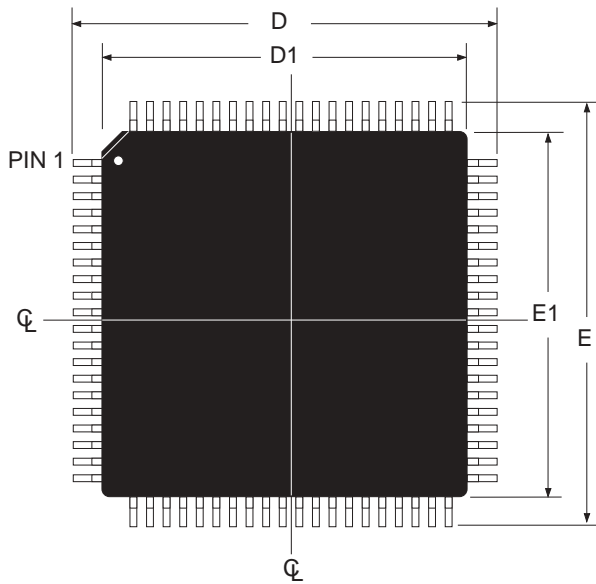


Figure 40. SP514 Typical Operating Circuit

PACKAGE: 80 Pin LQFP



DIMENSIONS Minimum/Maximum (mm)	80-PIN LQFP JEDEC MS-026 (BEC) Variation		
SYMBOL	MIN	NOM	MAX
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
D	16.00 BSC		
D1	14.00 BSC		
e	0.65 BSC		
E	16.00 BSC		
E1	14.00 BSC		
N	80		

COMMON DIMENTIONS			
SYMBL	MIN	NOM	MAX
c	0.11		23.00
L	0.45	0.60	0.75
L1	1.00 BASIC		

80 PIN LQFP

ORDERING INFORMATION

Model SP514CF	Temperature Range 0°C to +70°C	Package Types 80-pin JEDEC (BE-2 Outline) LQFP
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REVISION HISTORY

DATE	REVISION	DESCRIPTION
3/05/04	A	Implemented tracking revision.



ANALOG EXCELLENCE

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