SPT205

OVERDRIVE-PROTECTED WIDEBAND OP AMP

General Description

The SPT205 is a wideband overdrive-protected operational amplifier designed for applications needing both speed and low power operation. Utilizing a well-established current feedback architecture, the SPT205 exhibits performance far beyond that of conventional voltage feedback op amps. For example, the SPT205 has a bandwidth of 170MHz at a gain of +20 and settles to 0.1% in 22ns. Plus, the SPT205 has a combination of important features not found in other high-speed op amps.

For example, the SPT205 has been designed to consume little power – 570mW at ±15V supplies. The result is lower power supply requirements and less system-level heat dissipation. In addition, the device can be operated on supply voltages as low as ±5V for even lower power dissipation.

Complete overdrive protection has been designed into the part. This is critical for applications, such as ATE and instrumentation, which require protection from signal levels high enough to cause saturation of the amplifier. This feature allows the output of the op amp to be protected against short circuits using techniques developed for low-speed op amps. With this capability, even the fastest signal sources can feature effective short circuit protection.

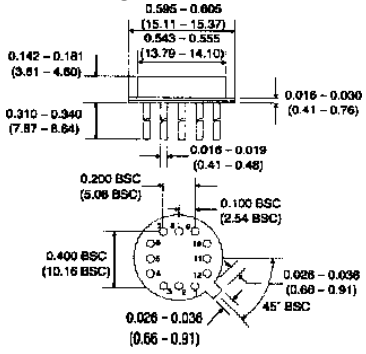
The SPT205 is constructed using thin film resistor/bipolar transistor technology, and is available in the following versions:

SPT205AIH -25 to +85 °C 12-pin TO-8 can
SPT205AMH -55 to +125 °C 12-pin TO-8 can, features burn-in and hermetic testing

Typical Performance

	Gain Setting						
Parameter	+7	+20	+50	-1	-20	-50	**Units**
Bandwidth (-3 dB)	220	170	80	220	130	80	MHz
Rise time	1.7	2.2	4.7	1.7	2.9	4.7	ns
Slew Rate	2.4	2.4	2.4	2.4	2.4	2.4	V/ns
Settling Time (to 0.1%)	22	22	20	21	20	19	ns

Package Dimensions



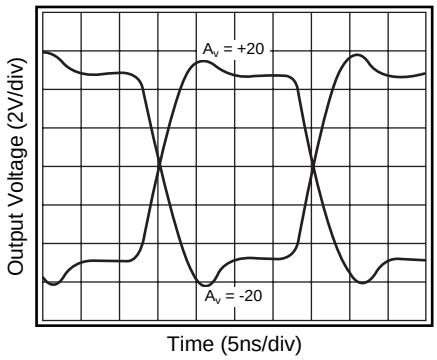
Features

- -3dB bandwidth of 170MHz
- 0.1% settling in 22ns
- Complete overdrive protection
- Low power: 570mW (190mW at ±5V)
- 3MΩ input resistance
- Output may be current limited
- Direct replacement for CLC205

Applications

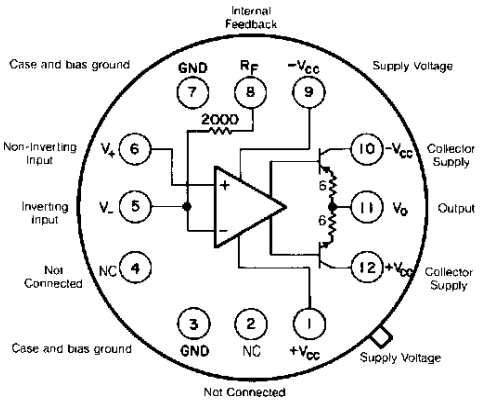
- Fast, precision A/D conversion
- Automatic test equipment
- Input/output amplifiers
- Photodiode, CCD preamps
- IF processors
- High-speed modems, radios
- Line drivers

Large Signal Pulse Response



205 Plot8

Bottom View



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SPT205 Electrical Characteristics (A_v = +20V, V_{CC} = ±15V, R_L = 200Ω, R_f = 2kΩ; unless specified)

PARAMETERS	CONDITIONS	TYP	MIN & MAX RATINGS			UNITS	SYM
Ambient Temperature	SPT205AIH	+25°C	-25°C	+25°C	+85°C		
Ambient Temperature	SPT205AMH	+25°C	-25°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
† -3dB bandwidth	V_o = <2V_{pp}	170	>140	>140	>125	MHz	SSBW
large-signal bandwidth	V_o = <10V_{pp}	100	>72	>80	>80	MHz	FPBW
gain flatness	V_o = <2V_{pp}						
† peaking	0.1 to 35MHz	0	<0.3	<0.3	<0.5	dB	GFPL
† peaking	>35MHz	0	<0.5	<0.5	<0.8	dB	GFPH
† rolloff	at 70MHz	–	<0.8	<0.8	<0.8	dB	GFR
group delay	to 70MHz	3.0 ± .2	–	–	–	ns	GD
linear phase deviation	to 70MHz	0.8	<3.0	<2.0	<3.0	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.2	<2.6	<2.6	<3.0	ns	TRS
	10V step	4.8	<5.5	<5.5	<5.5	ns	TRL
settling time to 0.1%	10V step, note 2	22	<27	<27	<27	ns	TS
to 0.05%	10V step, note 2	24	<30	<30	<30	ns	TSP
overshoot	5V step	7	<14	<14	<14	%	OS
slew rate	20V_{pp} at 50MHz	2.4	>1.8	>2.0	>2.0	V/ns	SR
NOISE AND DISTORTION RESPONSE							
† 2nd harmonic distortion	2V_{pp}, 20MHz	-57	<-50	<-50	<-50	dBc	HD2
† 3rd harmonic distortion	2V_{pp}, 20MHz	-68	<-55	<-55	<-55	dBc	HD3
equivalent input noise							
voltage	>100kHz	2.1	<3.0	<3.0	<3.5	nV/√Hz	VN
inverting current	>100kHz	22	<30	<30	<35	pA/√Hz	ICN
non-inverting current	>100kHz	4.8	<6.5	<6.5	<7.5	pA/√Hz	NCN
noise floor	>100kHz	-157	<-154	<-154	<-153	dBm(1Hz)	SNF
integrated noise	1kHz to 150MHz	39	<55	<55	<61	µV	INV
noise floor	>5MHz	-157	<-154	<-154	<-153	dBm(1Hz)	SNF
integrated noise	5MHz to 150MHz	39	<55	<55	<61	µV	INV
STATIC, DC PERFORMANCE							
* input offset voltage		3.5	<8.0	<8.0	<11.0	mV	VIO
average temperature coefficient		11	<25	<25	<25	µV/°C	DVIO
* input bias current	non-inverting	3.0	<25	<15	<15	µA	IBN
average temperature coefficient		15	<100	<100	<100	nA/°C	DIBN
* input bias current	inverting	2.0	<22	<10	<25	µA	IBI
average temperature coefficient		20	<150	<150	<150	nA/°C	DIBI
* power supply rejection ratio		69	>55	>55	>55	dB	PSRR
common mode rejection ratio		60	>50	>50	>50	dB	CMRR
* supply current	no load	19	<20	<20	<22	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance	DC	3.0	>1.0	>1.0	>1.0	MΩ	RIN
non-inverting input capacitance	70MHz	5.0	<7.0	<7.0	<7.0	pF	CIN
output impedance	DC	–	<0.1	<0.1	<0.1	Ω	RO
output voltage range	no load	±12	>±11	>±11	>±11	V	VO
internal feedback resistor							
absolute tolerance		–	–	<0.2	–	%	RFA
temperature coefficient		–	–	-100 ±40	–	ppm/°C	RFTC
inverting input current self limit		2.2	<3.0	<3.0	<3.2	mA	ICL

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

V_{CC}	±20V
I_o	±75mA
common mode input voltage	±(|V_{CC}| -1)V
differential input voltage	±3V
thermal resistance	(see thermal model)
operating temperature	AI: -25°C to +85°C
	AM: -55°C to +125°C
storage temperature	-65°C to +150°C
lead temperature (soldering 10s)	+300°C

Recommended Operating Conditions

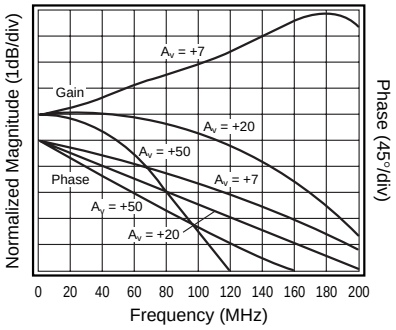
V_{CC}	±5V to ±15V
I_o	±50mA
common mode input voltage	±(|V_{CC}| -5)V
gain range	+7 to +50, -1 to -50

note 1: * AI, AM 100% tested at +25°C
† AM 100% tested at +25°C and sample tested at -55°C and +125°C
† AI sample tested at +25°C

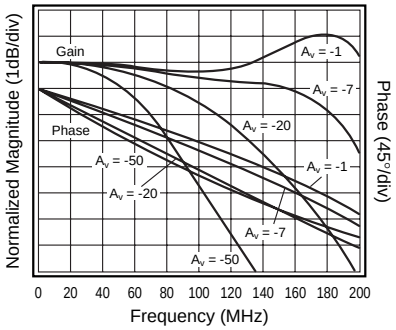
note 2: Settling time specifications require the use of an external feedback resistor (2Ω)

SPT205 Typical Performance Characteristics (T_A = +25°C, A_V = +20, V_{CC} = ±15V, R_L = 200Ω; unless specified)

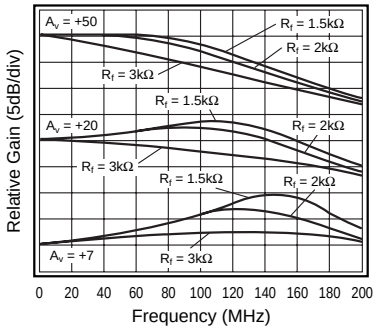
Non-Inverting Frequency Response



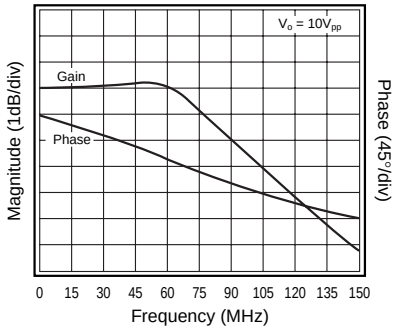
Inverting Frequency Response



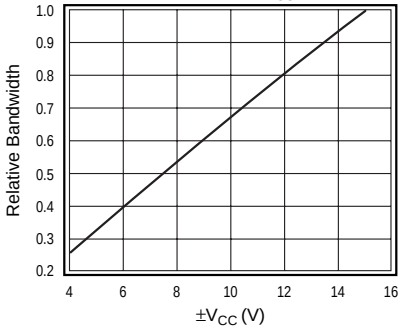
Frequency Response vs. External R_f



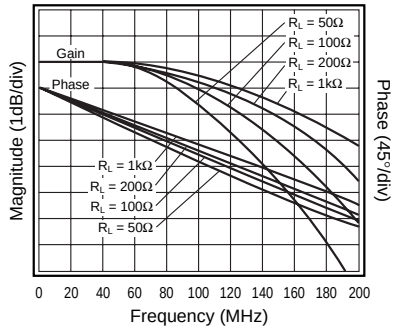
Large Signal Gain and Phase



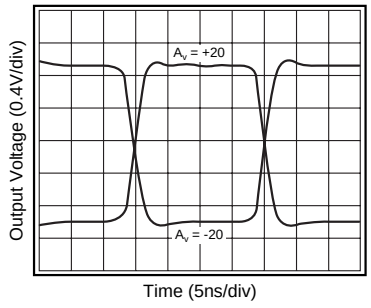
Relative Bandwidth vs. V_{CC}



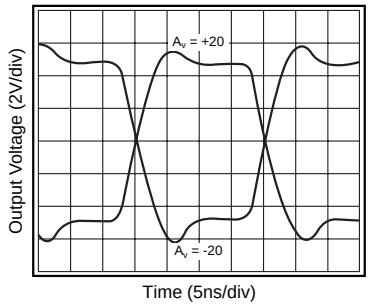
Gain and Phase for Various Loads



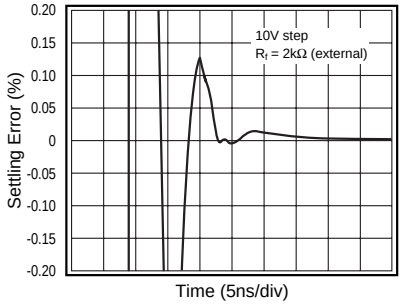
Small Signal Pulse Response



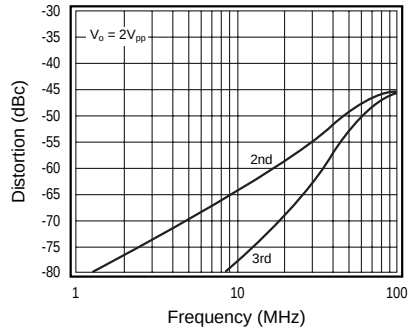
Large Signal Pulse Response



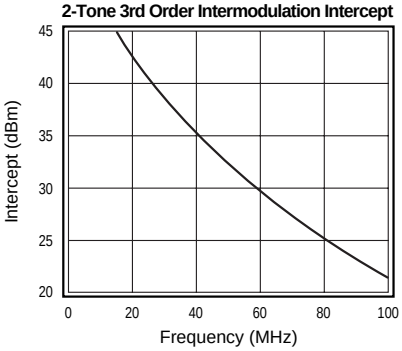
Settling Time



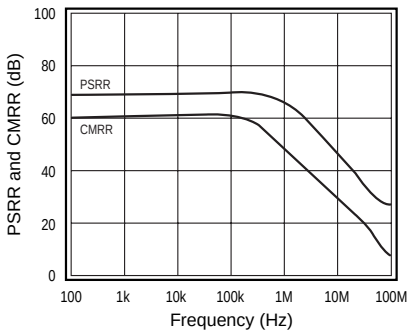
2nd and 3rd Harmonic Distortion



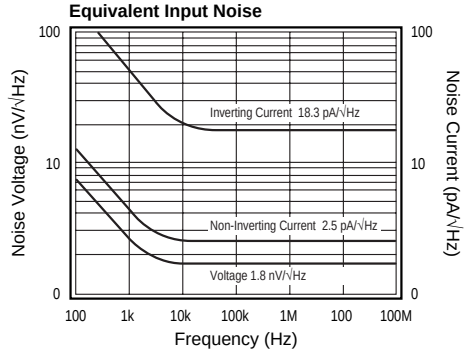
2-Tone 3rd Order Intermodulation Intercept



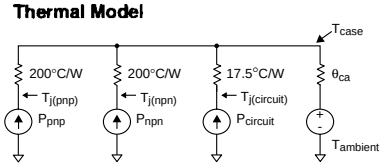
CMRR and PSRR



Equivalent Input Noise



Thermal Model



$P_{circuit} = [(+V_{CC}) - (-V_{CC})]^2 / 1.77k\Omega$

$P_{xxx} = [(\pm V_{CC}) - V_{out} - (I_{col}) (R_{col} + 6)] (I_{col})$ (% duty cycle)

(For positive V_o and V_{CC}, this is the power in the npn output stage.)

(For negative V_o and V_{CC}, this is the power in the pnp output stage.)

θ_{ca} = 65°C/W in still air without a heatsink.
35°C/W in still air without a Thermalloy 2268.
15°C/W in 300ft/min air with a Thermalloy 2268
(Thermalloy 2240 works equally well.)

$I_{col} = V_{out}/R_{load}$ or 3mA, whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33Ω recommended) between the xxx collector and $\pm V_{CC}$.

$T_{J\,(pnp)} = P_{pnp}\,(200 + \theta_{ca}) + (P_{ckt} + P_{npn})\theta_{ca} + T_a$, similar for $T_{J\,(npn)}$.

$T_{J\,(ckt)} = P_{ckt}\,(17.5 + \theta_{ca}) + (P_{pnp} + P_{npn})\theta_{ca} + T_a$.

Current Feedback Amplifiers

Some of the key features of current feedback technology are:

- Independence of AC bandwidth and voltage gain
- Adjustable frequency response with feedback resistor
- High slew rate
- Fast settling

Current feedback operation can be described using a simple equation. The voltage gain for a non-inverting or inverting current feedback amplifier is approximated by Equation 1.

$$\frac{V_o}{V_{in}} = \frac{A_v}{1+\frac{R_f}{Z(j\omega)}} \qquad \text{Equation 1}$$

where:

- A_v is the closed loop DC voltage gain
- R_f is the feedback resistor
- $Z(j\omega)$ is the SPT205's open loop transimpedance gain
- $\frac{Z(j\omega)}{R_f}$ is the loop gain

The denominator of Equation 1 is approximately equal to 1 at low frequencies. Near the -3dB corner frequency, the interaction between R_f and $Z(j\omega)$ dominates the circuit performance. The value of the feedback resistor has a large affect on the circuits performance. Increasing R_f has the following affects:

- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot
- Affects frequency response phase linearity

Overdrive Protection

Unlike most other high-speed op amps, the SPT205 is not damaged by saturation caused by overdriving input signals (where V_{in} x gain > max. V_o). The SPT205 self limits the current at the inverting input when the output is saturated (see the inverting input current self limit specification); this ensures that the amplifier will not be damaged due to excessive internal currents during overdrive. For protection against input signals which would exceed either the maximum differential or common mode input voltage, the diode clamp circuits below may be used.

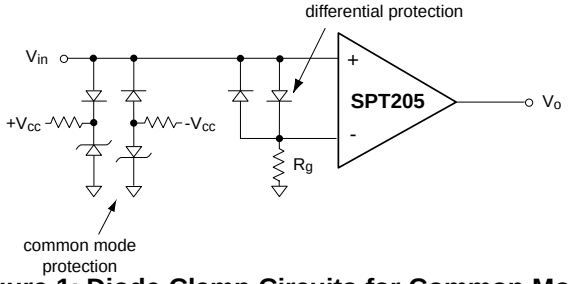


Figure 1: Diode Clamp Circuits for Common Mode and Differential Mode Protection

Short Circuit Protection

Damage caused by short circuits at the output may be prevented by limiting the output current to safe levels. The most simple current limit circuit calls for placing resistors between the output stage collector supplies and the output stage collectors (pins 12 and 10). The value of this resistor is determined by:

$$R_C = \frac{V_C}{I_l} - R_l$$

where I_l is the desired limit current and R_l is the minimum expected load resistance (0Ω for a short to ground). Bypass capacitors of 0.01µF on should be used on the collectors as in Figures 2 and 3.

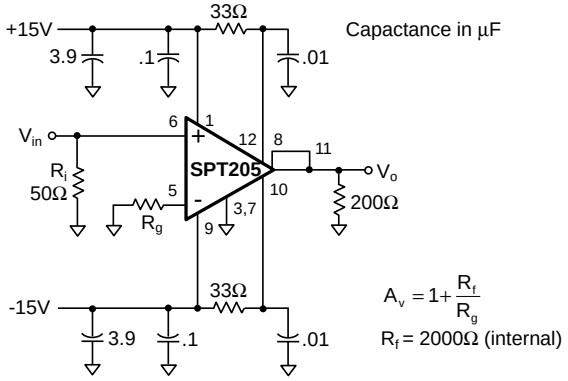


Figure 2: Recommended Non-Inverting Gain Circuit

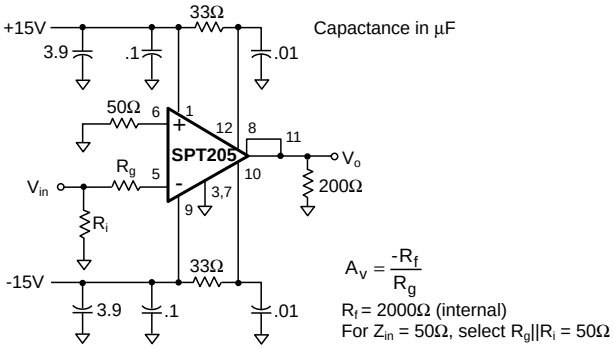


Figure 3: Recommended Inverting Gain Circuit

A more sophisticated current limit circuit which provides a limit current independent of R_l is shown in Figure 4 on page 5.

With the component values indicated, current limiting occurs at 50mA. For other values of current limit (I_l), select R_C to equal V_{be}/I_l. Where V_{be} is the base to emitter voltage drop of Q3 (or Q4) at a current of $[2V_{CC} - 1.4] / R_x$, where $R_x \leq [(2V_{CC} - 1.4) / I_l]$

B_{min}. Also, B_{min} is the minimum beta of Q1 (or Q2) at a current of I_l. Since the limit current depends on V_{be}, which is temperature dependent, the limit current is likewise temperature dependent.

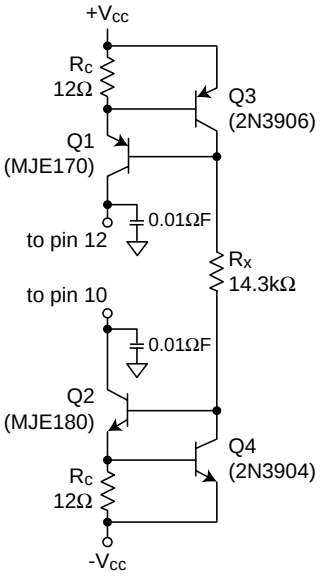


Figure 4: Active Current Limit Circuit (50mA)

Controlling Bandwidth and Passband Response

In most applications, a feedback resistor value of 2kΩ will provide optimum performance; nonetheless, some applications may require a resistor of some other value. The response versus R_f plot on the previous page shows how decreasing R_f will increase bandwidth (and frequency response peaking, which may lead to instability). Conversely, large values of feedback resistance tend to roll off the response.

The best settling time performance requires the use of an external feedback resistor (use of the internal resistor results in a 0.1% to 0.2% settling tail). The settling performance may be improved slightly by adding a capacitance of 0.4pF in parallel with the feedback resistor (settling time specifications reflect performance with an external feedback resistor but with no external capacitance).

Noise Analysis

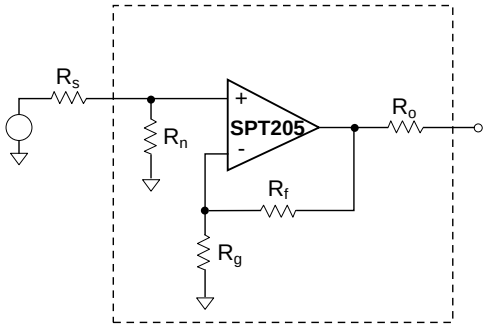
Approximate noise figure can be determined for the SPT205 using the ***Equivalent Input Noise*** plot on page 3 and the equations shown below.

$kT = 4.00 \times 10^{-21}$ Joules at 290°K

V_n is spot noise voltage (V/√Hz)

i_n is non-inverting spot noise current (A/√Hz)

i_i is inverting spot noise current (A/√Hz)



$$F = 10\log\left[1+\frac{R_s}{R_n}+\frac{R_s}{4kT}\cdot\left(i_n^2+\frac{V_n^2}{R_p^2}+\frac{R_f^2\,i_i^2}{R_p^2\,A_v^2}\right)\right]$$

$$\text{where } R_p = \frac{R_s\,R_n}{R_s+R_n};\quad A_v = \frac{R_f}{R_g}+1$$

Figure 5: Noise Figure Diagram and Equations (Noise Figure is for the Network Inside this Box.)

Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the SPT205 will improve stability and settling performance.

Transmission Line Matching

One method for matching the characteristic impedance (Z_o) of a transmission line or cable is to place the appropriate resistor at the input or output of the amplifier. Figure 6 shows typical inverting and non-inverting circuit configurations for matching transmission lines.

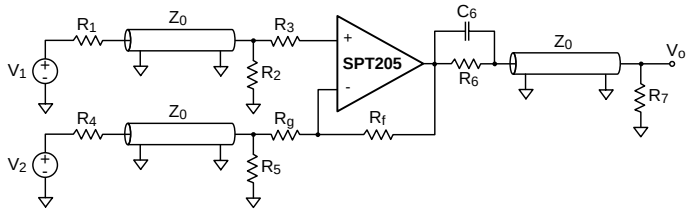


Figure 6: Transmission Line Matching

Non-inverting gain applications:

- Connect R_g directly to ground.
- Make R_1, R_2, R_6, and R_7 equal to Z_o.
- Use R_3 to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.

Inverting gain applications:

- Connect R_3 directly to ground.
- Make the resistors R_4, R_6, and R_7 equal to Z_o.
- Make R_5 II $R_g = Z_o$.

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use C_6 to match the output transmission line over a greater frequency range. C_6 compensates for the increase of the amplifier's output impedance with frequency.

Dynamic Range (Intermods)

For RF applications, the SPT205 specifies a third order intercept of 30dBm at 60MHz and P_o = 10dBm. A ***2-Tone, 3rd Order IMD Intercept*** plot is found in the ***Typical Performance Characteristics*** section. The output power level is taken at the load. Third-order harmonic distortion is calculated with the formula:

$$HD3^{rd} = 2 \cdot (IP3_o - P_o)$$

where:

- $IP3_o$ = third-order output intercept, dBm at the load.
- P_o = output power level, dBm at the load.
- $HD3^{rd}$ = third-order distortion from the fundamental, -dBc.
- dBm is the power in mW, at the load, expressed in dB.

Realized third-order output distortion is highly dependent upon the external circuit. Some of the common external circuit choices that improve 3^{rd} order distortion are:

- short and equal return paths from the load to the supplies.
- de-coupling capacitors of the correct value.
- higher load resistance.
- a lower ratio of the output swing to the power supply voltage.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance the performance of the SPT205. Good ground plane construction and power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal stray capacitance to the ground plane or other nodes. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

General layout and supply bypassing play major roles in high frequency performance. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF tantalum and 0.1µF ceramic capacitors on both supplies.
- Place the 6.8µF capacitors within 0.75 inches of the power pins.
- Place the 0.1µF capacitors less than 0.1 inches from the power pins.
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.

Evaluation PC boards (inverting and noninverting) for the SPT205 are available to aid in device testing.