SPT232

LOW DISTORTION WIDEBAND OP AMP

General Description

The SPT232 is a wideband low distortion operational amplifier designed specifically for high speed, low gain applications requiring wide dynamic range. Utilizing a current feedback architecture, the SPT232 offers high speed performance while maintaining DC precision.

The SPT232 offers precise gains from ±1 to ±5 with a true 0.1% linearity and provides stable, oscillation-free operation across the entire gain range without external compensation. The SPT232, a pin compatible enhanced version of the SPT231, reduces 2nd and 3rd harmonic distortion to an extremely low -69dBc at 20MHz ($2V_{pp}$, R_L = 100Ω). Additional features provided by the SPT232 include a small signal bandwidth of 270MHz, a large signal bandwidth of 95MHz and a 3000V/µs slew rate. The input offset voltage is typically 1mV with an input offset drift of 10µV/°C.

The SPT232 combines these high performance features with its 0.05% settling time of 15ns and its 100mA drive capability to provide high-speed, high-resolution A/D and D/A converter systems with an attractive solution for driving and buffering. Wide dynamic range systems such as radar and communication receivers requiring low harmonic distortion and low noise will find the SPT232 to be an excellent choice. As a linedriver, the SPT232 set at a gain of 2 cancels matched line losses.

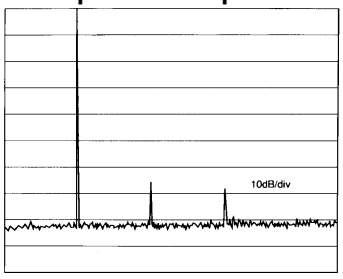
The SPT232 is constructed using thin film resistor/bipolar transistor technology, and is available in the following versions:

SPT232AIH	-25°C to +85°C	12-pin TO-8 can
SPT232AMH	-55°C to +125°C	12-pin TO-8 can, features burn-in and hermetic testing

Typical Performance

parameter	gain setting 1	2	5	−1	−2	−5	units
−3dB bandwidth	430	270	135	220	175	110	MHz
rise time (2V)	1.8	2.0	2.5	2.0	2.2	2.9	ns
slew rate	2.5	3	3	3	3	3	V/ns
settling time (to .1%)	12	12	12	12	12	15	ns

Spectral Response



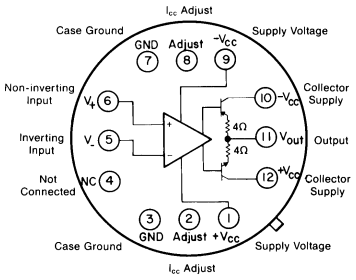
Features

- -69dBc 2nd and 3rd harmonics at 20MHz
- -3dB bandwidth of 270MHz
- 0.005% settling in 15ns
- 3000V/µs slew rate
- 1mV input offset voltage, 10µV/°C drift
- ±10V, 100mA max output
- Direct replacement for CLC232

Applications

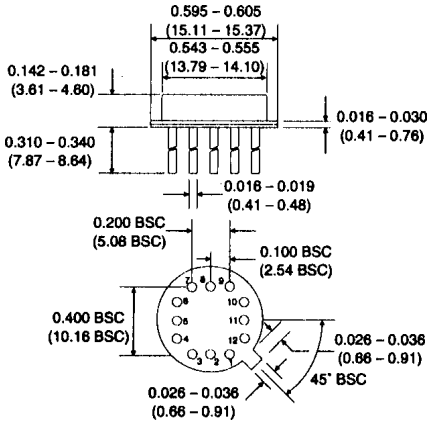
- Flash A/D drivers
- DAC current-to-voltage conversion
- Wide dynamic range IF amps
- VCO drivers
- DDS postamps
- Radar/communication receivers
- Precision line drivers

Bottom View



Pins 2 and 8 are used to adjust the supply current or to adjust the offset voltage (see text). These pins are normally left unconnected.

Package Dimensions



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SPT232 Electrical Characteristics (A_V = +2, V_{CC} = ±15V, R_L = 100Ω, R_f = 250Ω; unless specified)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS[1]			UNITS	SYMBOL
Ambient Temperature	SPT232AIH	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature	SPT232AMH	+25°C	−25°C	+25°C	+ 85°C		
FREQUENCY DOMAIN RESPONSE, note 2							
† −3dB bandwidth	V_{out}≤0.63V_{pp}	270	>200	>200	>200	MHz	SSBW1
	V_{out}≤2V_{pp}	165	>145	>145	>120	MHz	SSBW2
	V_{out}≤10V_{pp}	95	>80	>80	>60	MHz	LSBW
gain flatness	V_{out}≤0.63V_{pp}						
† peaking	0.1 to 50MHz	0.1	<0.6	<0.3	<0.6	dB	GFPL
† peaking	>50MHz	0.1	<1.5	<0.3	<0.8	dB	GFPH
† rolloff	at 100MHz	0.4	<0.6	<0.6	<1.0	dB	GFR
group delay	to 100MHz	3.5±.5	—	—	—	ns	GD
linear phase deviation	to 100MHz	0.5	<2.0	<2.0	<2.0	°	LPD
reverse isolation	to 100MHz						
non-inverting		53	>43	>43	>43	dB	RINI
inverting		36	>26	>26	>26	dB	RIIN
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.0	<2.4	<2.3	<2.7	ns	TRS
	10V step	5.0	<7.0	<6.5	<6.5	ns	TRL
settling time to 0.05%	5V step	15	—	—	—	ns	TS
to 0.1%	2.5V step	12	<22	<17	<22	ns	TSP
overshoot	5V step	5	<15	<10	<15	%	OS
slew rate		3000	>2500	>2500	>1800	V/μs	SR
overload recovery	<1% error						
<50ns pulse, 200% overdrive		120	—	—	—	ns	OR
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	$2V_{pp}$, 20MHz	−69	<−64	<−64	<−56	dBc	HD2
†3rd harmonic distortion	$2V_{pp}$, 20MHz	−69	<−64	<−64	<−64	dBc	HD3
equivalent noise input							
voltage	>100kHz	2.8	<3.2	<3.2	<3.5	nV/√Hz	VN
inverting current	>100kHz	20	<23	<23	<25	pA/√Hz	ICN
non-inverting current	>100kHz	2.3	<2.6	<2.6	<2.9	pA/√Hz	NCN
noise floor	>100kHz	−155	<−154	<−154	<−153	dBm_{1Hz}	SNF
integrated noise	1kHz to 200MHz	57	<64	<64	<72	μV	INV
integrated noise	5MHz to 200MHz	57	<64	<64	<72	μV	INV
STATIC DC PERFORMANCE							
*input offset voltage		1	<4.0	<2.0	<4.5	mV	VIO
temperature coefficient		10	<25	<25	<25	μV/°C	DVIO
*input bias current	non-inverting	5	<29	<21	<31	μA	IBN
temperature coefficient		50	<125	<125	<125	nA/°C	DIBN
*input bias current	inverting	10	<31	<15	<35	μA	IBI
temperature coefficient		125	<200	<200	<200	nA/°C	DIBI
*power supply rejection ratio		50	>45	>45	>45	dB	PSRR
common mode rejection ratio		46	>40	>40	>40	dB	CMRR
*supply current	no load	25	<27	<27	<29	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance		400	>100	>200	>400	kΩ	RIN
non-inverting input capacitance		1.3	<2.5	<2.5	<2.5	pF	CIN
output impedance	at 100MHz	5, 37	—	—	—	Ω, nH	ZO
output voltage range	no load	±12	>±11	>±11	>±11	V	VO

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

V_{CC}		±20V
I_{out}		±100mA
V_{CM}, V_{out}	$\|V_{CC}\|$>15V	±(30−$\|V_{CC}\|$)V
	$\|V_{CC}\|$≤15V	±$\|V_{CC}\|$V
differential input voltage		±3V
junction temperature		+175°C
operating temperature range	AIH:	−25°C to +85°C
	AMH:	−55°C to +125°C
Storage Temperature Range		−65°C to + 150°C
Lead Temperature (soldering 10s)		+300°C

Recommended Operating Conditions

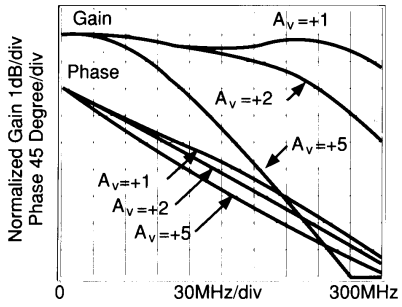
V_{CC}	±5V to ±15V
I_{out}	±75ma
V_{CM}	±($\|V_{CC}\|$−5)V
gain range	±1 to ±5

Note 1:
* AIH, AMH 100% tested at 25°C.
† AMH 100% tested at +25°C & sample tested at-55°C & +125°C
† AIH sample tested at +25°C.

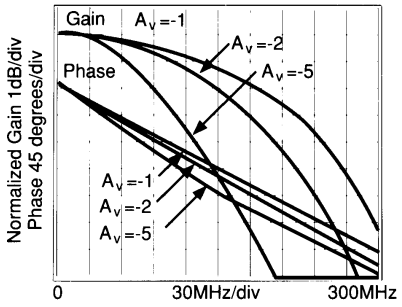
Note 2: The output amplitude used in testing is 0.63V_{pp}. Performance is guaranteed as listed above.

SPT232 Typical Performance Characteristics (T_A = 25°, A_V = +2, V_{CC} = ±15V, R_L = 100Ω, R_f = 250Ω)

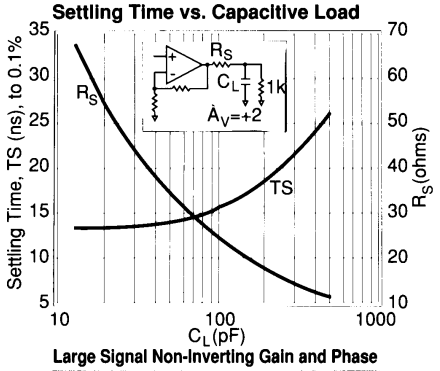
Non-Inverting Gain and Phase



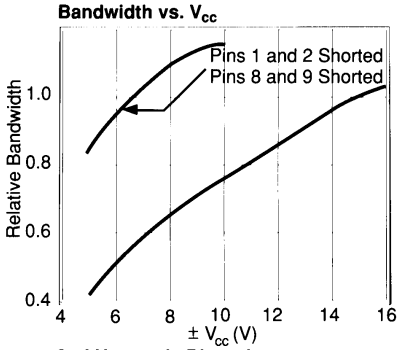
Inverting Gain and Phase



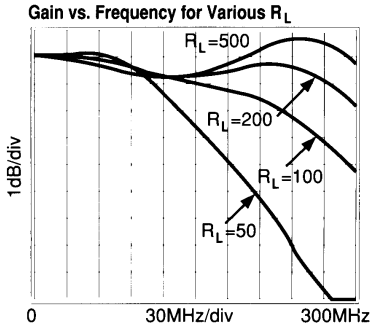
Settling Time vs. Capacitive Load



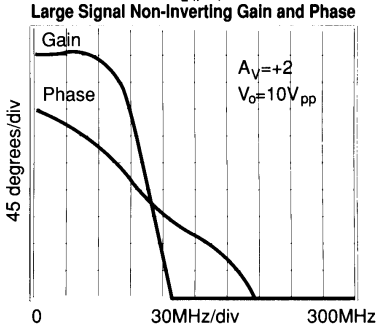
Bandwidth vs. V_{cc}



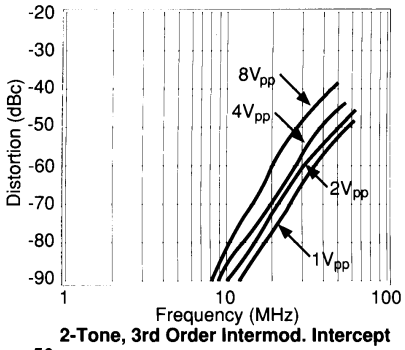
Gain vs. Frequency for Various R_L



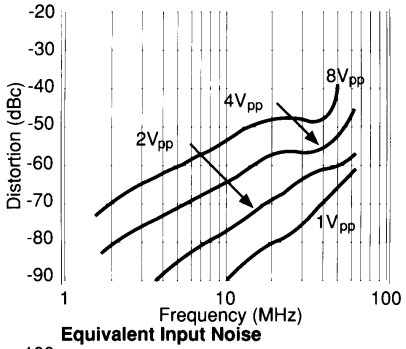
Large Signal Non-Inverting Gain and Phase



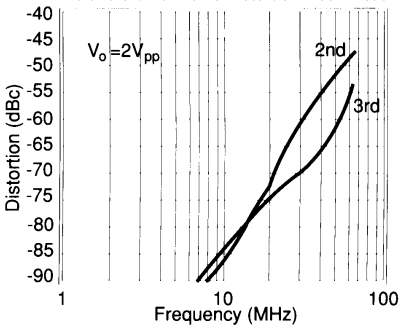
2nd Harmonic Distortion



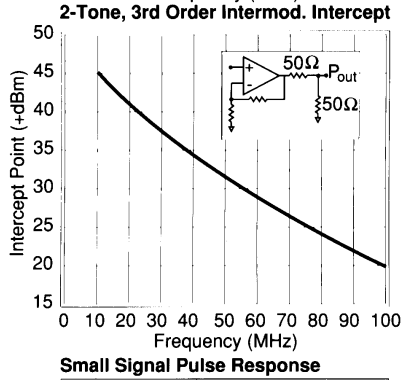
3rd Harmonic Distortion



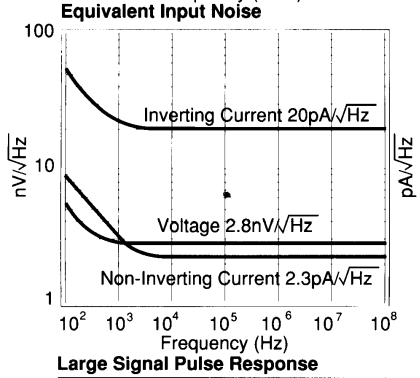
2nd and 3rd Harmonic Distortion: 200Ω Load



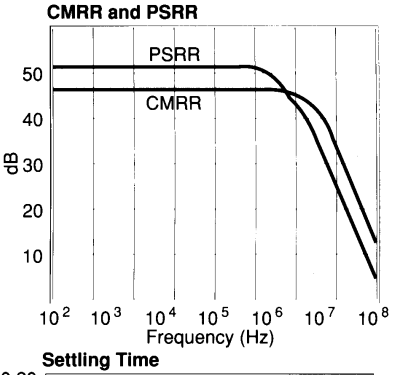
2-Tone, 3rd Order Intermod. Intercept



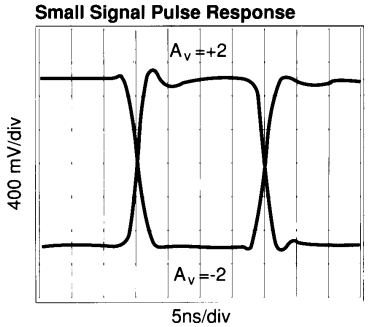
Equivalent Input Noise



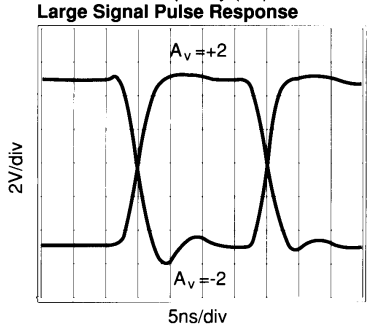
CMRR and PSRR



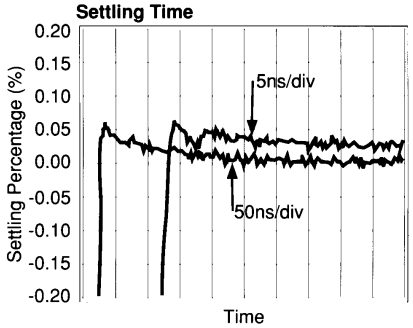
Small Signal Pulse Response



Large Signal Pulse Response



Settling Time



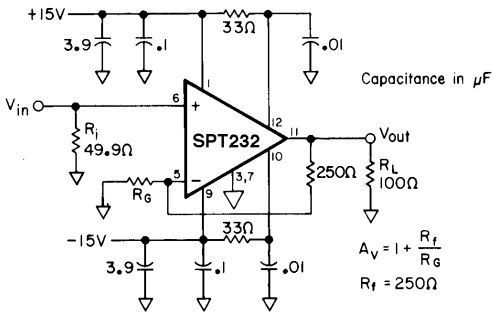


Figure 1: suggested non-inverting gain circuit

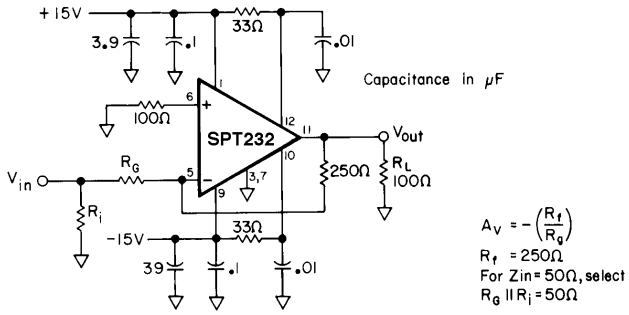


Figure 2: suggested inverting gain circuit

Operation

The SPT232 uses current feedback instead of the usual voltage feedback design topology.

The use of the SPT232 is basically the same as that of the conventional op amp (see the gain equations above). Since the device is designed specifically for low gain applications, the best performance is obtained when the circuit is used at gains between ±1 and ±5. Additionally, performance is optimum when a 250Ω feedback resistor is used.

Layout Considerations

To assure optimum performance the user should follow good layout practices which minimize the unwanted coupling of signals between nodes. During initial breadboarding of the circuit, use direct point to point wiring, keeping the lead lengths to less than .25". The use of solid, unbroken ground plane is helpful. Avoid wire-wrap type pc boards and methods. Sockets with small, short pin receptacles may be used with minimal performance degradation although their use is not recommended.

During pc board layout, keep all traces short and direct. The resistive body of R_g should be as close as possible to pin 5 to minimize capacitance at that point. For the same reason, remove ground plane from the vicinity of pins 5 and 6. In other areas, use as much ground plane as possible on one side of the board. It is especially important to provide a ground return path for current from the load resistor to the power supply bypass capacitors. Ceramic capacitors of .01 to .1μF (with short leads) should be less than .15 inches from pins 1 and 9. Larger tantalum capacitors should be placed within one inch of these pins. V_{cc} connections to pins 10 and 12 can be made directly from pins 9 and 1, but better supply rejection and settling time are obtained if they are separately bypassed as in Figures 1 and 2. To prevent signal distortion caused by reflections from impedance mismatches, use terminated microstrip or coaxial cable when the signal must traverse more than a few inches.

Since the pc board forms such an important part of the circuit, much time can be saved if prototype boards of any high frequency sections are built and tested early in the design phase. Evaluation boards designed for either inverting or non-inverting gains are available.

Thermal Considerations

At high ambient temperatures or large internal power dissipations, heat sinking is required to maintain acceptable junction temperatures. Use the thermal model on the previous page to determine junction temperatures. Many styles of heat sinks are available for TO-8 packages; the Thermalloy 2240 and 2268 are good examples. Some heat sinks are the radial fin type which cover the pc board and may interfere with external components. An excellent solution to this problem is to use surface mounted resistors and capacitors. They have a very low profile and actually improve high frequency performance. For use of these heat sinks with conventional components, a .1" high spacer can be inserted under the TO-8 package to allow sufficient clearance.

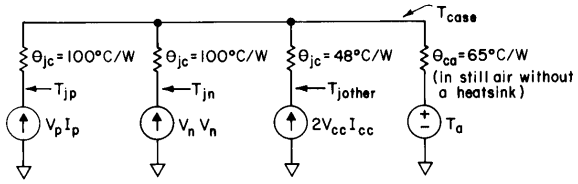
Low V_{cc} Operation: Supply Current Adjustment

The SPT232 is designed to operate on supplies as low as ±5V. In order to improve full bandwidth at reduced supply voltages, the supply current (I_{cc}) must be increased. The plot of Bandwidth vs V_{cc} shows the effect of shorting pins 1 and 2 and pins 8 and 9; this will increase both bandwidth and supply current. Care should be taken to not exceed the maximum junction temperatures; for this reason this technique should not be used with supplies exceeding ±10V. For intermediate values of V_{cc}, external resistors between pins 1 and 2 and pins 8 and 9 can be used.

Offset Voltage Adjustment

If trimming of the input offset voltage ($V_{os} = V_{ni} - V_{in}$) is desired, a resistor value of 10kΩ to 1MΩ placed between pins 8 and 9 will cause V_{os} to become more negative by 8mV to 0.2mV respectively. Similarly, a resistor placed between pins 1 and 2 will cause V_{os} to become more positive.

Thermal Model



$P_{circuit} = I_{cc}[(+V_{cc}) - (-V_{cc})]$ where I_{cc} = 14mA at ±15V

$P_{xxx} = [(\pm V_{cc}) - V_{out} - (I_{col})(R_{col} + 4)](I_{col})$ (%duty cycle)

(For positive V_o and V_{cc}, this is the power in the npn output stage.)

(For negative V_o and V_{cc}, this is the power in the pnp output stage.)

$I_{col} = V_{out}/R_{load}$ or 12mA, whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33Ω recommended) between the xxx collector and ±V_{cc}.

$T_{j\,(pnp)} = P_{pnp}(100 + \theta_{ca}) + (P_{cir} + P_{npn})\,\theta_{ca} + T_a$, similar for $T_{j\,(npn)}$.

$T_{j\,(cir)} = P_{cir}(48 + \theta_{ca}) + (P_{pnp} + P_{npn})\,\theta_{ca} + T_a$.

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