

Advance Information

LCD Segment / Common Driver with Controller CMOS

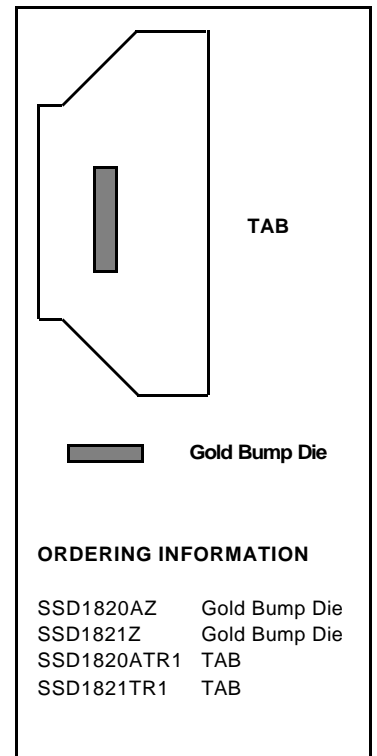
SSD1820A/21 is a single-chip CMOS LCD driver with controller for a liquid crystal dot-matrix graphic display system. SSD1820A consists of 194 high voltage driving output pins for driving 128 Segments, 64 Commons and 2 icon driving Commons, while SSD1821 consists of 210 high voltage driving output pins for driving 128 Segments, 80 Commons and 2 icon driving Commons.

SSD1820A/21 displays data directly from its internal 128x65/128x81 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through a hardware selectable 6800-/8080-series compatible Parallel Interface or 3/4 wires Serial Peripheral Interface.

SSD1820A/21 embeds a DC-DC Converter, a LCD Voltage Regulator, an On-Chip Bias Divider and an On-Chip Oscillator which reduce the number of external components. With the special design on minimizing power consumption and die/package layout, SSD1820A/21 is suitable for any portable battery-driven applications requiring a long operation period and a compact size.

- 128 x 64/80 Graphic Display with a Icon Line
- Programmable Multiplex ratio [16Mux - 65Mux/81Mux] (Partial Display)
- Single Supply Operation, 1.8 V - 3.3V
- Low Current Sleep Mode(<1.0uA)
- On-Chip Voltage Generator / External Power Supply
- Software selectable 2X / 3X / 4X / 5X / 6X On-Chip DC-DC Converter
- On-Chip Oscillator
- Software Selectable On-Chip Bias Dividers
- Programmable 1/4, 1/5, 1/6, 1/7, 1/8, 1/9 and 1/10 bias ratio
- Maximum +15.0V LCD Driving Output Voltage
- Hardware pin selectable for 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, 3-wire Serial Peripheral Interface or 4-wire Serial Peripheral Interface
- On-Chip 128 x 65/81 Graphic Display Data RAM
- Re-mapping of Row and Column Drivers
- Vertical Scrolling
- Display Offset Control
- 64 Levels Internal Contrast Control
- External Contrast Control
- Maximum 17MHz SPI or 15MHz PPI operation
- Selectable LCD Driving Voltage Temperature Coefficients (2 settings)
- Available in Gold Bump Die and Standard TAB (Tape Automated Bonding) Package

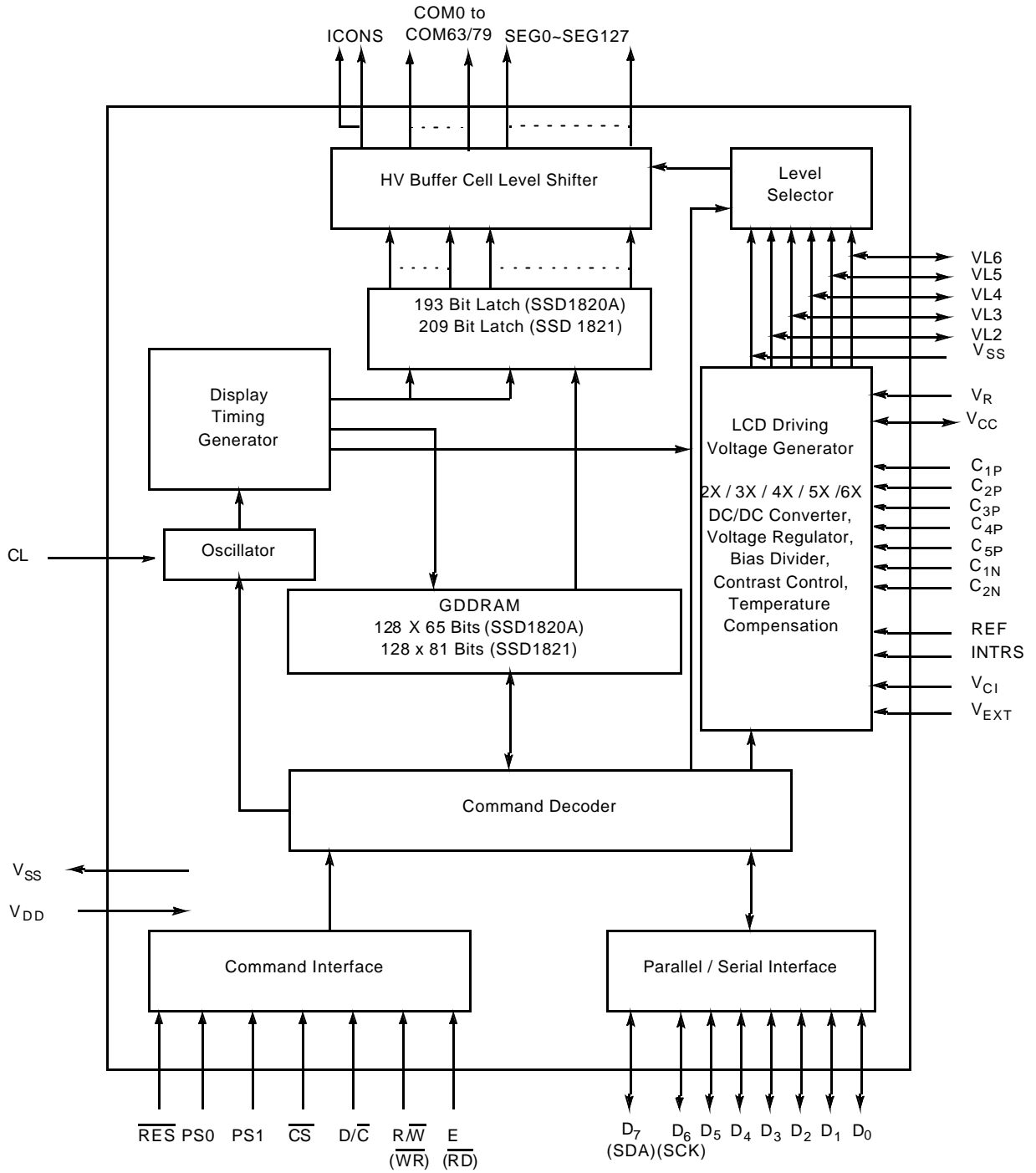
SSD1820A
SSD1821

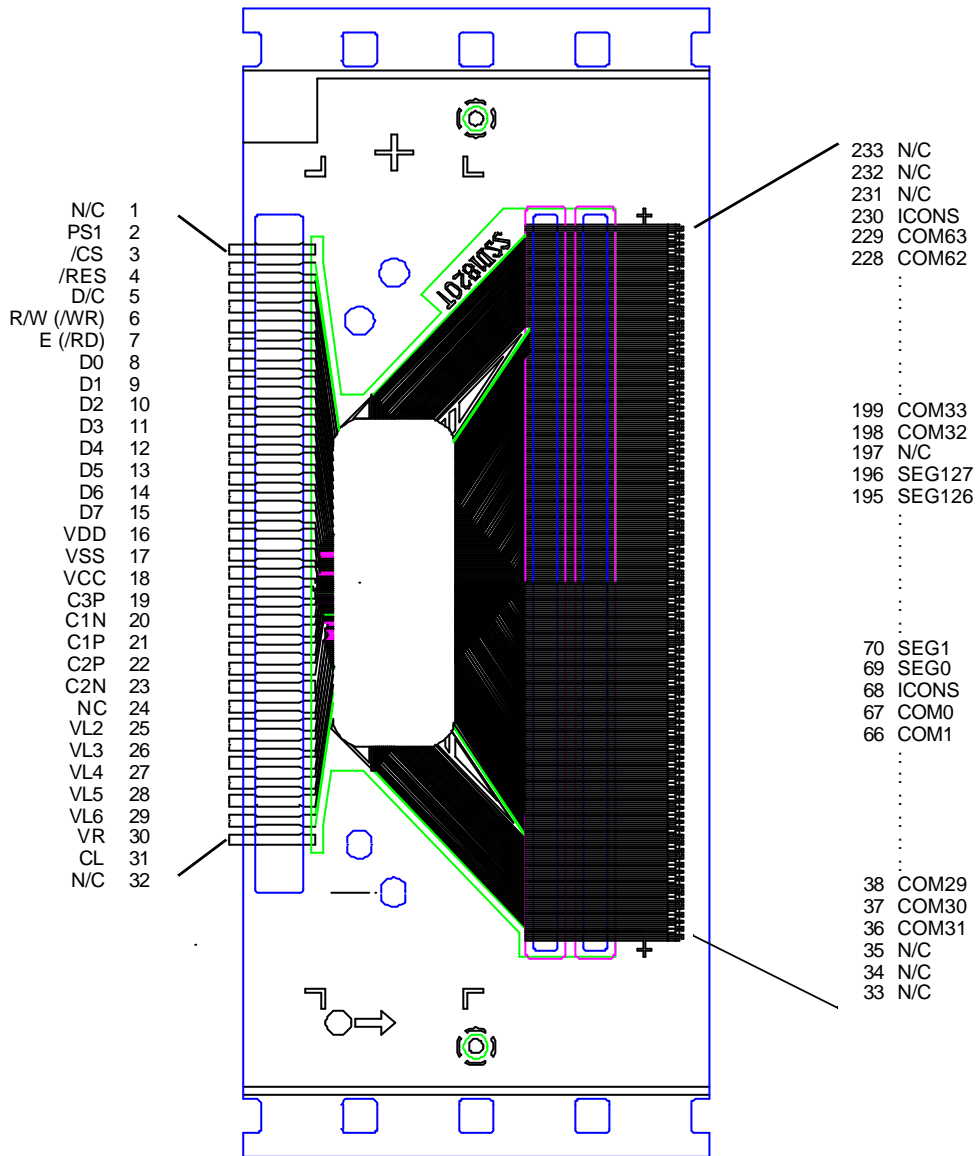


This document contains information on a new product. Specifications and information herein are subject to change without notice.



Block Diagram





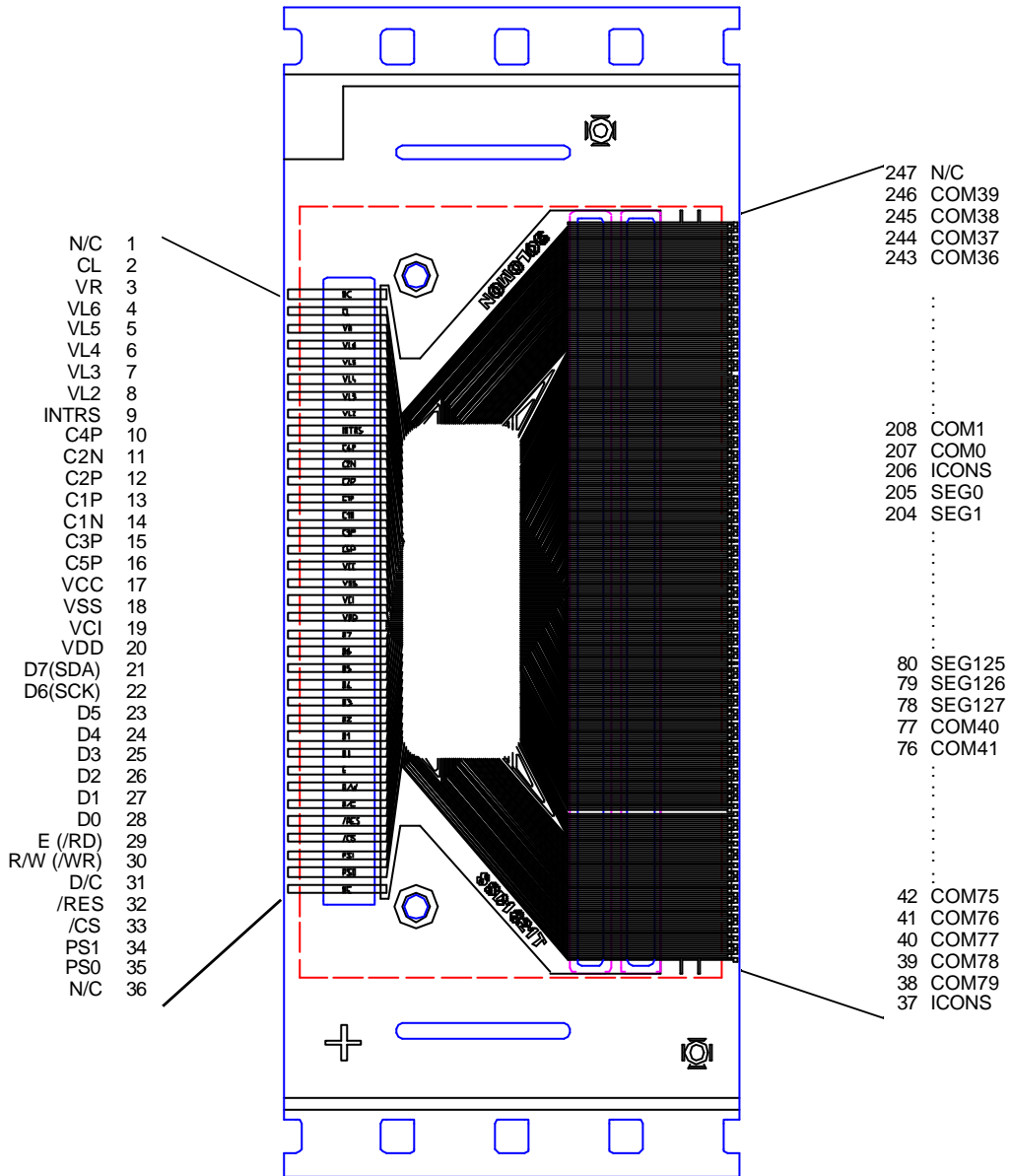
Note :

PS0, REF, INTRS and VCI are connected to VDD

Set condition:

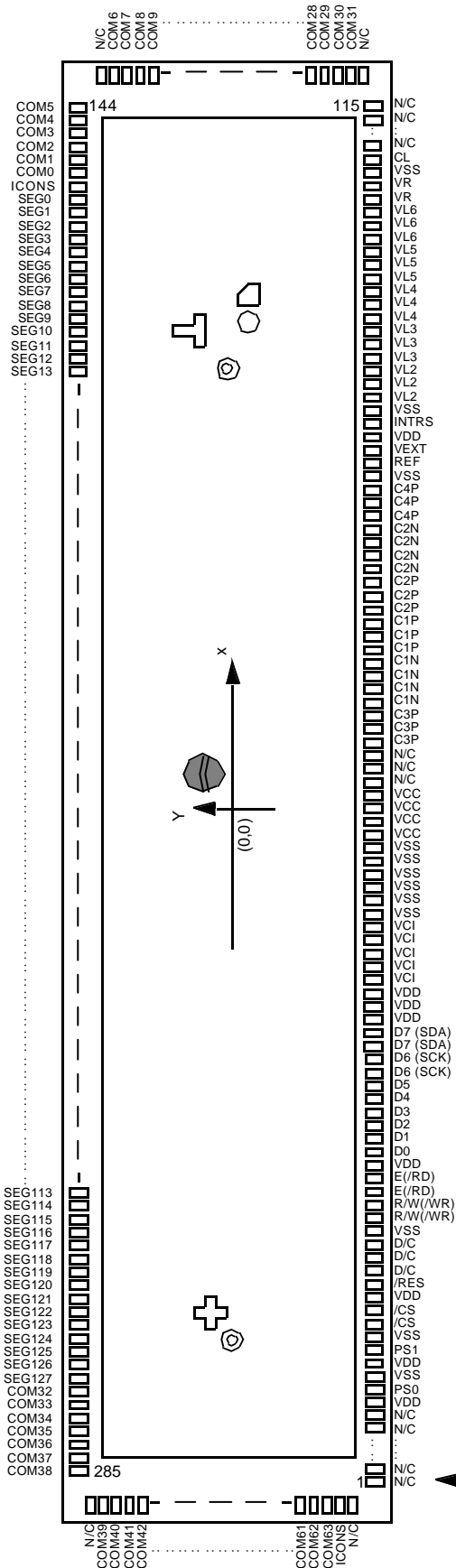
Parallel interface, internal reference voltage, internal voltage regulator and Booster reference voltage is VDD

**SSD1820AT Pin Assignment
(Copper View)**



Note :
REF connected to VDD

**SSD1821T Pin Assignment
(Copper View)**

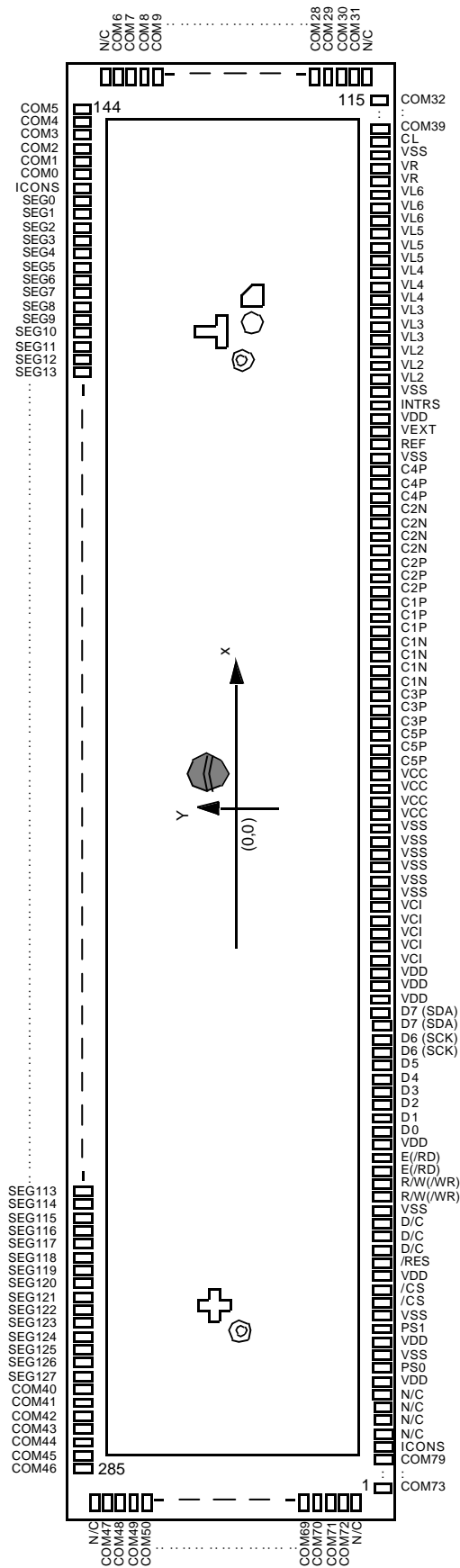


- Note:**
1. Diagram showing the face of the die.
 2. Coordinates are reference to center of the chip.
 3. Unit of coordinates and Size of all alignment marks are in μm .
 4. All alignment keys do not contain gold bump.

Die Size: 10.8mm x 1.96mm
 Die Thickness: 534 μm +/- 25 μm
 Bump Height: 18 μm +/- 3 μm

SSD1820AZ Die Pin Assignment

DRAWING NOT TO SCALE



Note:

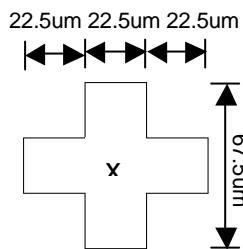
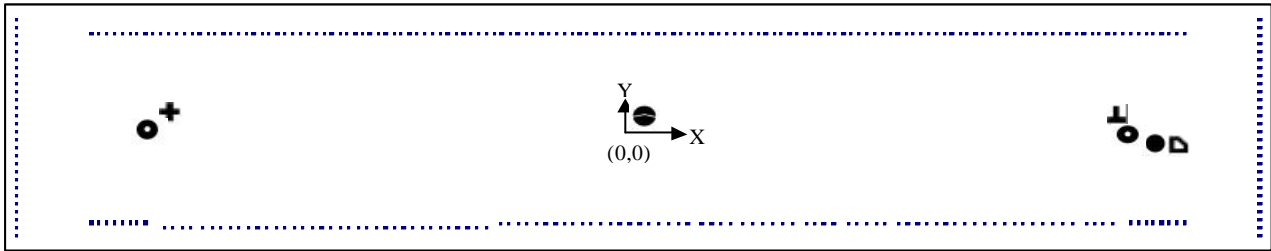
1. Diagram showing the face of the die.
2. Coordinates are reference to center of the chip.
3. Unit of coordinates and Size of all alignment marks are in um.
4. All alignment keys do not contain gold bump.

SSD1821Z Die Pin Assignment

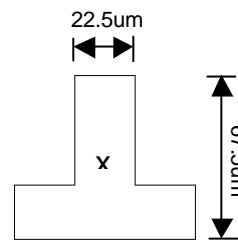
DRAWING NOT TO SCALE

Die Size: 10.8mm x 1.96mm
 Die Thickness: 534um +/- 25um
 Bump Height: 18um +/- 3um

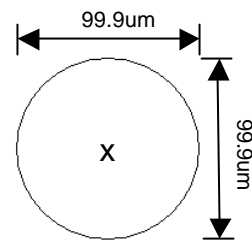
SSD1820AZ & SSD1821Z Alignment Key Position



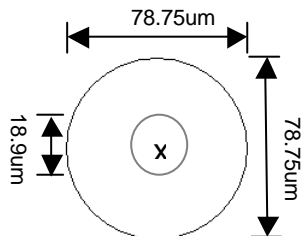
Center (-3926.1, 120)



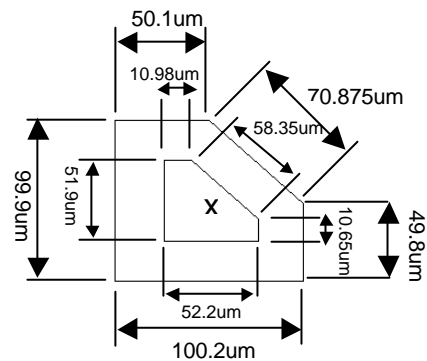
Center (3991.5, 120)



Center (4409.4, -147.9)



Center (-4095, -64.65)
Center (4263, -64.65)



Center (4515.6, -148.05)

Notes:

1. Diagram showing the gold bump view of the die.
2. Coordinates are reference to center of the chip
3. Unit of coordinates and Size of all alignment marks are in um.
4. All alignment keys do not contain gold bump.
5. 'X' represents the center point.
6. Drawing not to scale

SSD1820A/21Z Die Pad Coordinates

Pad#	SSD1820A	SSD1821	x-pos	y-pos	Pad#	SSD1820A	SSD1821	x-pos	y-pos	Pad#	SSD1820A	SSD1821	x-pos	y-pos	Pad#	SSD1820A	SSD1821	x-pos	y-pos
1	N/C	COM73	-4568.40	-773.40	116	N/C	N/C	5191.50	-874.80	144	COM5	COM5	4568.40	773.40	286	N/C	N/C	-5191.50	874.80
2	N/C	COM74	-4503.60	-773.40	117	COM31	COM31	5191.50	-810.00	145	COM4	COM4	4503.60	773.40	287	COM39	COM47	-5191.50	810.00
3	N/C	COM75	-4438.80	-773.40	118	COM30	COM30	5191.50	-745.20	146	COM3	COM3	4438.80	773.40	288	COM40	COM48	-5191.50	745.20
4	N/C	COM76	-4374.00	-773.40	119	COM29	COM29	5191.50	-680.40	147	COM2	COM2	4374.00	773.40	289	COM41	COM49	-5191.50	680.40
5	N/C	COM77	-4309.20	-773.40	120	COM28	COM28	5191.50	-615.60	148	COM1	COM1	4309.20	773.40	290	COM42	COM50	-5191.50	615.60
6	N/C	COM78	-4244.40	-773.40	121	COM27	COM27	5191.50	-550.80	149	COM0	COM0	4244.40	773.40	291	COM43	COM51	-5191.50	550.80
7	N/C	COM79	-4179.60	-773.40	122	COM26	COM26	5191.50	-486.00	150	ICONS	ICONS	4179.60	773.40	292	COM44	COM52	-5191.50	486.00
8	N/C	ICONS	-4114.80	-773.40	123	COM25	COM25	5191.50	-421.20	151	SEG0	SEG0	4114.80	773.40	293	COM45	COM53	-5191.50	421.20
9	NC	NC	-3964.80	-807.45	124	COM24	COM24	5191.50	-356.40	152	SEG1	SEG1	4050.00	773.40	294	COM46	COM54	-5191.50	356.40
10	NC	NC	-3887.40	-807.45	125	COM23	COM23	5191.50	-291.60	153	SEG2	SEG2	3985.20	773.40	295	COM47	COM55	-5191.50	291.60
11	NC	NC	-3810.00	-807.45	126	COM22	COM22	5191.50	-226.80	154	SEG3	SEG3	3920.40	773.40	296	COM48	COM56	-5191.50	226.80
12	NC	NC	-3732.60	-807.45	127	COM21	COM21	5191.50	-162.00	155	SEG4	SEG4	3855.60	773.40	297	COM49	COM57	-5191.50	162.00
13	VDD	VDD	-3634.28	-807.45	128	COM20	COM20	5191.50	-97.20	156	SEG5	SEG5	3790.80	773.40	298	COM50	COM58	-5191.50	97.20
14	PS0	PS0	-3558.08	-807.45	129	COM19	COM19	5191.50	-32.40	157	SEG6	SEG6	3726.00	773.40	299	COM51	COM59	-5191.50	32.40
15	VSS	VSS	-3481.88	-807.45	130	COM18	COM18	5191.50	32.40	158	SEG7	SEG7	3661.20	773.40	300	COM52	COM60	-5191.50	-32.40
16	VDD	VDD	-3405.68	-807.45	131	COM17	COM17	5191.50	97.20	159	SEG8	SEG8	3596.40	773.40	301	COM53	COM61	-5191.50	-97.20
17	PS1	PS1	-3329.48	-807.45	132	COM16	COM16	5191.50	162.00	160	SEG9	SEG9	3531.60	773.40	302	COM54	COM62	-5191.50	-162.00
18	VSS	VSS	-3253.28	-807.45	133	COM15	COM15	5191.50	226.80	161	SEG10	SEG10	3466.80	773.40	303	COM55	COM63	-5191.50	-226.80
19	/CS	/CS	-3177.08	-807.45	134	COM14	COM14	5191.50	291.60	162	SEG11	SEG11	3402.00	773.40	304	COM56	COM64	-5191.50	-291.60
20	/CS	/CS	-3100.88	-807.45	135	COM13	COM13	5191.50	356.40	163	SEG12	SEG12	3337.20	773.40	305	COM57	COM65	-5191.50	-356.40
21	VDD	VDD	-3024.68	-807.45	136	COM12	COM12	5191.50	421.20	164	SEG13	SEG13	3272.40	773.40	306	COM58	COM66	-5191.50	-421.20
22	/RES	/RES	-2948.48	-807.45	137	COM11	COM11	5191.50	486.00	165	SEG14	SEG14	3207.60	773.40	307	COM59	COM67	-5191.50	-486.00
23	D/C	D/C	-2872.28	-807.45	138	COM10	COM10	5191.50	550.80	166	SEG15	SEG15	3142.80	773.40	308	COM60	COM68	-5191.50	-550.80
24	D/C	D/C	-2796.08	-807.45	139	COM9	COM9	5191.50	615.60	167	SEG16	SEG16	3078.00	773.40	309	COM61	COM69	-5191.50	-615.60
25	D/C	D/C	-2719.88	-807.45	140	COM8	COM8	5191.50	680.40	168	SEG17	SEG17	3013.20	773.40	310	COM62	COM70	-5191.50	-680.40
26	VSS	VSS	-2643.68	-807.45	141	COM7	COM7	5191.50	745.20	169	SEG18	SEG18	2948.40	773.40	311	COM63	COM71	-5191.50	-745.20
27	R/W	R/W	-2567.48	-807.45	142	COM6	COM6	5191.50	810.00	170	SEG19	SEG19	2883.60	773.40	312	ICONS	COM72	-5191.50	-810.00
28	R/W	R/W	-2491.28	-807.45	143	N/C	N/C	5191.50	874.80	171	SEG20	SEG20	2818.80	773.40	313	N/C	N/C	-5191.50	-874.80
29	E	E	-2415.08	-807.45						172	SEG21	SEG21	2754.00	773.40					
30	E	E	-2338.88	-807.45						173	SEG22	SEG22	2689.20	773.40					
31	VDD	VDD	-2262.68	-807.45						174	SEG23	SEG23	2624.40	773.40					
32	D0	D0	-2186.48	-807.45						175	SEG24	SEG24	2559.60	773.40					
33	D1	D1	-2110.28	-807.45						176	SEG25	SEG25	2494.80	773.40					
34	D2	D2	-2034.08	-807.45						177	SEG26	SEG26	2430.00	773.40					
35	D3	D3	-1957.88	-807.45						178	SEG27	SEG27	2365.20	773.40					
36	D4	D4	-1881.68	-807.45						179	SEG28	SEG28	2300.40	773.40					
37	D5	D5	-1805.48	-807.45						180	SEG29	SEG29	2235.60	773.40					
38	D6	D6	-1729.28	-807.45						181	SEG30	SEG30	2170.80	773.40					
39	D6	D6	-1653.08	-807.45						182	SEG31	SEG31	2106.00	773.40					
40	D7	D7	-1576.88	-807.45						183	SEG32	SEG32	2041.20	773.40					
41	D7	D7	-1500.68	-807.45						184	SEG33	SEG33	1976.40	773.40					
42	VDD	VDD	-1424.48	-807.45						185	SEG34	SEG34	1911.60	773.40					
43	VDD	VDD	-1348.28	-807.45						186	SEG35	SEG35	1846.80	773.40					
44	VDD	VDD	-1272.08	-807.45						187	SEG36	SEG36	1782.00	773.40					
45	VCI	VCI	-1195.88	-780.75						188	SEG37	SEG37	1717.20	773.40					
46	VCI	VCI	-1119.68	-780.75						189	SEG38	SEG38	1652.40	773.40					
47	VCI	VCI	-1043.48	-780.75						190	SEG39	SEG39	1587.60	773.40					
48	VCI	VCI	-967.28	-780.75						191	SEG40	SEG40	1522.80	773.40					
49	VCI	VCI	-891.08	-780.75						192	SEG41	SEG41	1458.00	773.40					
50	VSS	VSS	-814.88	-780.75						193	SEG42	SEG42	1393.20	773.40					
51	VSS	VSS	-738.68	-780.75						194	SEG43	SEG43	1328.40	773.40					
52	VSS	VSS	-662.48	-780.75						195	SEG44	SEG44	1263.60	773.40					
53	VSS	VSS	-586.28	-780.75						196	SEG45	SEG45	1198.80	773.40					
54	VSS	VSS	-510.08	-780.75						197	SEG46	SEG46	1134.00	773.40					
55	VSS	VSS	-433.88	-780.75						198	SEG47	SEG47	1069.20	773.40					
56	VCC	VCC	-357.68	-780.75						199	SEG48	SEG48	1004.40	773.40					
57	VCC	VCC	-281.48	-780.75						200	SEG49	SEG49	939.60	773.40					
58	VCC	VCC	-205.28	-780.75						201	SEG50	SEG50	874.80	773.40					
59	VCC	VCC	-129.08	-780.75						202	SEG51	SEG51	810.00	773.40					
60	NC	C5P	13.50	-780.75						203	SEG52	SEG52	745.20	773.40					
61	NC	C5P	94.80	-780.75						204	SEG53	SEG53	680.40	773.40					
62	NC	C5P	176.10	-780.75						205	SEG54	SEG54	615.60	773.40					
63	C3P	C3P	257.40	-780.75						206	SEG55	SEG55	550.80	773.40					
64	C3P	C3P	338.70	-780.75						207	SEG56	SEG56	486.00	773.40					
65	C3P	C3P	420.00	-780.75						208	SEG57	SEG57	421.20	773.40					
66	C1N	C1N	536.70	-780.75						209	SEG58	SEG58	356.40	773.40					
67	C1N	C1N	612.90	-780.75						210	SEG59	SEG59	291.60	773.40					
68	C1N	C1N	689.10	-780.75						211	SEG60	SEG60	226.80	773.40					
69	C1N	C1N	765.30	-780.75						212	SEG61	SEG61	162.00	773.40					
70	C1P	C1P	841.50	-780.75						213	SEG62	SEG62	97.20	773.40					
71	C1P	C1P	917.70	-780.75						214	SEG63	SEG63	32.40	773.40					

SSD1820A/21Z Die Pad Coordinates

72	C1P	C1P	1044.60	-780.75
73	C2P	C2P	1125.90	-780.75
74	C2P	C2P	1207.20	-780.75
75	C2P	C2P	1288.50	-780.75
76	C2N	C2N	1405.20	-780.75
77	C2N	C2N	1481.40	-780.75
78	C2N	C2N	1557.60	-780.75
79	C2N	C2N	1633.80	-780.75
80	C4P	C4P	1750.50	-780.75
81	C4P	C4P	1831.80	-780.75
82	C4P	C4P	1913.10	-780.75
83	VSS	VSS	1989.30	-780.75
84	REF	REF	2065.50	-780.75
85	VEXT	VEXT	2182.20	-780.75
86	VDD	VDD	2258.40	-780.75
87	INTRS	INTRS	2334.60	-780.75
88	VSS	VSS	2410.80	-780.75
89	VL2	VL2	2487.00	-780.75
90	VL2	VL2	2568.30	-780.75
91	VL2	VL2	2649.60	-780.75
92	VL3	VL3	2730.90	-780.75
93	VL3	VL3	2812.20	-780.75
94	VL3	VL3	2893.50	-780.75
95	VL4	VL4	2974.80	-780.75
96	VL4	VL4	3056.10	-780.75
97	VL4	VL4	3137.40	-780.75
98	VL5	VL5	3218.70	-780.75
99	VL5	VL5	3300.00	-780.75
100	VL5	VL5	3381.30	-780.75
101	VL6	VL6	3462.60	-780.75
102	VL6	VL6	3543.90	-780.75
103	VL6	VL6	3625.20	-780.75
104	VR	VR	3741.90	-780.75
105	VR	VR	3818.10	-780.75
106	VSS	VSS	3894.30	-780.75
107	CL	CL	3970.50	-780.75
108	N/C	COM39	4114.80	-773.40
109	N/C	COM38	4179.60	-773.40
110	N/C	COM37	4244.40	-773.40
111	N/C	COM36	4309.20	-773.40
112	N/C	COM35	4374.00	-773.40
113	N/C	COM34	4438.80	-773.40
114	N/C	COM33	4503.60	-773.40
115	N/C	COM32	4568.40	-773.40

215	SEG64	SEG64	-32.40	773.40
216	SEG65	SEG65	-97.20	773.40
217	SEG66	SEG66	-162.00	773.40
218	SEG67	SEG67	-226.80	773.40
219	SEG68	SEG68	-291.60	773.40
220	SEG69	SEG69	-356.40	773.40
221	SEG70	SEG70	-421.20	773.40
222	SEG71	SEG71	-486.00	773.40
223	SEG72	SEG72	-550.80	773.40
224	SEG73	SEG73	-615.60	773.40
225	SEG74	SEG74	-680.40	773.40
226	SEG75	SEG75	-745.20	773.40
227	SEG76	SEG76	-810.00	773.40
228	SEG77	SEG77	-874.80	773.40
229	SEG78	SEG78	-939.60	773.40
230	SEG79	SEG79	-1004.40	773.40
231	SEG80	SEG80	-1069.20	773.40
232	SEG81	SEG81	-1134.00	773.40
233	SEG82	SEG82	-1198.80	773.40
234	SEG83	SEG83	-1263.60	773.40
235	SEG84	SEG84	-1328.40	773.40
236	SEG85	SEG85	-1393.20	773.40
237	SEG86	SEG86	-1458.00	773.40
238	SEG87	SEG87	-1522.80	773.40
239	SEG88	SEG88	-1587.60	773.40
240	SEG89	SEG89	-1652.40	773.40
241	SEG90	SEG90	-1717.20	773.40
242	SEG91	SEG91	-1782.00	773.40
243	SEG92	SEG92	-1846.80	773.40
244	SEG93	SEG93	-1911.60	773.40
245	SEG94	SEG94	-1976.40	773.40
246	SEG95	SEG95	-2041.20	773.40
247	SEG96	SEG96	-2106.00	773.40
248	SEG97	SEG97	-2170.80	773.40
249	SEG98	SEG98	-2235.60	773.40
250	SEG99	SEG99	-2300.40	773.40
251	SEG100	SEG100	-2365.20	773.40
252	SEG101	SEG101	-2430.00	773.40
253	SEG102	SEG102	-2494.80	773.40
254	SEG103	SEG103	-2559.60	773.40
255	SEG104	SEG104	-2624.40	773.40
256	SEG105	SEG105	-2689.20	773.40
257	SEG106	SEG106	-2754.00	773.40
258	SEG107	SEG107	-2818.80	773.40
259	SEG108	SEG108	-2883.60	773.40
260	SEG109	SEG109	-2948.40	773.40
261	SEG110	SEG110	-3013.20	773.40
262	SEG111	SEG111	-3078.00	773.40
263	SEG112	SEG112	-3142.80	773.40
264	SEG113	SEG113	-3207.60	773.40
265	SEG114	SEG114	-3272.40	773.40
266	SEG115	SEG115	-3337.20	773.40
267	SEG116	SEG116	-3402.00	773.40
268	SEG117	SEG117	-3466.80	773.40
269	SEG118	SEG118	-3531.60	773.40
270	SEG119	SEG119	-3596.40	773.40
271	SEG120	SEG120	-3661.20	773.40
272	SEG121	SEG121	-3726.00	773.40
273	SEG122	SEG122	-3790.80	773.40
274	SEG123	SEG123	-3855.60	773.40
275	SEG124	SEG124	-3920.40	773.40
276	SEG125	SEG125	-3985.20	773.40
277	SEG126	SEG126	-4050.00	773.40
278	SEG127	SEG127	-4114.80	773.40
279	COM32	COM40	-4179.60	773.40
280	COM33	COM41	-4244.40	773.40
281	COM34	COM42	-4309.20	773.40
282	COM35	COM43	-4374.00	773.40
283	COM36	COM44	-4438.80	773.40
284	COM37	COM45	-4503.60	773.40
285	COM38	COM46	-4568.40	773.40



SSD1820A /21

Pad 1, 2, 3, > 115

Bump size :

- Pad 1-8, 108-115, 144-285: 45x75um
- Pad 9-107 : 52.2x60um
- Pad 116-143, 286-313: 75x45um
- Tolerance : +/- 3um

PIN DESCRIPTIONS

$\overline{\text{RES}}$

This pin is reset signal input. When the pin is low, initialization of the chip is executed.

PS0

This pin use together with PS1 to determine the interface protocol between the driver and MCU. Refer to PS1 pin descriptions for more details.

PS1

This pin use together with PS0 to determine the interface protocol between the driver and MCU according to the following table.

PS0	PS1	Interface
L	L	3-wire SPI (write only)
L	H	4-wire SPI (write only)
H	L	8080 parallel interface (read and write allowed)
H	H	6800 parallel interface (read and write allowed)

$\overline{\text{CS}}$

This pin is chip select input. The chip is enabled for display data/command transfer only when $\overline{\text{CS}}$ is low.

$\overline{\text{D/C}}$

This input pin is to identify display data/command cycle. When the pin is high, the data written to the driver will be written into display RAM. When the pin is low, the data will be interpret as command. This pin must be connected to V_{SS} when 3-lines SPI interface is used.

$\overline{\text{R/W(WR)}}$

This pin is microprocessor interface signal. When interfacing to an 6800-series microprocessor, the signal indicates read mode when high and write mode when low. When interfacing to an 8080-microprocessor, a data write operation is initiated when $\overline{\text{R/W(WR)}}$ is low and the chip is selected.

$\overline{\text{E(RD)}}$

This pin is microprocessor interface signal. When interfacing to an 6800-series microprocessor, a data operation is initiated when $\overline{\text{E(RD)}}$ is high and the chip is selected. When interfacing to an 8080-microprocessor, a data read operation is initiated when $\overline{\text{E(RD)}}$ is low and the chip is selected.

$\text{D}_0\text{-D}_7$

These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D_7 is the serial data input SDA and D_6 is the serial clock input SCK.

INTRS

This pin is an input pin to enable the internal resistors network for the voltage regulator when INTRS is high. When it is low, the external resistors R_1/R_2 should be connected to V_{L6} , V_R and V_{SS} .

REF

This pin is an input pin to enable the internal reference voltage used for the internal regulator. When it is high, an internal reference voltage source will be used. When it is low, an external reference voltage source must be provided in V_{EXT} pin if internal regulator is used.

V_{DD}

Power supply pin.

V_{SS}

Ground.

V_{CI}

Reference voltage input for internal DC-DC converter. The voltage of generated V_{CC} equals to the multiple factor (2X, 3X, 4X, 5X or 6X) times V_{CI} with respect to V_{SS} .

Note:

- 1.) voltage at this input pin must be larger than or equal to V_{DD} .
- 2.) 6X is available for SSD1821 only.

V_{CC}

This is the most positive voltage supply pin of the chip. It can be supplied externally or generated by the internal DC-DC converter.

When using internal DC-DC converter as generator, voltage at this pin is for internal reference only. It CANNOT be used for driving external circuitries.

C_{1P} , C_{2P} , C_{3P} , C_{4P} , C_{5P} , C_{1N} and C_{2N}

When internal DC-DC voltage converter is used, external capacitor(s) is/are connected among these pins.

V_{L6}

This pin is the most positive LCD driving voltage. It can be supplied externally or generated by the internal regulator.

V_R

This pin is an input of the internal voltage regulator. When the internal resistors network for the voltage regulator is disabled (INTRS is pulled low), external resistors should be connected between V_{SS} and V_R , and V_R and V_{L6} , respectively (see application circuit).

V_{EXT}

This pin is an input to provide an external voltage reference for the internal voltage regulator when REF pin is pulled low.

V_{L5}, V_{L4}, V_{L3} and V_{L2}

LCD driving voltages. They can be supplied externally or generated by the internal bias divider. They have the following relationship:

$$V_{L6} > V_{L5} > V_{L4} > V_{L3} > V_{L2} > V_{SS}$$

	1:a bias
V _{L5}	(a-1)/a*V _{L6}
V _{L4}	(a-2)/a*V _{L6}
V _{L3}	2/a*V _{L6}
V _{L2}	1/a*V _{L6}

For SSD1820A, a equals to 9 at POR.

For SSD1821, a equal to 10 at POR.

COM0 - COM63/COM79

These pins provide the row driving signal COM0 - COM63/COM79 to the LCD panel. See Table 1 or 2 about the COM signal mapping in different multiplex ratio N.

ICONS

This pin is the special icons line COM signal output.

SEG0 - SEG127

These pins provide the LCD column driving signal. Their voltage level is V_{SS} during sleep mode and standby mode.

CL

This pin is the external clock input for the device which is enabled by using an extended command. Under normal operation, this pin should be left opened and internal oscillator will be used after power on reset.

N/C

These No Connection pins should NOT be connected to any signal pins nor shorted together. They should be left open.

OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

Description of Block Diagram Module

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the $\overline{D/C}$ pin. If $\overline{D/C}$ is high, data is written to Graphic Display Data RAM (GDDRAM). If $\overline{D/C}$ is low, the input at D_0 - D_7 is interpreted as a Command and it will be decoded and written to the corresponding command register.

Reset is of the same function as Power ON Reset (POR). Once \overline{RES} receives a negative reset pulse of about 1 μ s, all internal circuitry will be back to its initial status. Refer to Command Description section for more information.

MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D_0 - D_7), R/\overline{W} (\overline{WR}), $\overline{D/C}$, \overline{E} (\overline{RD}) and \overline{CS} . R/\overline{W} (\overline{WR}) input High indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. R/\overline{W} (\overline{WR}) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of $\overline{D/C}$ input. The \overline{E} (\overline{RD}) and \overline{CS} input serves as data latch signal (clock) when they are high and low respectively. Refer to Figure 1 of parallel timing characteristics for Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 4 below.

MPU Parallel 8080-series interface

The parallel interface consists of 8 bi-directional data pins (D_0 - D_7), R/\overline{W} (\overline{WR}), \overline{E} (\overline{RD}), $\overline{D/C}$ and \overline{CS} . The \overline{CS} input serves as data latch signal (clock) when it is low. Whether it is display data or status register read is controlled by $\overline{D/C}$. R/\overline{W} (\overline{WR}) and \overline{E} (\overline{RD}) input indicates a write or read cycle when \overline{CS} is low. Refer to Figure 2 of parallel timing characteristics for Parallel Interface Timing Diagram of 8080-series microprocessor.

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

MPU Serial 4-wire Interface

The serial interface consists of serial clock SCK, serial data SDA, $\overline{D/C}$ and \overline{CS} . SDA is shifted into a 8-bit shift register on every rising edge of SCL in the order of D_7 , D_6 ,... D_0 . $\overline{D/C}$ is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock. No extra clock or command is required to end the transmission.

MPU Serial 3-wire Interface

Operation is similar to 4-wire serial interface while $\overline{D/C}$ is not been used. The Display Data Length instruction is used to indicate that a specified number display data byte (1-256) are to be transmitted. Next byte after the display data string is handled as a command.

It should be noted that if there is a signal glitch at SCK that causing an out of synchronization in the serial communication, a hardware reset pulse at \overline{RES} pin is required to initialize the chip for re-synchronization.

Modes of operation

	6800 parallel	8080 parallel	Serial
Data Read	Yes	Yes	No
Data Write	Yes	Yes	Yes
Command Read	Status only	Status only	No
Command Write	Yes	Yes	Yes

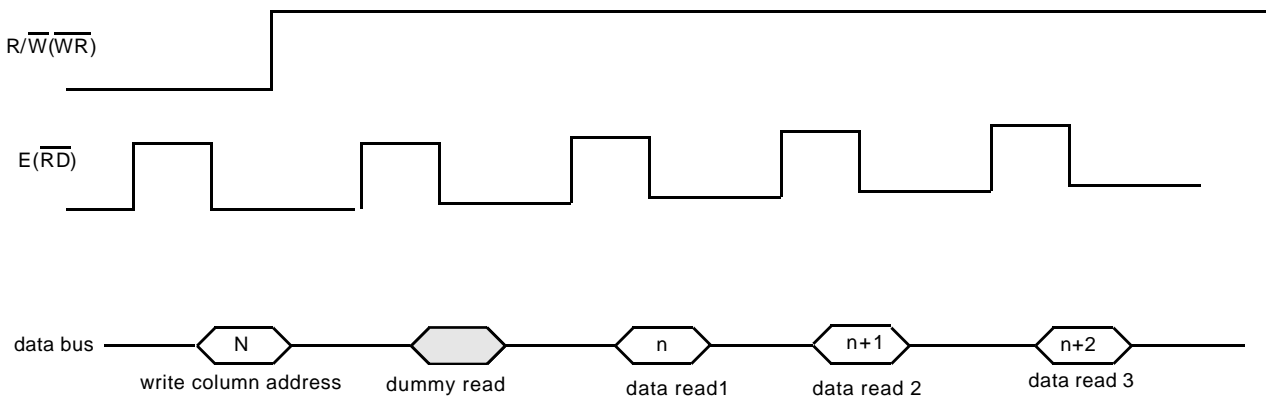
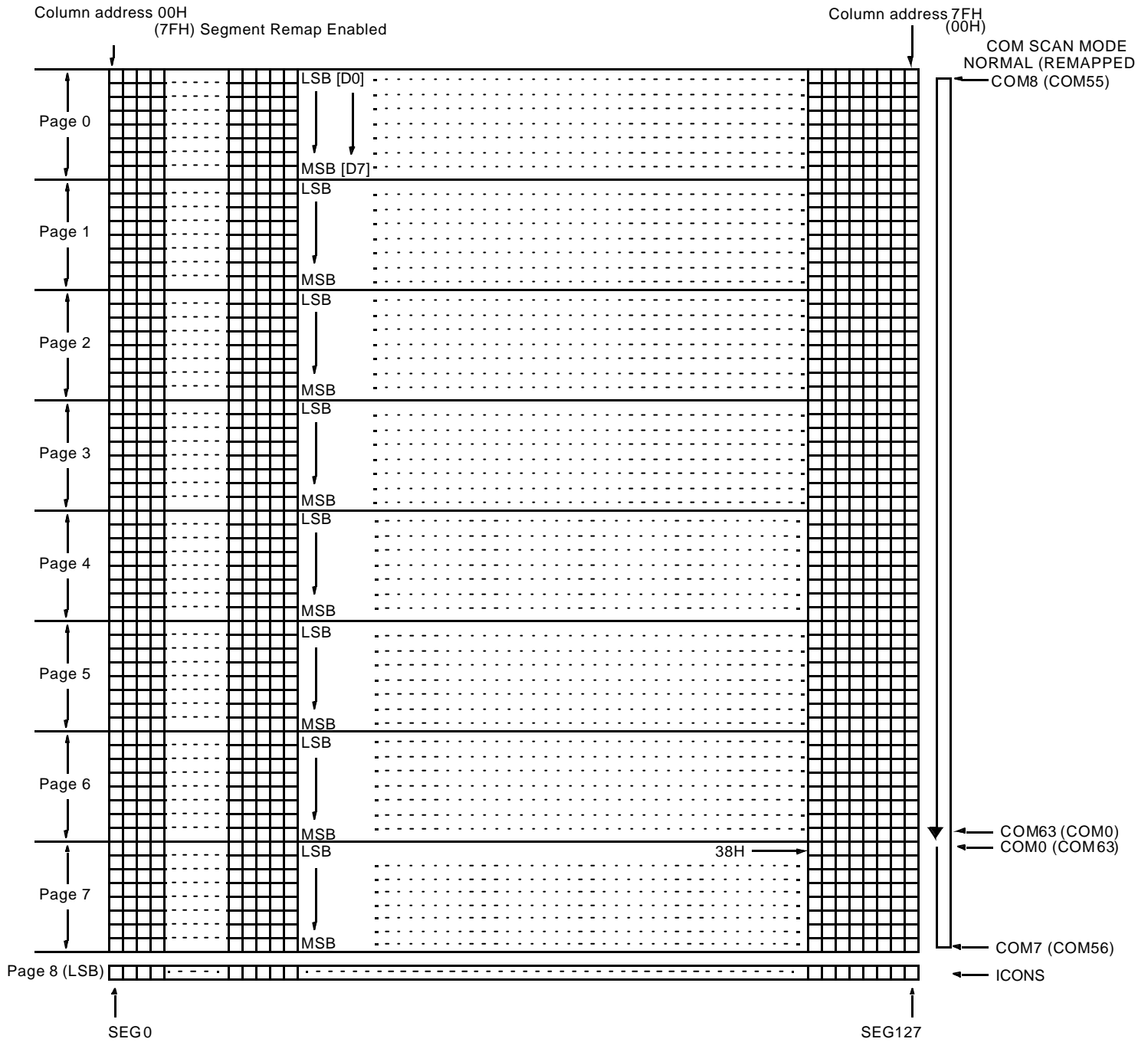


Figure 4: display data read with the insertion of dummy read

Graphic Display Data RAM (GDDRAM)

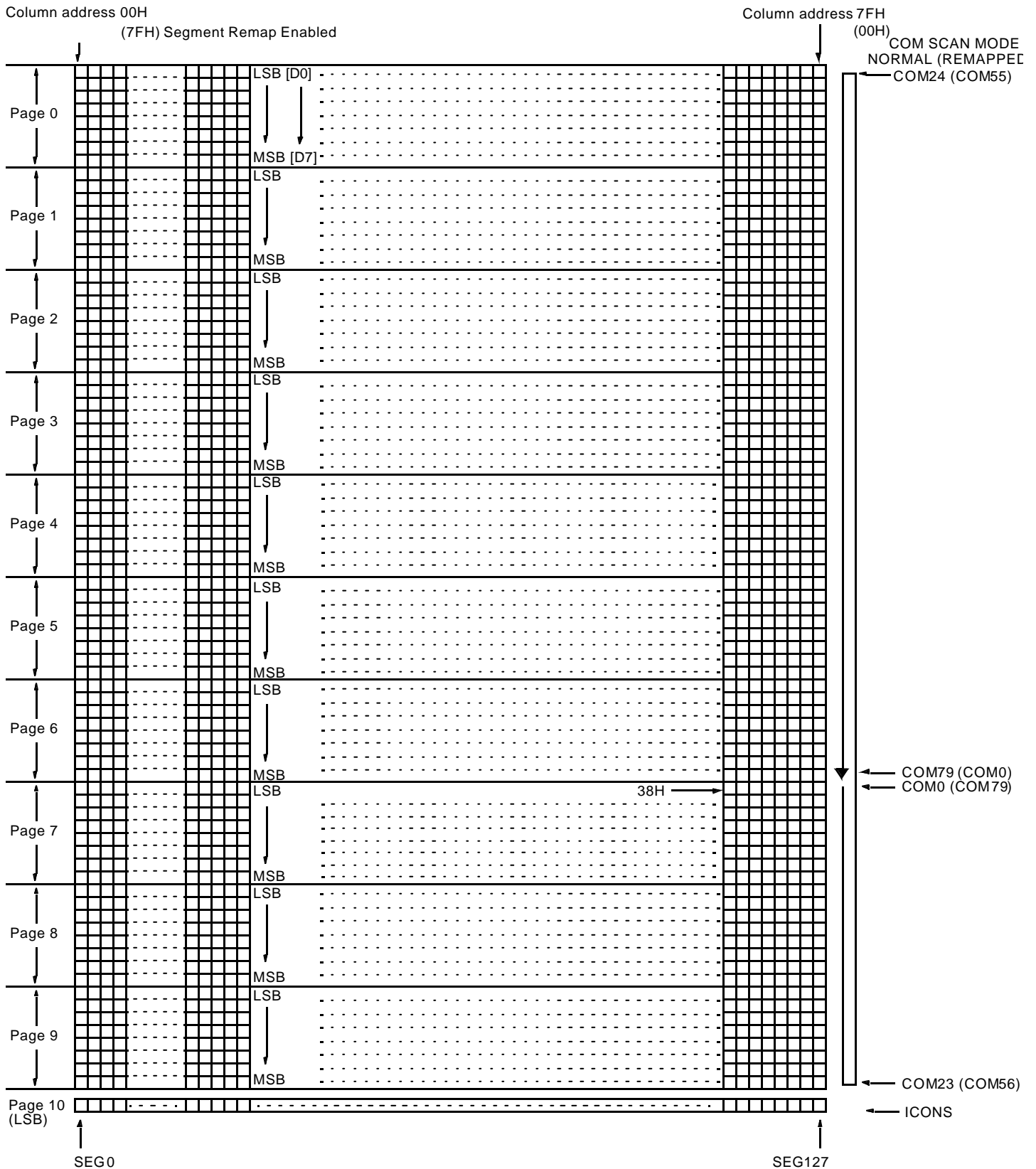
The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is $128 \times 65 = 8320$ bits for SSD1820A; $128 \times 81 = 10368$ bits for SSD1821. Figure 5, 6 are the description of the GDDRAM address map. For mechanical flexibility, re-mapping on both

Segment and Common outputs are provided. For vertical scrolling of display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display. Figure 5, 6 show the case in which the display start line register is set at 38H.



Note: The configuration in parentheses represent the remapping of Rows and Columns

Figure 5. SSD1820A Graphic Display Data RAM (GDDRAM) Address Map (with vertical scroll value 38H)



Note: The configuration in parentheses represent the remapping of Rows and Columns

Figure 6. SSD1821 Graphic Display Data RAM (GDDRAM) Address Map (with vertical scroll value 38H)

Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 7). The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

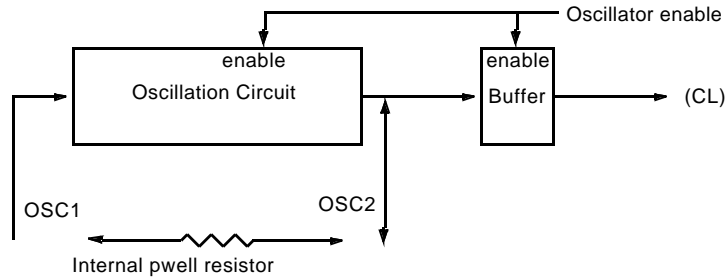


Figure 7. Oscillator Circuitry

LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage needed for display output. It takes a single supply input and generate necessary bias voltages. It consists of:

1. 2X, 3X, 4X, 5X and 6X DC-DC voltage converter

Please refer to application notes.

Please note that SSD1820A works up to 5X and SSD1820AT works up to 4X only.

2. Voltage Regulator

Feedback gain control for initial LCD voltage. External resistors are connected between V_{SS} and V_R , and between V_R and V_{L6} . These resistors are chosen to give the desired V_{L6} according to the following equation:

$$V_{L6} = \left(1 + \frac{R_2}{R_1}\right) \times V_{con} \times G$$

$$V_{con} = \left(1 - \frac{63 - \alpha}{210}\right) \times V_{ref}$$

where V_{ref} is the internally generated reference voltage with a known R_1 and R_2 . Typical value for V_{ref} is 2.1V

R_1 is the resistance of the resistor between V_{SS} and V_R .

R_2 is the resistance of the resistors between V_R and V_{L6} .

α is the software contrast level from 0 to 63.

$G = 1$ if INTRS = VDD; REF = VDD

$G = 0.84$ if INTRS = VSS; REF = VDD

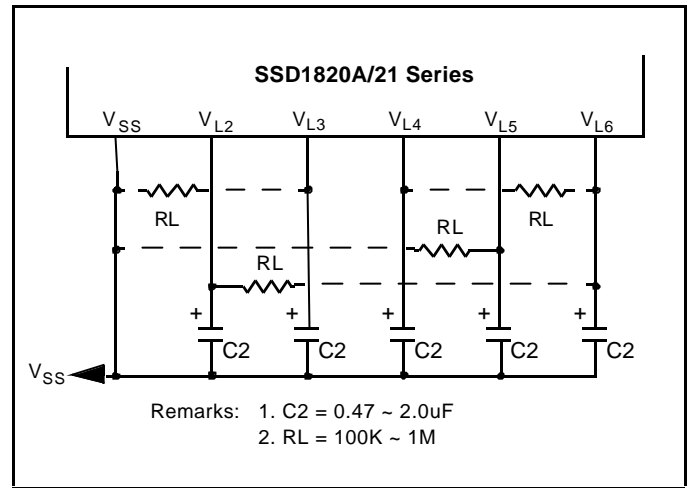
3. Bias Divider

If the output op-amp buffer option in Set Power Control Register command is enabled, this circuit block will divide the regulator output (V_{L6}) to give the LCD driving levels ($V_{L2} - V_{L5}$).

A low power consumption circuit design in this bias divider saves most of the display current comparing to traditional design.

Stablizing Capacitors (0.47~2uF) are required to be connected between these voltage level pins ($V_{L2} - V_{L5}$) and V_{SS} . If the LCD panel loading is heavy, capacitors and four additional resistors are suggest-

ed to add to the application circuit as follows:



Connections for heavy loading applications

4. Contrast Control

Software control of 64 voltage levels of LCD voltage.

5. Bias Ratio Selection circuitry

Software control of 1/4 to 1/10 bias ratio to match the characteristic of LCD panel.

Note: SSD1820A has 1/4 to 1/9 bias only.

6. Self adjust temperature compensation circuitry

Provide 2 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control. Defaulted temperature coefficient (TC) value is $-0.05\%/^{\circ}\text{C}$ for SSD1820A and $-0.07\%/^{\circ}\text{C}$ for SSD1821.

193/209 Bit Latch

A register carries the display signal information. In 128 X 65/81 display mode. Data will be fed to the HV-buffer Cell and level-shifted to the required level.

Level Selector

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

HV Buffer Cell (Level Shifter)

HV Buffer Cell works as a level shifter which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

Reset Circuit

When $\overline{\text{RES}}$ input is low, the chip is initialized to the following:

1. Page address is set to 0
2. Column address is set to 0
3. Display is OFF
4. Display Start Line is set to 0 (GDDRAM page 0, D0)
5. Display Offset is set to 0 (COM0 is mapped to ROW0)
6. 128x64 for SSD1820A / 128x80 for SSD1821
7. Normal/Reverse Display is Normal
8. n-line Inversion Register is 0
9. Entire Display is OFF
10. Power Control Register (VC, VR, VF) is set to (0,0,0)
11. 2X/3X Booster is selected
12. Internal Resistor Ratio register is set to 0H
13. Software Contrast is set to 32
14. LCD Bias Ratio is set to 1/9 for SSD1820A and 1/10 for SSD1821.
15. Normal scan direction of COM outputs
16. Segment remap is disabled (SEG0 display column address 0)
17. Internal oscillator is OFF
18. Test mode is OFF
19. Temperature coefficient is set to PTC0 for SSD1820A and PTC1 for SSD1821.
20. Icon display line is OFF
21. Interface Lock / Unlock register will be clear

When RESET command is issued, the following parameters are initialized only:

1. Page address is set to 0
2. Column address is set to 0
3. Initial Display Line is set to 0 (point to display RAM page 0, D0)
4. Internal Resistor Ratio register is set to 0H

LCD Panel Driving Waveform

The following is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveforms shown in Figure 8a and 7b illustrate the desired multiplex scheme with N-line Inversion feature is disabled (default).

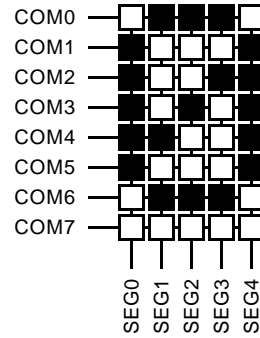
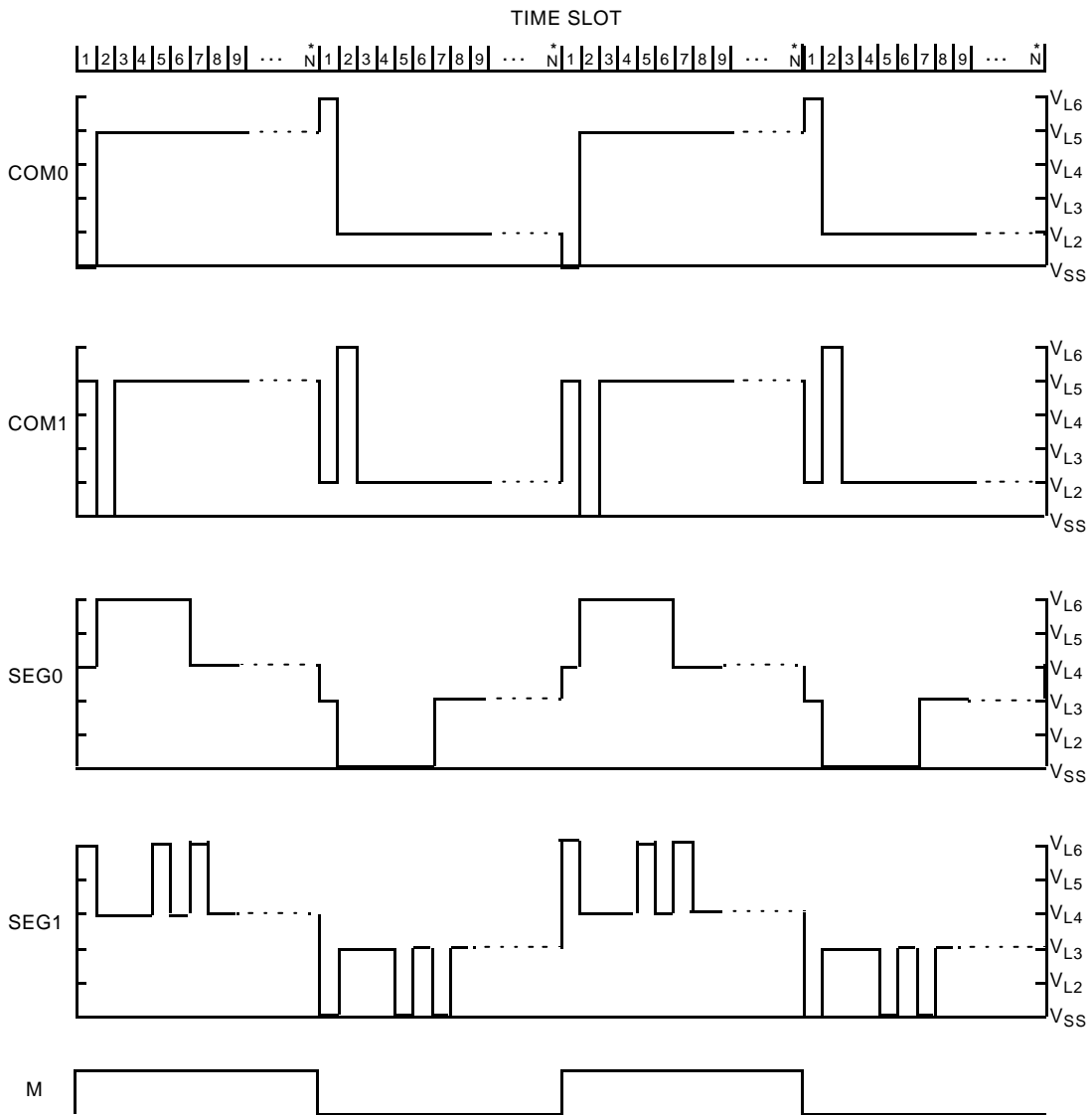


Figure 8a. LCD Display Example "0"



* Note : N is the number of multiplex ratio including Icon line if it is enabled, N is equal to 64/80 on POR.

Figure 8b. LCD Driving Signal from SSD1820A/SSD1821

COMMAND TABLE

Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Comment
00~0F	0	0	0	0	C3	C2	C1	C0	Set Lower Column Address	Sets the lower nibble of the column address pointer for RAM access. The pointer is reset to 0 after reset.
10~17	0	0	0	1	0	C6	C5	C4	Set Upper Column Address	Sets the upper nibble of the column address pointer for RAM access. The pointer is reset to 0 after reset.
18~1F									Reserved	Reserved
20~27	0	0	1	0	0	R2	R1	R0	Set Internal Regulator Resistor Ratio	The internal regulator gain $(1+R2/R1)V_{con}$ increases as R2R1R0 is increased from 000b to 111b. The resistor ratio $(1+R2/R1)$ is given by: R2R1R0 = 000: 2.3 (POR) R2R1R0 = 001: 3.0 R2R1R0 = 010: 3.7 R2R1R0 = 011: 4.4 R2R1R0 = 100: 5.1 R2R1R0 = 101: 5.8 R2R1R0 = 110: 6.5 R2R1R0 = 111: 7.2
28~2F	0	0	1	0	1	VC	VR	VF	Set Power Control Register	VC=0: turns OFF the internal voltage booster (POR) VC=1: turns ON the internal voltage booster VR=0: turns OFF the internal regulator (POR) VR=1: turns ON the internal regulator VF=0: turns OFF the output op-amp buffer (POR) VF=1: turns ON the output op-amp buffer
30~3F									Reserved	Reserved
40~43	0 x	1 L6	0 L5	0 L4	0 L3	0 L2	x L1	x L0	Set Display Start Line	The next command specifies the row address pointer (0-63) of the RAM data to be displayed in COM0. This command has no effect on COMS. The pointer is set to 0 after reset.
44~47	0 x	1 C6	0 C5	0 C4	0 C3	1 C2	x C1	x C0	Set Display Offset	The next command specifies the mapping of first display line (COM0) to one of ROW0~63. This command has no effect on COMS. COM0 is mapped to ROW0 after reset.
48~4B	0 x	1 D6	0 D5	0 D4	1 D3	0 D2	x D1	x D0	Set Multiplex Ratio	The next command specifies the number of lines, excluding COMS, to be displayed. With Icon is disabled (POR), duties 1/16~1/64 or 1/80 could be selected. With Icon enabled, the available duty ratios are 1/17~ 1/65 or 1/81.
4C~4F	0 x	1 x	0 x	0 N4	1 N3	1 N2	x N1	x N0	Set N-line Inversion	The next command sets the n-line inversion register from 3 to 33 lines to reduce display crosstalk. Register values from 00001b to 11111b are mapped to 3 lines to 33 lines respectively. Value 00000b disables the N-line inversion, which is the POR value. To avoid a fix polarity at some lines, it should be noted that the total number of mux (including the icon line) should NOT be a multiple of the lines of inversion (n).
50~57	0	1	0	1	0	B2	B1	B0	Set LCD Bias	Sets the LCD bias from 1/4 ~ 1/10 according to B2B1B0: 000: 1/4 bias 001: 1/5 bias 010: 1/6 bias 011: 1/7bias 100: 1/8 bias 101: 1/9 bias (POR for SSD1820A) 110: 1/9 bias (for SSD1820A) 1/10 bias (POR for SSD1821) 111: 1/9 bias (for SSD1820A); 1/10 bias (for SSD1821)

58-63										Reserved	Reserved
64-67	0	1	1	0	0	1	B1	B0		Set DC-DC Converter Factor	Sets the DC-DC multiplying factor from 2X to 6X B1B0: 00: 2X/3X (POR, 2X or 3X multiplying depended on the DC-DC converter configuration) 01: 4X 10: 5X (for SSD1820A) 11: 5X (for SSD1820A); 6X (for SSD1821)
68-80										Reserved	Reserved
81	1 x	0 x	0 C5	0 C4	0 C3	0 C2	0 C1	1 C0		Set Contrast Control Register	The next command sets one of the 64 contrast levels. The darkness increase as the contrast level increase. The level is set to 32 after POR.
82-9F										Reserved	Reserved
A0-A1	1	0	1	0	0	0	0	S0		Set Segment Re-map	S0=0: column address 00H is mapped to SEG0 (POR) S0=1: column address 7FH is mapped to SEG0
A2-A3	1	0	1	0	0	0	1	C0		Set Icon Enable	C0=0: Disable icon row (Mux = 16 to 64/80, POR) C0=1: Enable icon row (Mux = 17 to 65/81)
A4-A5	1	0	1	0	0	1	0	E0		Set Entire Display On/Off	E0=0: Normal display (display according to RAM contents, POR) E0=1: All pixels are ON regardless of the RAM contents *Note: This command will override the effect of "Set Normal/Reverse Display"
A6-A7	1	0	1	0	0	1	1	R0		Set Normal/Reverse Display	R0=0: Normal display (display according to RAM contents, POR) R0=1: Reverse display (ON and OFF pixels are inverted) *Note: This command will not affect the display of the icon lines
A8										Reserved	Reserved
A9	1	0	1	0	1	0	0	1		Set Power Save Mode	Enter Sleep mode
AA										Reserved	Reserved
AB	1	0	1	0	1	0	1	1		Start Internal Oscillator	Oscillator is OFF after reset, until this command is issued. This command is required even if external oscillator is used.
AE-AF	1	0	1	0	1	1	1	D0		Set Display On/Off	D0=0: Display OFF (POR) D0=1: Display ON
B0-BF	1	0	1	1	P3	P2	P1	P0		Set Page Address	Set GDDRAM page address (0-10) using P3P2P1P0 for RAM access. The page address is sets to 0 after reset.
C0-CF	1	1	0	0	S0	x	x	x		Set COM Output Scan Direction	S0=0: Normal mode (POR) S0=1: Remapped mode. COM0 to COM[N-1] becomes COM[N-1] to COM0 when the duty is set to N. See Figure 5/6 as an example for N equals to 64/80. *Note: This command will not affect the display of the icon lines
D0-E0										Reserved	Reserved
E1	1	1	1	0	0	0	0	1		Exit Power-save Mode	DC-DC converter, regulator and divider status before entering the power-save mode is restored. At POR, Power-save Mode is released.
E2	1	1	1	0	0	0	1	0		Software Reset	Initialize some internal registers
E3										Reserved	Reserved
E4	1	1	1	0	0	1	0	0		Exit N-line Inversion	The frame will be inverted once per frame
E5-E7										Reserved	Reserved

E8	1	1	1	0	1	0	0	0	0	Set Display Data Length	This command is valid only at 3-wire SPI (PS0=PS1=L) The next command specifies the number of bytes of display data to be written after this composite command. D(7:0)=00: 1 byte of display data is to be sent D(7:0)=FF: 256 bytes of display data is to be sent
E9~EF										Reserved	Reserved
F0~FF	1	1	1	1	x	x	x	x		Extended Features	Test mode commands and Extended features, see Extended Command Table.

EXTENDED COMMAND TABLE

Bit Pattern	Command	Comment
11110001 00001X ₂ X ₁ X ₀	X ₂ X ₁ X ₀ : Set TC Value	X ₂ X ₁ X ₀ = 000: -0.05%/C (POR for 1820A) X ₂ X ₁ X ₀ = 001: -0.07%/C (POR for 1821)
11110010 0010X ₃ X ₂ X ₁ X ₀	X ₃ : Select Oscillator Source X ₂ X ₁ X ₀ : Set Oscillator Value	X ₃ = 0: Internal RC oscillator is selected (POR) X ₃ = 1: External oscillator from CL pin is selected if X ₃ = 0, X ₂ X ₁ X ₀ = 000: -16% X ₂ X ₁ X ₀ = 001: -10% X ₂ X ₁ X ₀ = 010: 0% (POR) X ₂ X ₁ X ₀ = 011: +10% X ₂ X ₁ X ₀ = 100: +16% X ₂ X ₁ X ₀ = 101: +30% X ₂ X ₁ X ₀ = 110: +54% X ₂ X ₁ X ₀ = 111: +81%
11111101 00010L10	L: Interface Lock / Unlock	L = 0 Interface Unlock (POR) L = 1 Interface Lock
Other than above	Reserved	

Read Status Byte

A 8 bits status byte will be placed to the data bus if a read operation is performed if \overline{DC} is low. The status byte is defined as follow.

D7	D6	D5	D4	D3	D2	D1	D0	Comment
BUSY	ON	RES	0	1	0	0	DS0	BUSY=0: Chip is idle BUSY=1: Chip is executing instruction ON=0: Display is OFF ON=1: Display is ON RES=0: Chip is idlex RES=1: Chip is executing reset DS0=0: SSD1820A; DS0=1:SSD1821

Data Read / Write

To read data from the GDDRAM, input High to $R/\overline{W}(\overline{WR})$ pin and $\overline{D}/\overline{C}$ pin for 6800-series parallel mode, Low to $E(\overline{RD})$ pin and High to $\overline{D}/\overline{C}$ pin for 8080-series parallel mode. No data read is provided for serial mode. In normal mode, GDDRAM column address pointer will be increased by one automatically after each data read. Also, a dummy read is required before the first data is read. See Figure 4 in Func-

tional Description.

To write data to the GDDRAM, input Low to $\overline{R\overline{W}}(\overline{WR})$ pin and High to $\overline{D/C}$ pin for 6800-series parallel mode. For serial interface, it will always be in write mode. GDDRAM column address pointer will be increased by one automatically after each data write. The address will be reset to 0 in next data read/write operation is executed when it is 127.

Address Increment Table (Automatic)

$\overline{D/C}$	$\overline{R\overline{W}}(\overline{WR})$	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

Address Increment is done automatically after data read/write. The column address pointer of GDDRAM is also affected. It will be reset to 0 in next data read/write operation is executed when it is 127.

Commands Required for $\overline{R\overline{W}}(\overline{WR})$ Actions on RAM

$\overline{R\overline{W}}(\overline{WR})$ Actions on RAMs	Commands Required	
Read/Write Data from/to GDDRAM.	Set GDDRAM Page Address	(1011X ₃ X ₂ X ₁ X ₀)*
	Set GDDRAM Column Address	(0001X ₃ X ₂ X ₁ X ₀)*
		(0000X ₃ X ₂ X ₁ X ₀)*
	Read/Write Data	(X ₇ X ₆ X ₅ X ₄ X ₃ X ₂ X ₁ X ₀)

* No need to resend the command again if it is set previously.

The read / write action to the Display Data RAM does not depend on the display mode. This means the user can change the RAM content whether the target RAM content is being displayed or not.

Command Description

Set Display On/Off

This command turns the display on/off, by the value of the LSB.

Set Display Start Line

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 63/79. With value equals to 0, D0 of Page 0 is mapped to COM0. With value equals to 1, D1 of Page0 is mapped to COM0. The display start line values of 0 to 63/79 are assigned to Page 0 to 7/9.

Set Page Address

This command positions the page address to 0 to 8/10 possible positions in GDDRAM. Refer to figure 5/6.

Set Higher Column Address

This command specifies the higher nibble of the 7-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU and returning to 0 once overflow (>127).

Set Lower Column Address

This command specifies the lower nibble of the 7-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU and returning to 0 once overflow (>127).

Set Segment Re-map

This commands changes the mapping between the display data column address and segment driver. It allows flexibility in layout during LCD module assembly. Refer to figure 5/6.

Set Normal/Reverse Display

This command sets the display to be either normal/reverse. In normal display, a RAM data of 1 indicates an "ON" pixel while in reverse display, a RAM data of 0 indicates an "ON" pixel. The icon line is not affected by this command.

Set Entire Display On/Off

This command forces the entire display, including the icon row, to be "ON" regardless of the contents of the display data RAM. This command has priority over normal/reverse display.

To executed this command, Set Display On command must be sent in advance.

Set LCD Bias

This command selects a suitable bias ratio (1/4 to 1/9 or 1/10) required for driving the particular LCD panel in use. The POR default for SSD1820A is set to 1/9 bias; and 1/10 bias for SSD1821.

Software Reset

This command causes some of the internal status of the chip to be initialized:

1. Page address is set to 0
2. Column address is set to 0
3. Initial Display Line is set to 0 (point to display RAM page 0, D0)
4. Internal Resistor Ratio register is set to (0,0,0)
5. Software Contrast is set to 32

Set COM Output Scan Direction

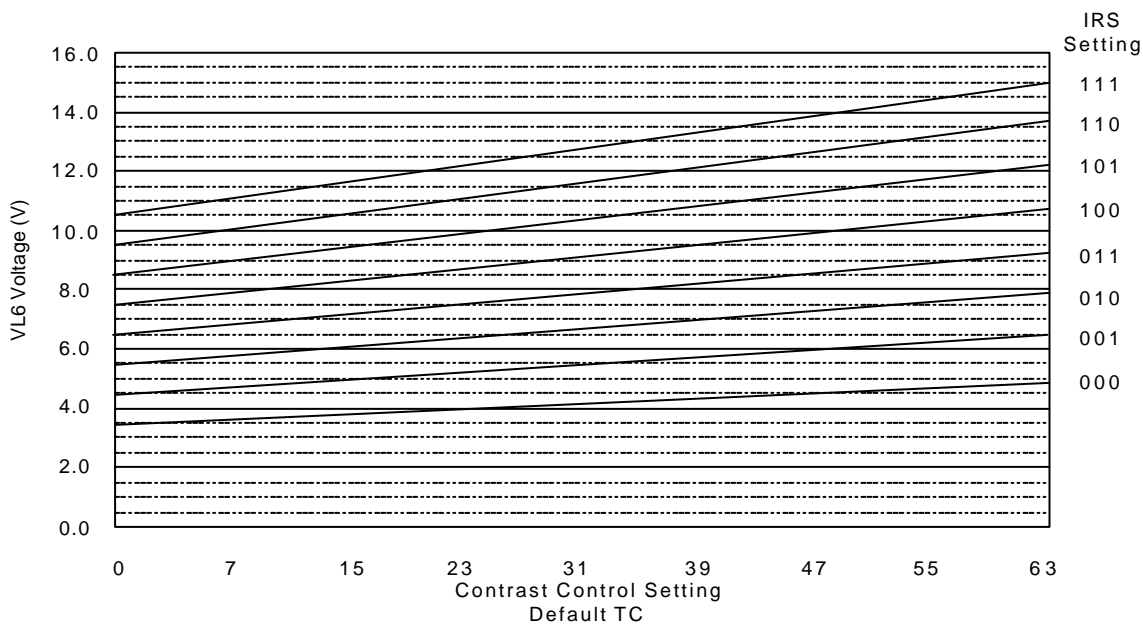
This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly.

Set Power Control Register

This command turns on/off the various power circuits associated with the chip.

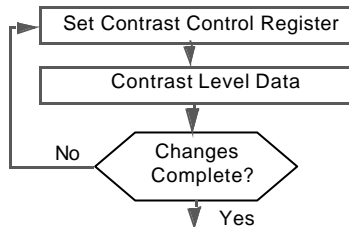
Set Internal Regulator Resistors Ratio

This command is to enable any one of the eight internal resistor (IRS) settings for different regulator gains when using internal regulator resistor network (INTRS pin pulled high). When external resistors are used, INTRS must be connected to VSS. The Contrast Control Voltage Range curves is given in the figure below:



Set Contrast Control Register

This command adjusts the contrast of the LCD panel by changing VL6 of the LCD drive voltage provided by the On-Chip power circuits. VL6 is set with 64 steps (6-bit) contrast control register. It is a compound commands:



Set Display Offset

The next command specifies the mapping of display start line (COM0 if display start line register equals to 0) to one of ROW0-63/79. This command has no effect on COMS. COM0 is mapped to ROW0 after reset.

Set Multiplex Ratio

This command switches default 64 multiplex mode to any multiplex from 16 to 64/80, if Icon is disabled (POR). When Icon is set enable, the corresponding multiplex ratio setting will be mapped to 17 to 65/81. The chip pads ROW0-ROW63/ROW79 will be switched to corresponding COM signal output as specified in Table 1 or 2.

Set Power Save Mode

To force the chip to enter Sleep Mode.

Exit Power Save Mode

This command releases the chip from Sleep Mode and return to normal operation.

Set N-line Inversion

Number of line inversion is set by this command for reducing crosstalk noise. 3 to 33-line inversion operations could be selected. At POR, this operation is disabled.

It should be noted that the total number of mux (including the icon line) should NOT be a multiple of the inversion number (n). Or else, some lines will not change their polarity during frame change.

Exit N-line Inverstion

This command releases the chip from N-line inversion mode. The driving waveform will be inverted once per frame after issuing this command.

Set DC-DC Converter Factor

Internal DC-DC converter factor is set by this command. For SSD1820A, 2X to 5X multiplying factors could be selected. For SSD1821, 2X to 6X multiplying factors could be selected. 2X/3X, 4X, 5X and 6X factors are selected using this command. Hardware configuration is used for 2X or 3X setup.

Set Icon Enable

This command enable/disable the Icon display.

Start InternalOscillator

After POR, the internal oscillator is OFF. It should be turned ON by sending this command to the chip.

Set Display Data Length

This two-byte command only valid when 3-wire SPI configuration is set by H/W input (PS0=PS1=L). The second 8-bit is used to indicate that a specified number display data byte (1-256) are to be transmitted. Next byte after the display data string is handled as a command.

Set Test Mode

This command force the driver chip into its test mode for internal testing of the chip. Under normal operation, user should NOT use this command.

Status register Read

This command is issued by setting \overline{DC} Low during a data read (refer to figure 1 and 2 parallel interface waveform). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

EXTENDED COMMANDS

These commands are used, in addition to basic commands, to enable the enhanced features designed in the chips.

Set Temperature Coefficient (TC) Value

This command is to set 1 out of 2 different temperature coefficients in order to match various liquid crystal temperature grades.

Enable external oscillator input.

This command enables the external clock input from CL pin.

Select Oscillator Source

This command is used to adjust the oscillator frequency to desire frame frequency.

Set Interface Lock / Unlock

After the interface lock command is issued, no more data or commands will be accepted until an interface unlock command is issued.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{CC}		$V_{SS}-0.3$ to $V_{SS}+15.0$	V
V_{CI}	Booster Supply Voltage	V_{DD} to +4.0	V
V_{in}	Input Voltage	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-40 to +85	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} < \text{or} = (V_{in} \text{ or } V_{out}) < \text{or} = V_{DD}$. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS} , $V_{DD}=1.8$ to $3.3V$, $T_A=-40$ to 85°C ; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ (at 25°C)	Max	Unit
V_{DD}	Logic Circuit Supply Voltage Range Voltage Generator Circuit Supply Voltage Range	(Absolute value referenced to V_{SS})	1.8	2.7	3.3	V
I_{AC}	Access Mode Supply Current Drain (V_{DD} Pins)	$V_{DD} = 2.7V$, Voltage Generator On, 4X Converter Enabled, Write accessing, $T_{Cyc} = 3.3MHz$, Osc. Freq.=31kHz, Display On.	-	300	600	μA
I_{DP1}	Display Mode Supply Current Drain (V_{DD} Pins)	$V_{DD} = 2.7V$, $V_{CC} = 10.8V$, Voltage Generator Off, external Divider Enabled. Read/Write Halt, Osc. Freq. = 31kHz, Display On, VL6= 9.0V.	-	15	26	μA
I_{DP2}	Display Mode Supply Current Drain (V_{DD} Pins)	$V_{DD} = V_{CI} = 2.7V$, $V_{CC} = 10.8V$, Voltage Generator On, 4x DC-DC Converter Enabled, V_{CI} pin connected to V_{DD} . Internal Divider Enabled. Read/Write Halt, Osc. Freq. = 31kHz, Display On, VL6 = 9.0V.	-	90	120	μA
I_{SB}	Standby Mode Supply Current Drain (V_{DD} Pins)	$V_{DD}=2.7V$, LCD Driving Waveform Off, Osc. Freq. = 31kHz, Read/Write halt.	-	8.0	37	μA
I_{SLEEP}	Sleep Mode Supply Current Drain (V_{DD} Pins)	$V_{DD} = 2.7V$, LCD Driving Waveform Off, Oscillator Off, Read/Write halt.	-	0.5	3	μA
V_{CC}	LCD Driving Voltage Generator Output (V_{CC} Pin)	Display On, Voltage Generator Enabled, DC/DC Converter Enabled, Osc. Freq.=31kHz, Regulator Enabled, Divider Enabled.	V_{DD}	-	15.0	V
V_{LCD}	DC-DC Converter Efficiency	$I_{CC} < 20\mu A$	95	99		%
	LCD Driving Voltage Input (V_{CC} Pin)	Voltage Generator Disabled.	4.0	-	15.0	V
V_{REF}	External Reference Voltage Input	Internal Reference Voltage Source Disable (REF pin pulled Low), External Reference voltage input to V_{EXT} pin.	2.04	2.10	2.16	V
	Internal Reference Voltage	Internal Reference Voltage Source Enabled (REF pin pulled High), V_{EXT} pin NC.		2.10		V

V _{OH1}	Output High Voltage (D ₀ -D ₇)	I _{out} = +500μA	0.8*V _D	-	V _{DD}	V
V _{OL1}	Output Low Voltage (D ₀ -D ₇)	I _{out} = -500μA	D	-	0.2*V _D	V
VL6	LCD Driving Voltage Source (VL6 Pin)	Regulator Enabled (VL6 voltage depends on Int/Ext Contrast Control)	0	-	D	V
VL6	LCD Driving Voltage Source (VL6 Pin)	Regulator Disable	V _{DD}	-	V _{CC} -0.5	V
VL6	LCD Driving Voltage Source (VL6 Pin)	Regulator Disable	-	Floating	-	V
V _{IH1}	Input high voltage (RES, PS0, PS1, CS, D/C, R/W, D ₀ -D ₇ , REF, INTRIS)		0.8*V _D	-	V _{DD}	V
V _{IL1}	Input Low voltage (RES, PS0, PS1, CS, D/C, R/W, D ₀ -D ₇ , REF, INTRIS)		D	-	0.2*V _D	V
V _{L6} V _{L5} V _{L4} V _{L3} V _{L2}	LCD Display Voltage Output (V _{L6} , V _{L5} , V _{L4} , V _{L3} , V _{L2} Pins)	Bias Divider Enabled, 1:a bias ratio	-	V _{L6} (a-1)/a*V _{L6} (a-2)/a*V _{L6} 2/a*V _{L6} 1/a*V _{L6}	-	V V V V V
V _{L6} V _{L5} V _{L4} V _{L3} V _{L2}	LCD Display Voltage Input (V _{L6} , V _{L5} , V _{L4} , V _{L3} , V _{L2} Pins)	Voltage reference to V _{SS} , External Voltage Generator, Bias Divider Disabled	V _{L5} V _{L4} V _{L3} V _{L2} V _{SS}	-	V _{CC} V _{L6} V _{L5} V _{L4} V _{L3}	V V V V V
I _{OH}	Output High Current Source (D ₀ -D ₇)	V _{out} =V _{DD} -0.4V	50	-	-	μA
I _{OL}	Output Low Current Drain (D ₀ -D ₇)	V _{out} =0.4V	-	-	-50	μA
I _{OZ}	Output Tri-state Current Drain Source (D ₀ -D ₇)		-1	-	1	μA
I _{IL} /I _{IH}	Input Current (RES, PS0, PS1, CS, E, D/C, R/W, D ₀ -D ₇ , REF, INTRIS)		-1	-	1	μA
C _{IN}	Input Capacitance (all logic pins)		-	5	7.5	pF
ΔVL6	Variation of VL6 Output (1.8V < V _{DD} < 3.0V)	Regulator Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0	-	± 2	-	%
PTC0 PTC1	Temperature Coefficient Compensation* Temperature Coefficient 0 Temperature Coefficient 1	Voltage Regulator Enabled (POR for SSD1820A) Voltage Regulator Enabled (POR for SSD1821)	-0.04 -0.06	-0.05 -0.07	-0.06 -0.08	% %

* The formula for the temperature coefficient is:

$$TC(\%) = \frac{V_{L6} \text{ at } 50^{\circ}\text{C} - V_{L6} \text{ at } 0^{\circ}\text{C}}{50^{\circ}\text{C} - 0^{\circ}\text{C}} \times \frac{1}{V_{L6} \text{ at } 25^{\circ}\text{C}} \times 100\%$$

AC ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$, Voltage referenced to V_{SS} , $V_{DD}=V_{CI}=2.7\text{V}$, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ(at 25°C)	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing Generator (SSD1820A/21)	Internal Oscillator Enabled	28.4	33	39	kHz
F_{FRM}	Frame Frequency $\frac{F_{OSC}}{6 \times 65}$ (SSD1820A)	Display ON, Set 128 x 64 Graphic Display Mode, Icon Line Enabled. POR Oscillator Settings	70	84.6	100	Hz
	Frame Frequency $\frac{F_{OSC}}{5 \times 81}$ (SSD1821)	Display ON, Set 128 x 80 Graphic Display Mode, Icon Line Enabled. POR Oscillator Settings	70	81.5	100	Hz

TABLE 3a. Parallel Timing Characteristics ($T_A=-40$ to 85°C , $V_{DD}=2.7\text{V}$, $V_{SS}=0\text{V}$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	66	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	2	-	-	ns
t_{DHR}	Read Data Hold Time	10	-	-	ns
t_{OH}	Output Disable Time	-	-	30	ns
t_{ACC}	Access Time (RAM)	-	-	80	ns
	Access Time (Command)	-	-	25	ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM)	95	-	-	ns
	Chip Select Low Pulse Width (read Command)	40	-	-	ns
	Chip Select Low Pulse Width (write)	15	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	30	-	-	ns
	Chip Select High Pulse Width (write)	30	-	-	ns
t_{R}	Rise Time	-	-	10	ns
t_{F}	Fall Time	-	-	10	ns

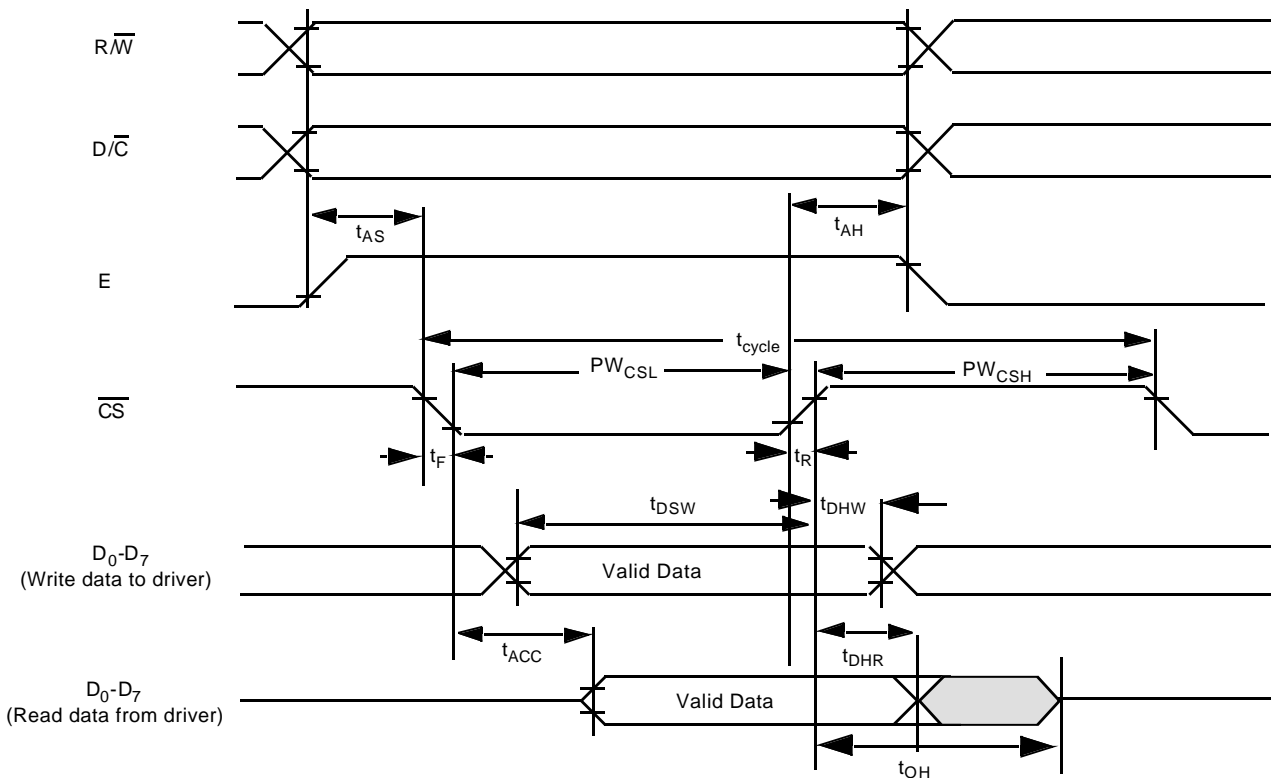


Figure 1a. Parallel 6800-series Interface Timing Characteristics (PS0 = H, PS1 = H)

TABLE 3b. Parallel Timing Characteristics ($T_A=-40$ to 85°C , $V_{DD}=1.8\text{V}$, $V_{SS}=0\text{V}$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	80	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	5	-	-	ns
t_{DHR}	Read Data Hold Time	15	-	-	ns
t_{OH}	Output Disable Time	-	-	40	ns
t_{ACC}	Access Time (RAM)	-	-	100	ns
	Access Time (command)	-	-	35	ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM)	120	-	-	ns
	Chip Select Low Pulse Width (read Command)	55	-	-	ns
	Chip Select Low Pulse Width (write)	20	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	40	-	-	ns
	Chip Select High Pulse Width (write)	40	-	-	ns
t_{R}	Rise Time	-	-	10	ns
t_{F}	Fall Time	-	-	10	ns

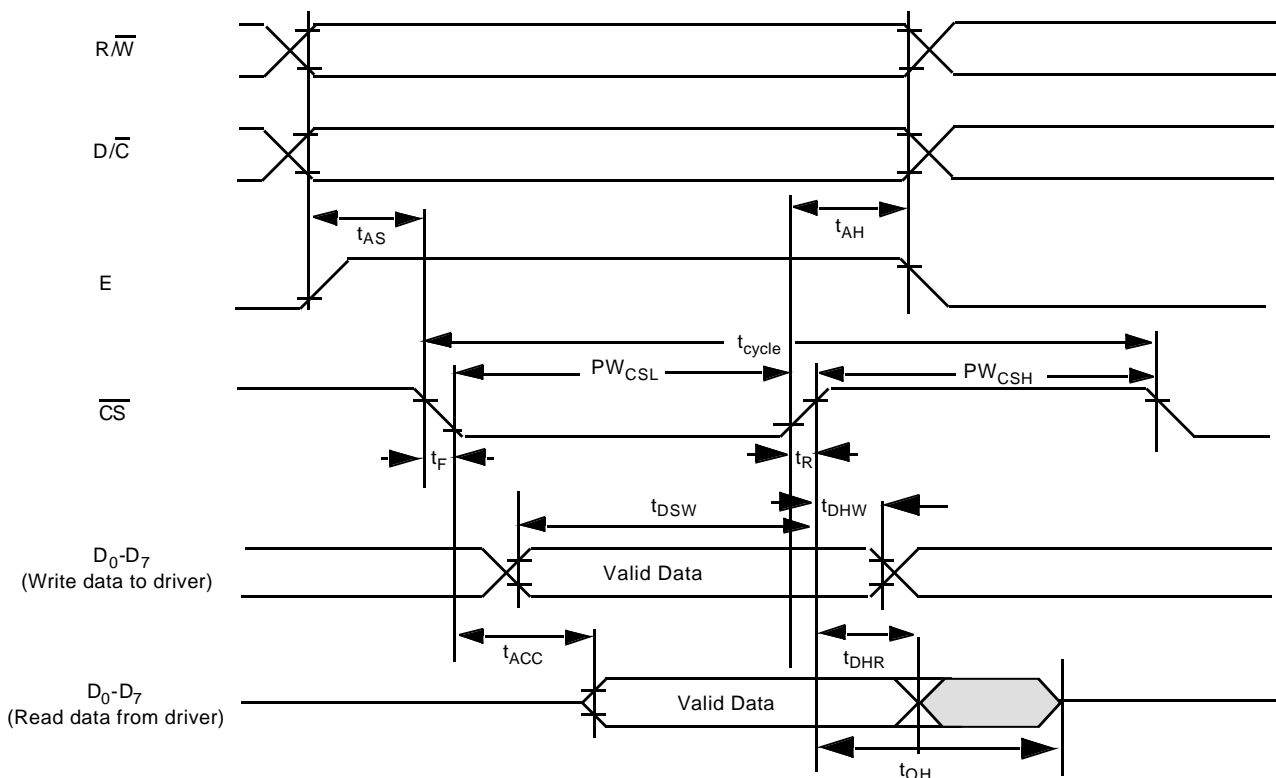


Figure 1b. Parallel 6800-series Interface Timing Characteristics (PS0 = H, PS1 = H)

TABLE 4a. Parallel Timing Characteristics ($T_A=-40$ to 85°C , $V_{DD}=2.7\text{V}$, $V_{SS}=0\text{V}$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	66	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	2	-	-	ns
t_{DHR}	Read Data Hold Time	10	-	-	ns
t_{OH}	Output Disable Time	-	-	30	ns
t_{ACC}	Access Time (RAM)	-	-	80	ns
	Access Time (Command)	-	-	25	ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM)	95	-	-	ns
	Chip Select Low Pulse Width (read Command)	40	-	-	ns
	Chip Select Low Pulse Width (write)	15	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	30	-	-	ns
	Chip Select High Pulse Width (write)	30	-	-	ns
t_{R}	Rise Time	-	-	10	ns
t_{F}	Fall Time	-	-	10	ns

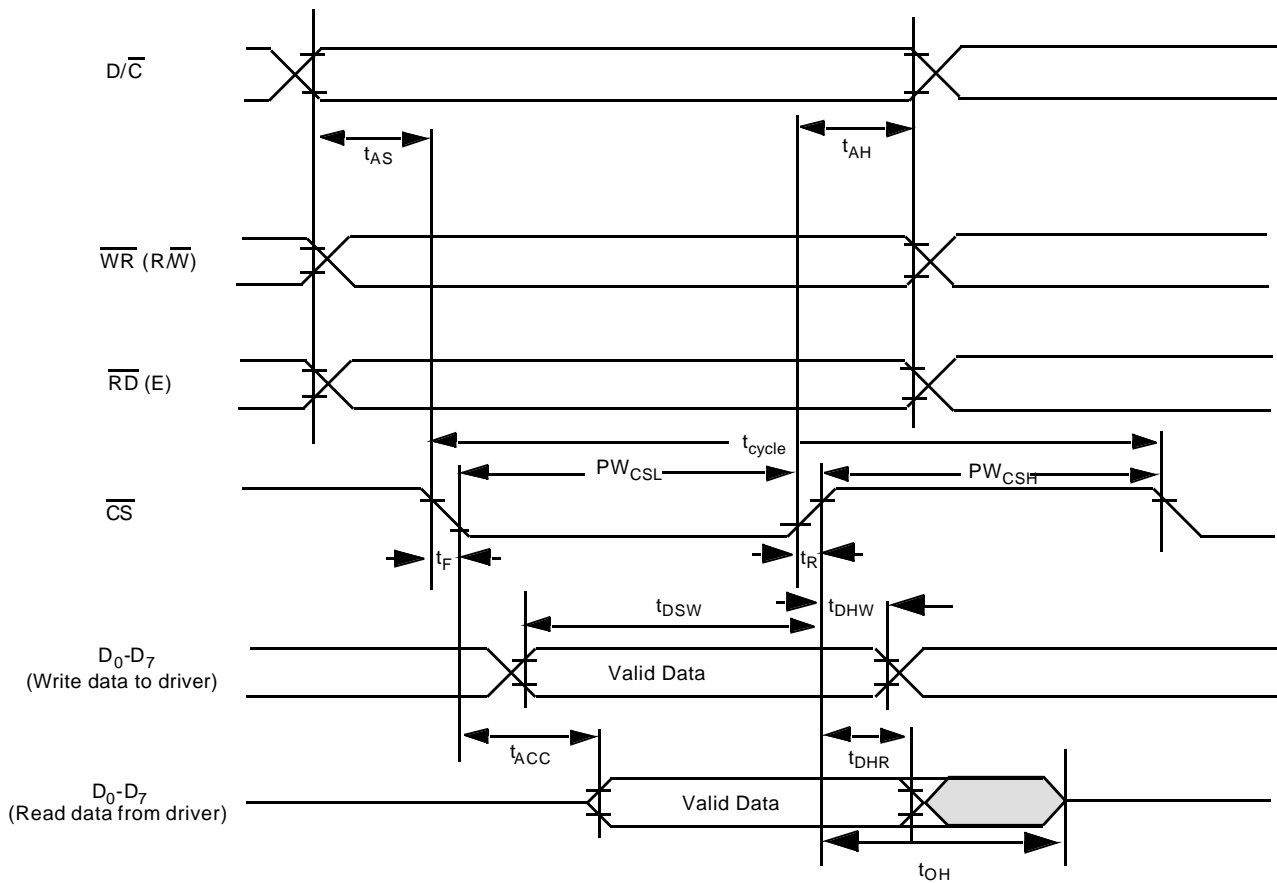


Figure 2a. Parallel 8080-series Interface Timing Characteristics ($\text{PS0} = \text{H}$, $\text{PS1} = \text{L}$)

TABLE 4b. Parallel Timing Characteristics ($T_A=-40$ to 85°C , $V_{DD}=1.8\text{V}$, $V_{SS}=0\text{V}$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	80	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	5	-	-	ns
t_{DHR}	Read Data Hold Time	15	-	-	ns
t_{OH}	Output Disable Time	-	-	40	ns
t_{ACC}	Access Time (RAM)	-	-	100	ns
	Access Time (command)	-	-	35	ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM)	120	-	-	ns
	Chip Select Low Pulse Width (read Command)	55	-	-	ns
	Chip Select Low Pulse Width (write)	20	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	40	-	-	ns
	Chip Select High Pulse Width (write)	40	-	-	ns
t_{R}	Rise Time	-	-	10	ns
t_{F}	Fall Time	-	-	10	ns

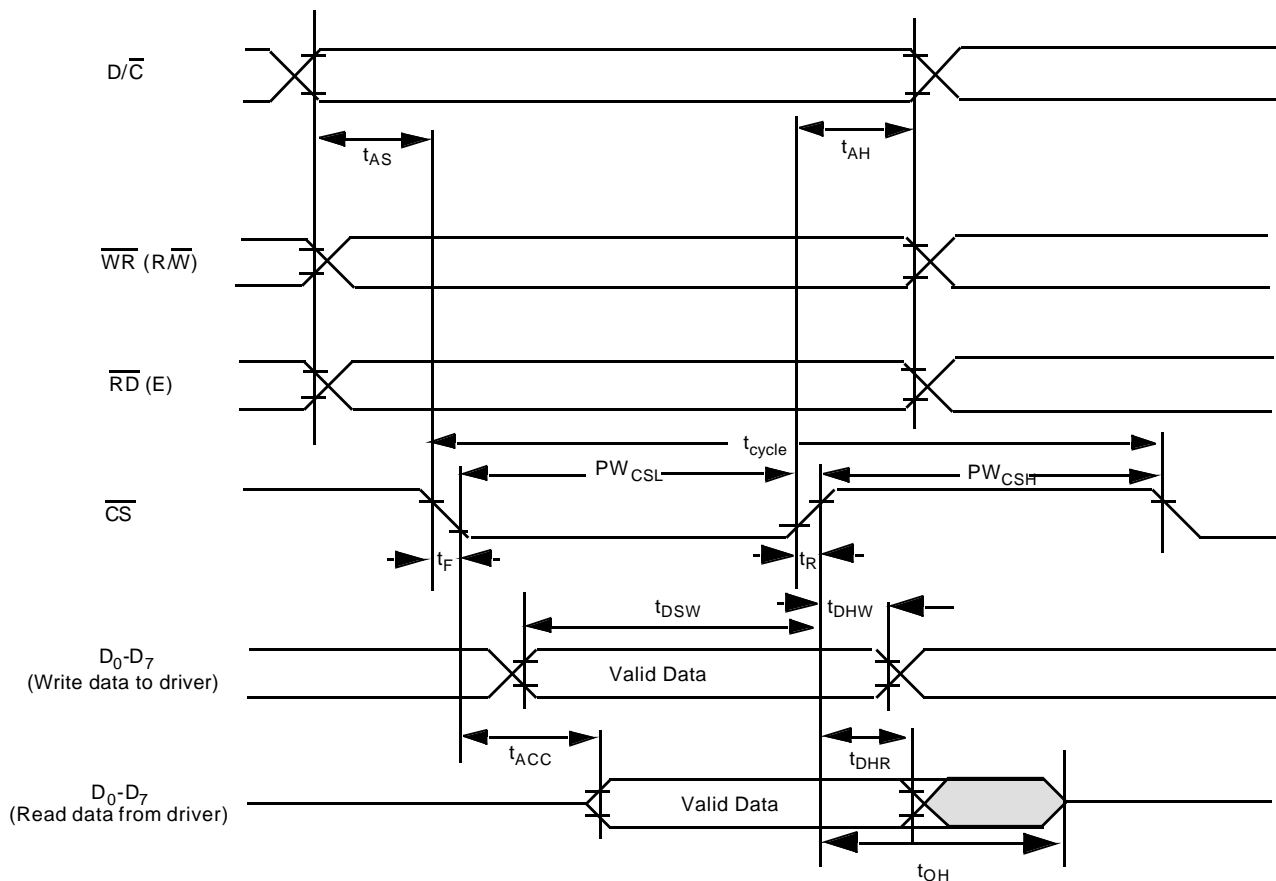


Figure 2b. Parallel 8080-series Interface Timing Characteristics (PS0 = H, PS1 = L)

TABLE 5a. Serial Timing Characteristics ($T_A=-40$ to 85°C , $V_{DD}=2.7\text{V}$, $V_{SS}=0\text{V}$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	59	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	5	-	-	ns
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	5	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	10	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_{R}	Rise Time	-	-	10	ns
t_{F}	Fall Time	-	-	10	ns

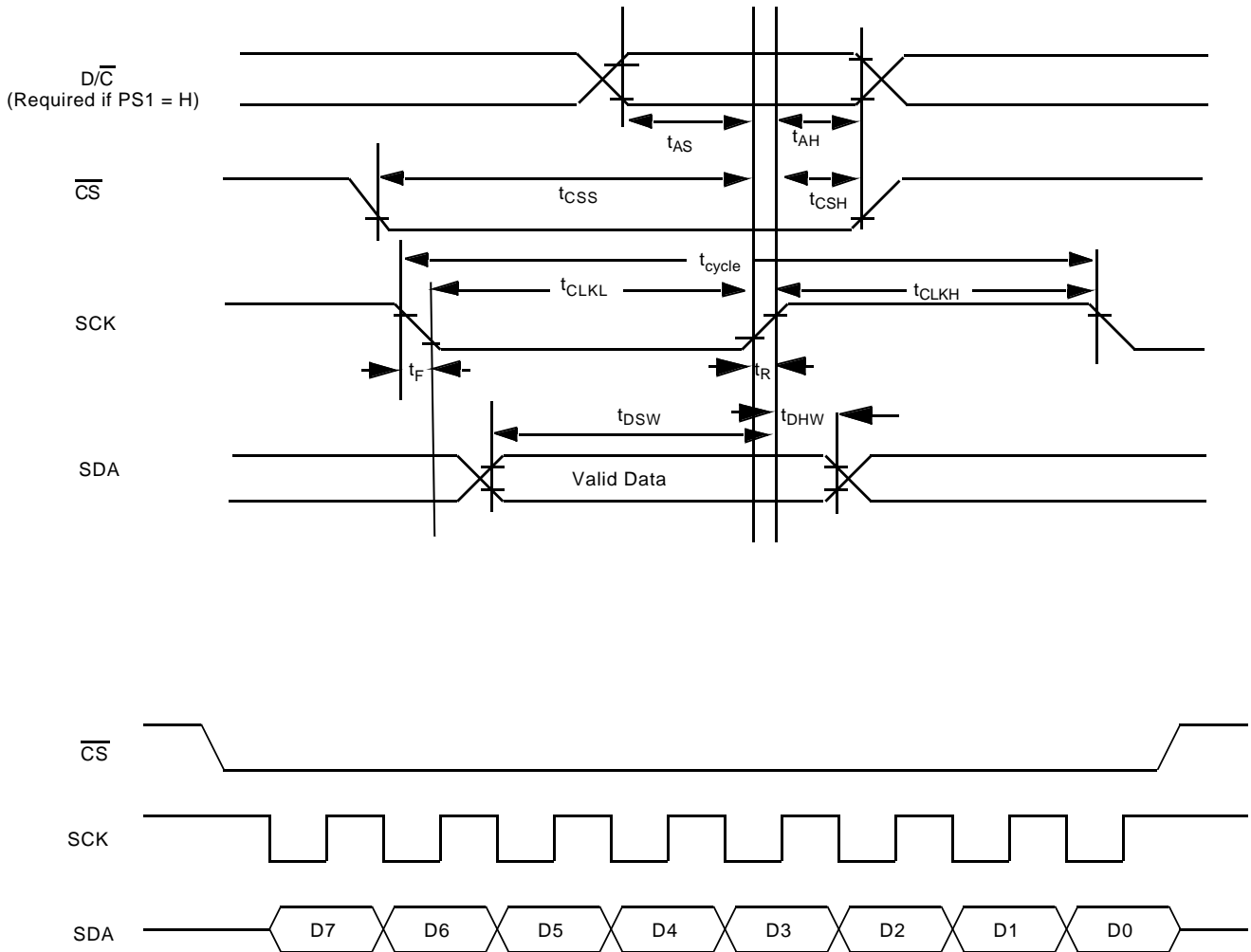


Figure 3a. Serial Timing Characteristics (PS0 = L)

TABLE 5b. Serial Timing Characteristics ($T_A=-40$ to 85°C , $V_{DD}=1.8\text{V}$, $V_{SS}=0\text{V}$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	70	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{CSS}	Chip Select Setup Time	15	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	15	-	-	ns
t_{CLKH}	Clock High Time	30	-	-	ns
t_{R}	Rise Time	-	-	10	ns
t_{F}	Fall Time	-	-	10	ns

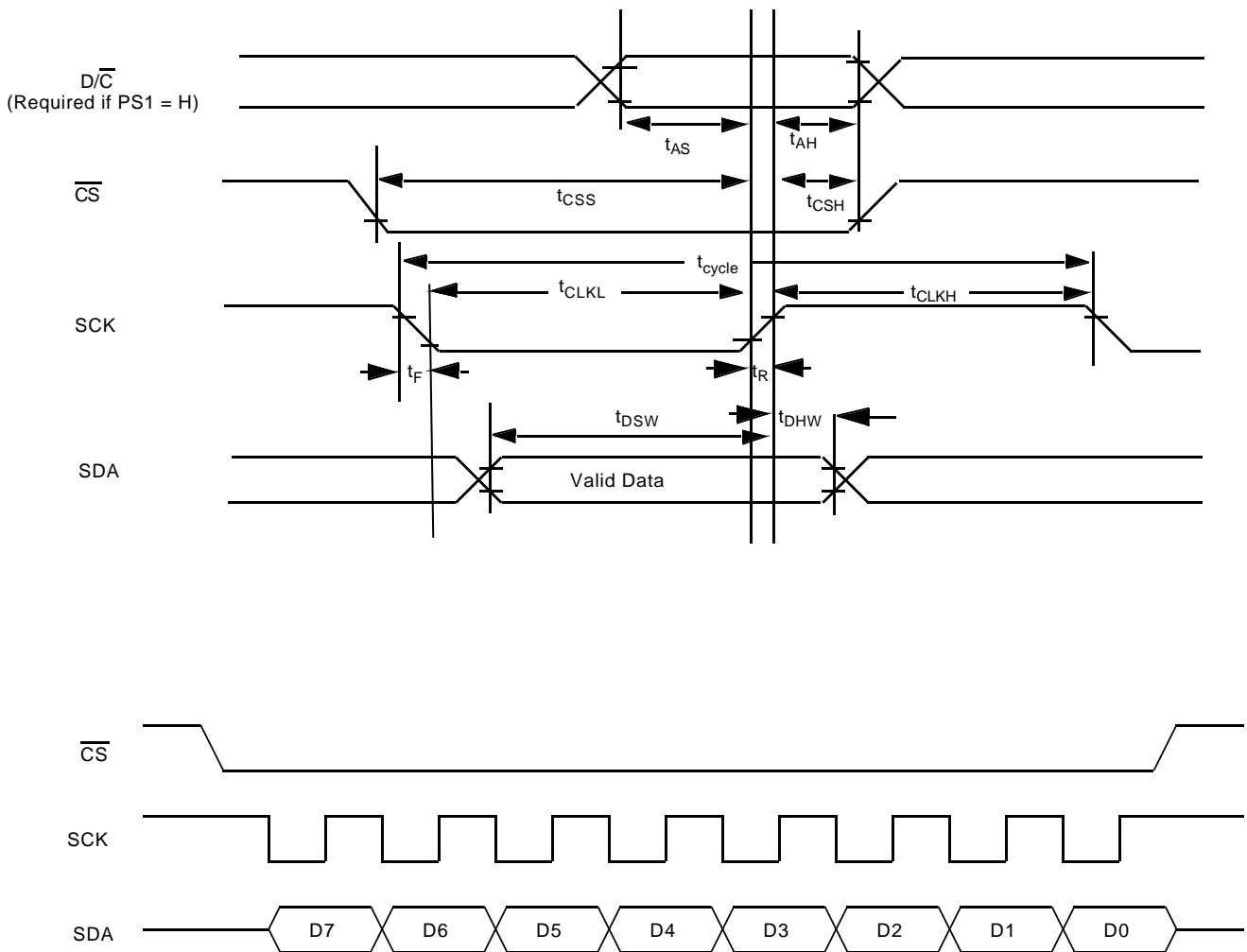
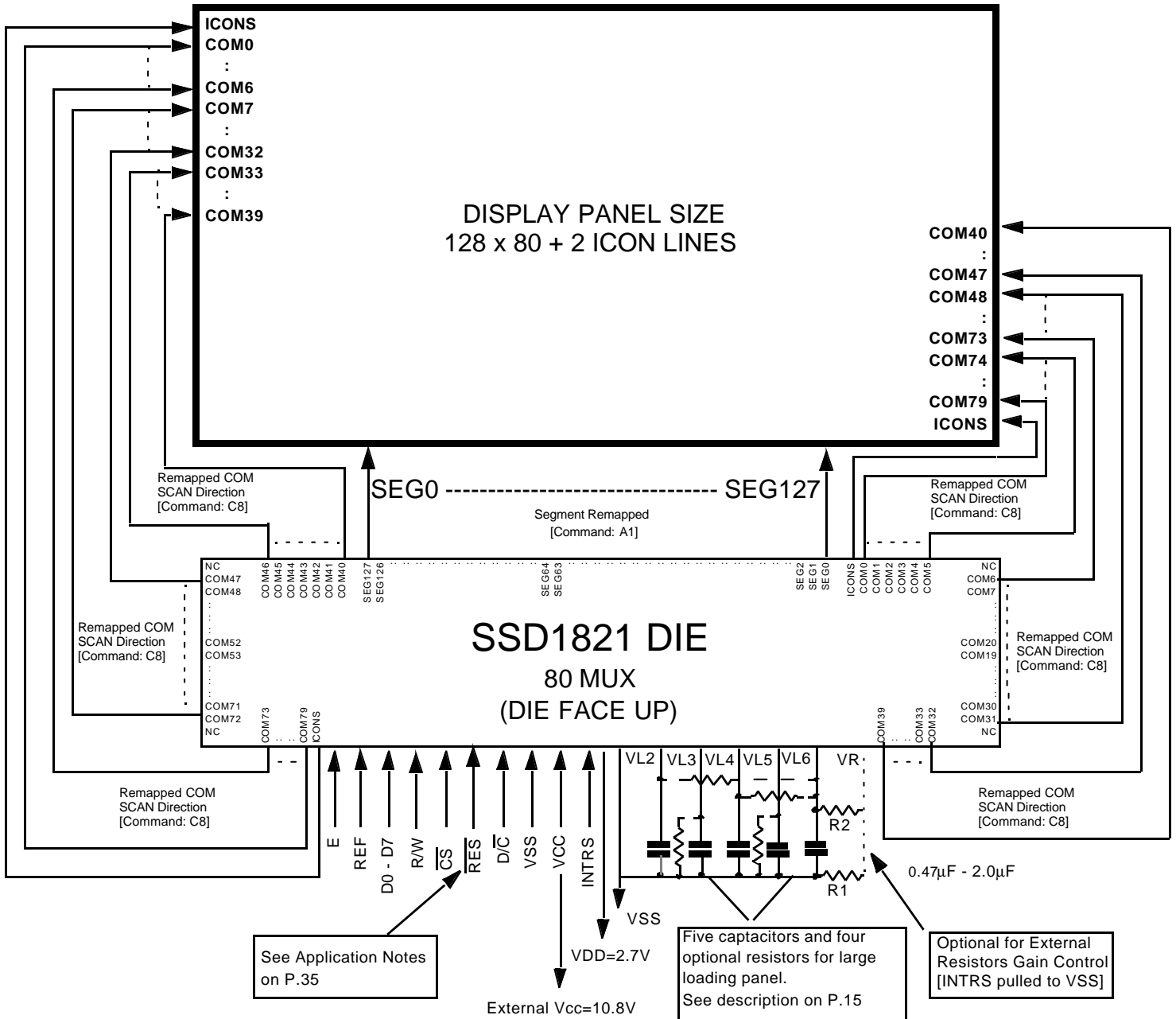


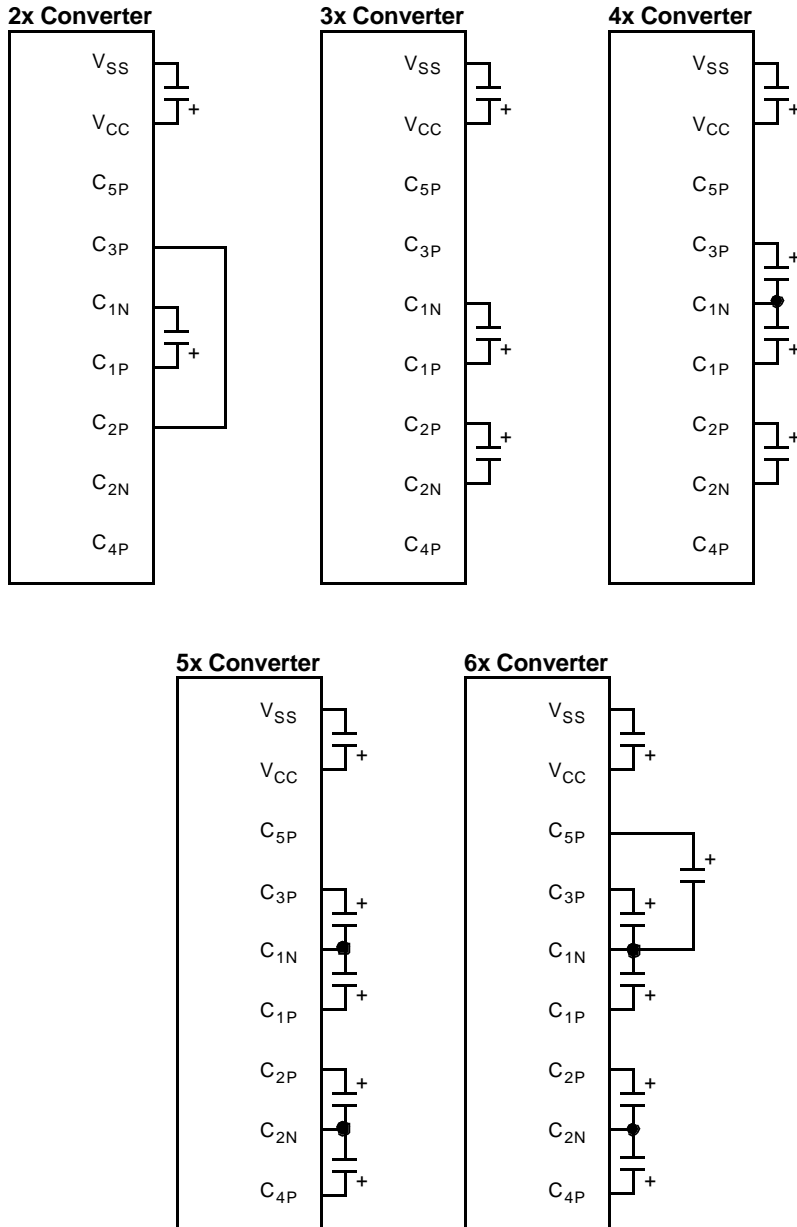
Figure 3b. Serial Timing Characteristics (PS0 = L)

Application Circuit: Bias divider enabled with external V_{CC}.



Application Circuit: DC-DC Converter Circuit Configuration

SSD1820A and SSD1821 IC work from 2X to 5X and 2X to 6X DC-DC converter respectively. For the capacitor connections, please refer to below circuit diagrams. Note that if the capacitor connection does not match with the software setting of DC-DC Converter Factor (0x64~0x67), abnormal current consumption will be observed.



*Note: Capacitor value = 1.0uF to 4.7uF

APPLICATION NOTE 1: ESD PROTECTION CIRCUIT

For SSD1820A/21 IC, it is recommended to design a simple protection circuit to prevent from unexpected external interference. This is useful especially the designed product has to go through unexpected electrostatic discharge. Figure 1 is an example of the common circuit used.

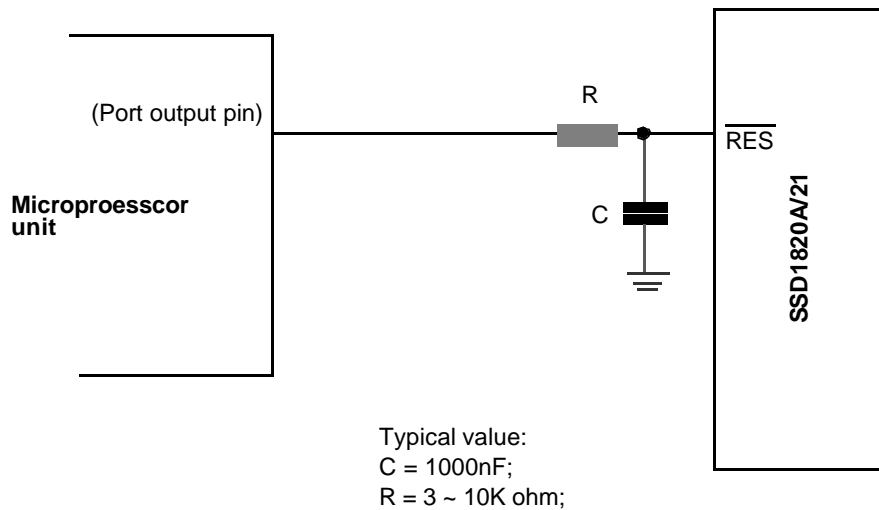


Figure 9: Additional ESD protection circuit

Figure 9 shows one of the most common connection design of the LCD driver IC and the main Microprocessor (MCU) unit, the RES pin of the driver is connected directly to one of the port of the MCU. When external charge is brought near the device, or electrostatic charge (a spike), the charge will be induced inside the device and it will discharge by finding its way to the shortest path to ground.

This discharge sometimes will affect the normal operation of the device, causing data disruption inside RAM or internal registers, or even re-initialize / reset the device. The IC design is in-built with a protection circuit (or a diode circuit to the power and ground rails), to protect the I/O pins from external charge or spike. Since the diode circuit in the IC is very small, the protection of the circuit is limited. Therefore, it is very useful to build an external device to help prevent the disturbance. It is easy to add a capacitor across the RES pin, this will have a big improvement on the stability of the driver IC.

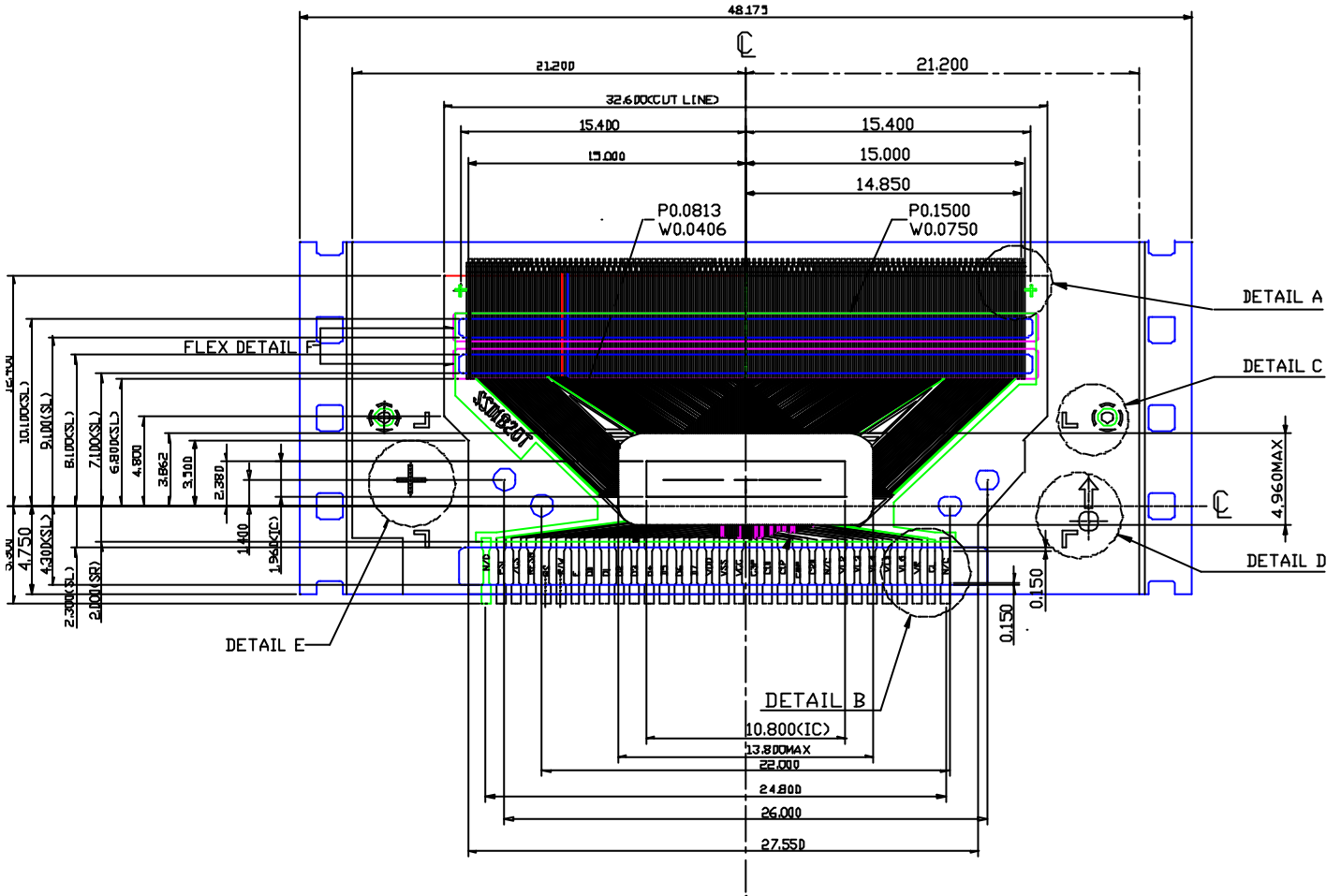
In addition, more protection can be done by adding a resistor in series, directly in between the RES pin of the driver IC and the port of the MCU. This will create a filter (R-C circuit) effect, that will be able to eliminate external noises entering the RES pin of the driver IC.

The value of the capacitor and resistor used largely depend on the application printed circuit board design. It is recommended to test and evaluate to find out the best capacitor value for a particular design application. However, for mobile communication devices (eg mobile phones), a lot of applications there is a 1nF capacitor placed across the RES pin and ground.

SSD1820AT TAB PACKAGE DIMENSION (1 OF 3)

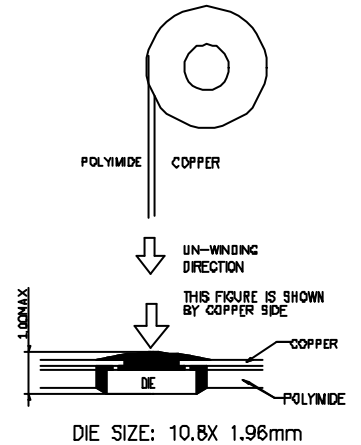
DO NOT SCALE THIS DRAWING

TAPE
UN-WINDING
DIRECTION



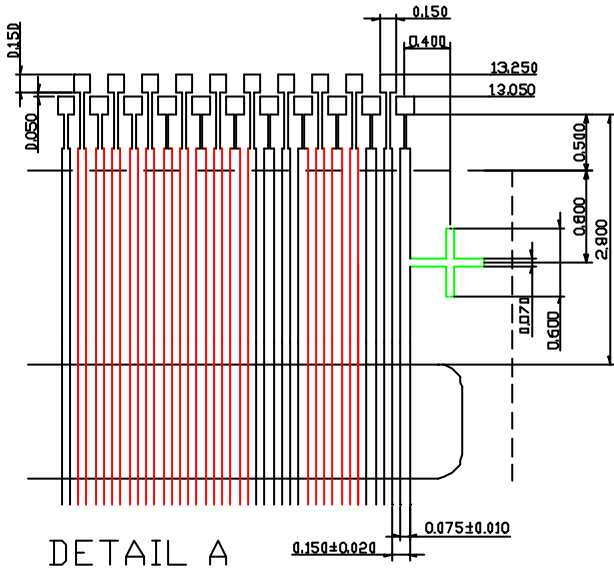
NOTES

1. GENERAL TOLERANCE: $\pm 0.050\text{MM}$
2. ALL CHAMFER IS R0.20
3. MATERIAL
 PI: UPILEX-S 75um+6 THICKNESS
 ADHESIVE: TORAY #7100 12um \pm 2 THICKNESS
 CU: FQ-VLP 18um
 FLEX COATING: FS-100
 SOLDER RESIST: AE-70-M11 26 \pm 14um
4. PLATING
 SN: 0.35 \pm 0.05um
5. OPTIONAL FEATURE FOR SSL EXTERNAL USE ONLY WHICH MAY BE REPLACED BY $\varnothing 2.0\text{MM}$ HOLE
6. 4 SPROCKET HOLES (19.00mm) FOR 1 TAPE

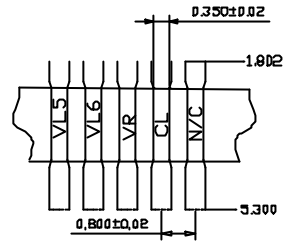


SSD1820AT TAB PACKAGE DIMENSION (2 OF 3)

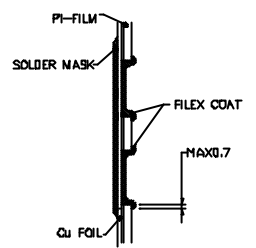
DO NOT SCALE THIS DRAWING



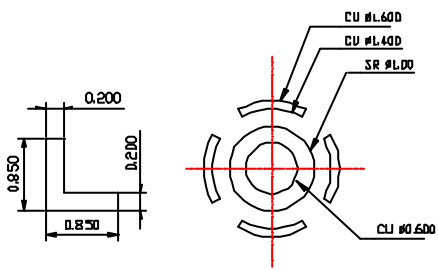
DETAIL A



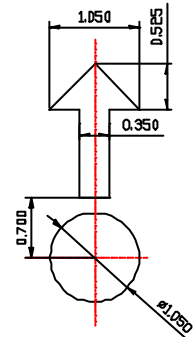
DETAIL B



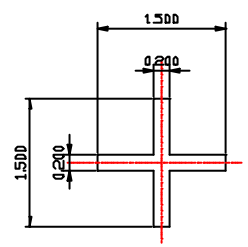
DETAIL F - FLEX



DETAIL C



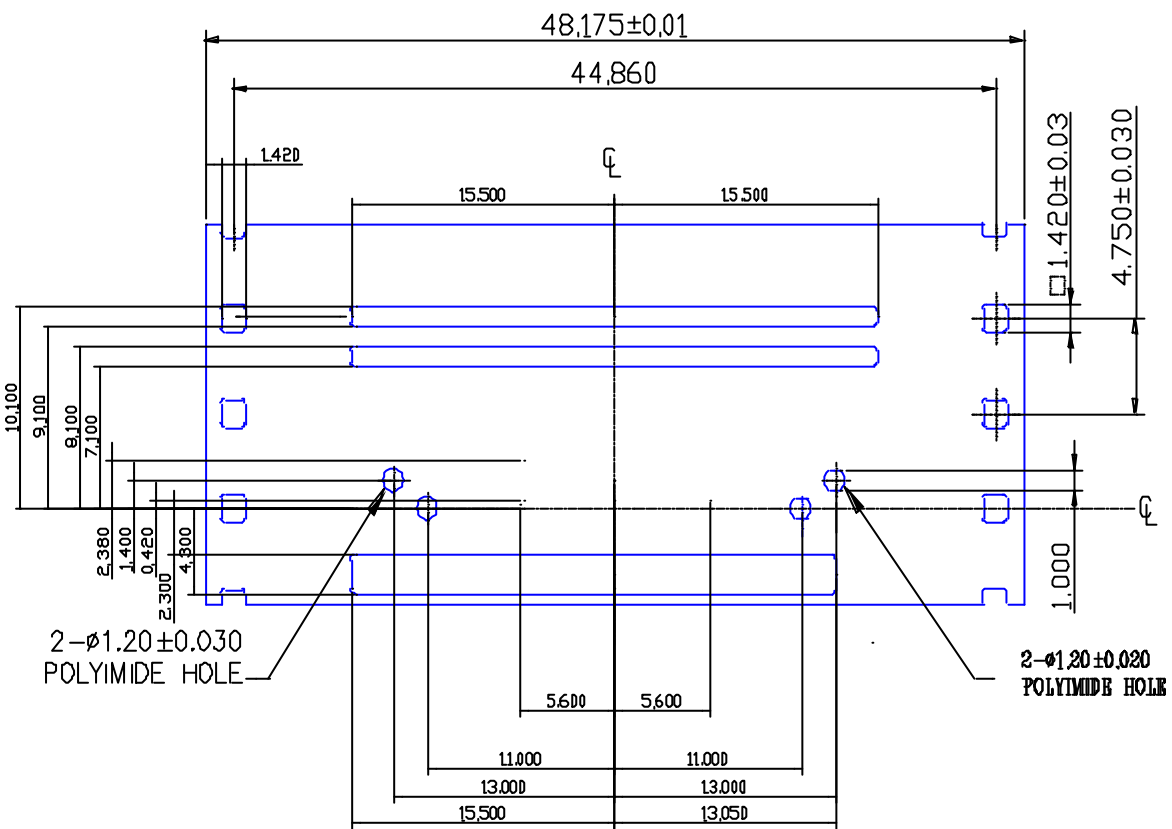
DETAIL D



DETAIL E

SSD1820AT TAB PACKAGE DIMENSION (3 OF 3)

DO NOT SCALE THIS DRAWING



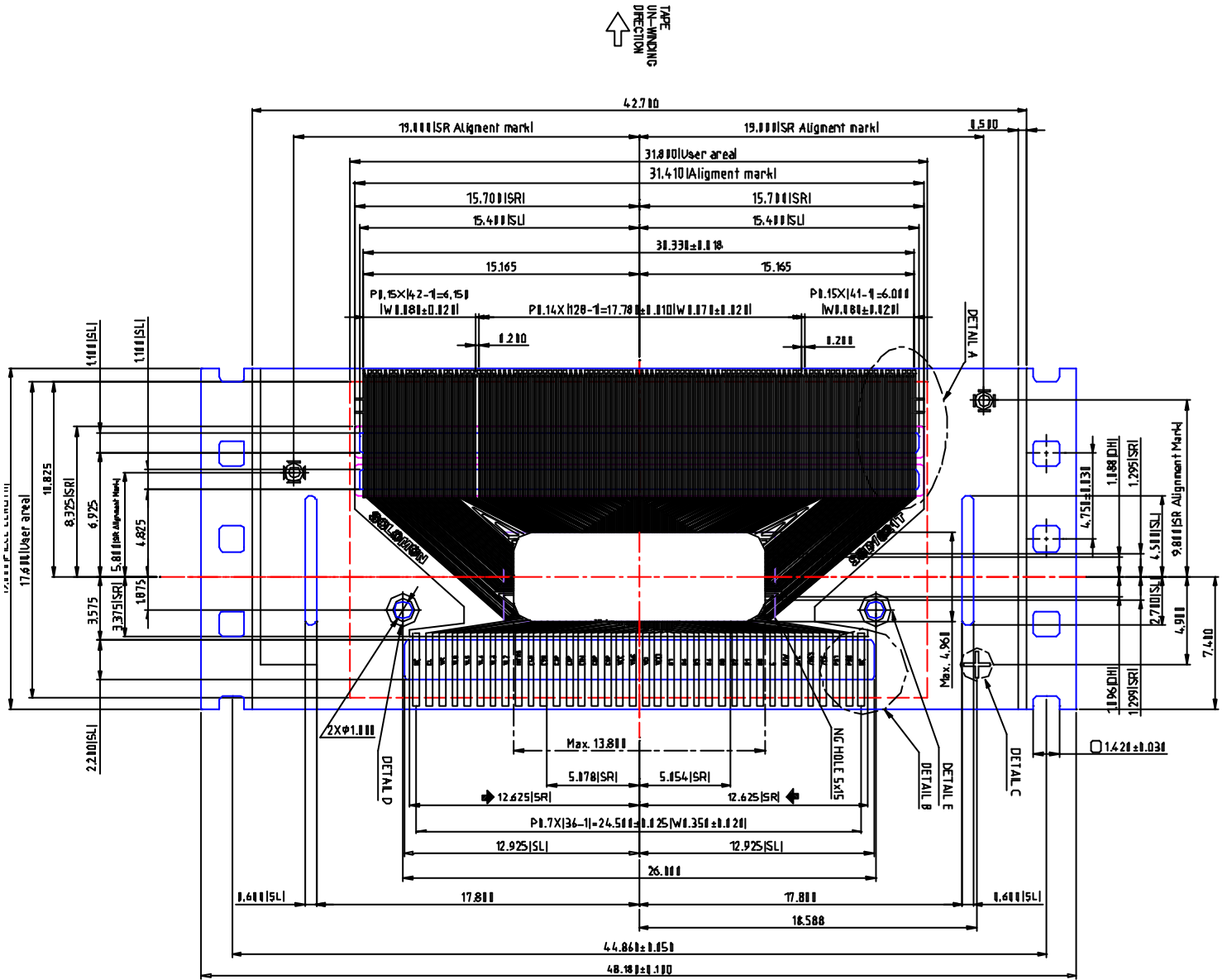
COPPER VIEW

MATERIAL	IMPLEMENTS	PT. FILM	7.5um	+6um
YES	Adhesive	12um	+2um	
NO	PREPARED	20um		
HOLE	HOLE DIMENSION	NUMBER		
	1.420X1.420	8		
	31.000X1.000	2		
	11.200X2.360	1		
	29.550X2.000	1		
CIRCLE	Ø1.200	4		
ELLIPSE				

ALL OTHER CHAMFER IS R0.200
GENERAL TOLERANCE ±0.05

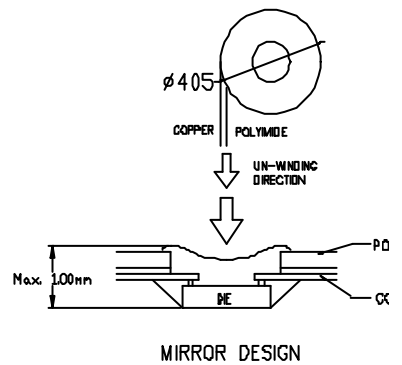
SSD1821T TAB PACKAGE DIMENSION (1 OF 3)

DO NOT SCALE THIS DRAWING



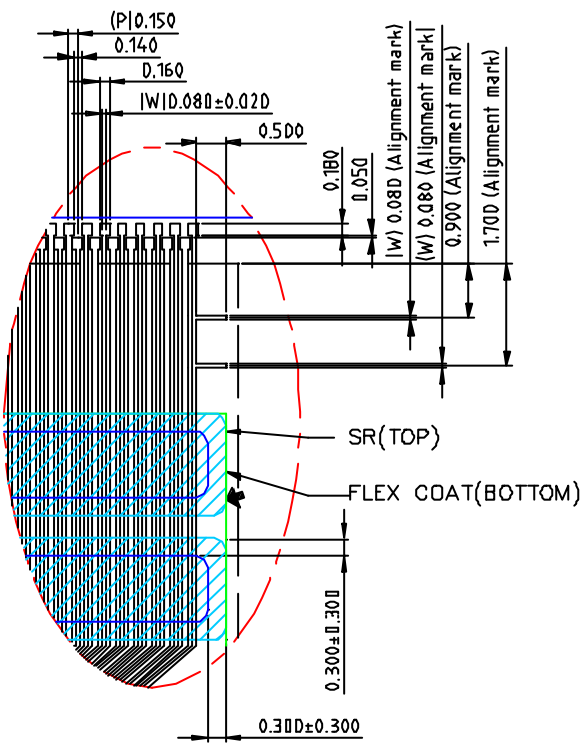
NOTES

1. GENERAL TOLERANCE: $\pm 0.050\text{MM}$
2. ALL CHAMFER IS R0.20
3. MATERIAL
 PI: UPILEX-S 75um+6 THICKNESS
 ADHESIVE: TORAY #7100 $12 \pm 2\text{um}$ THICKNESS
 CU: FQ-VLP 25um $\pm 5\text{um}$
 FLEX COATING: FS-100L
 SOLDER RESIST: AR-7100 $26 \pm 14\text{um}$
 GENERAL TOLERANCE $\pm 0.300\text{mm}$
4. PLATING SN: $0.35 \pm 0.05\text{um}$ ($0.2 \pm 0.05\text{um}$ PURE TIN)
5. OPTIONAL FEATURE FOR SSL EXTERNAL USE ONLY WHICH MAY BE REPLACED BY $\varnothing 2.0\text{MM}$ HOLE
6. 4 SPROCKET HOLES (19.00mm) FOR 1 TAPE

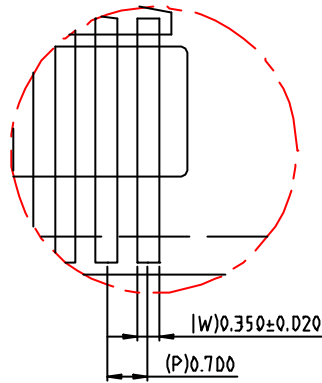


SSD1821T TAB PACKAGE DIMENSION (2 OF 3)

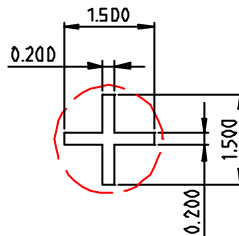
DO NOT SCALE THIS DRAWING



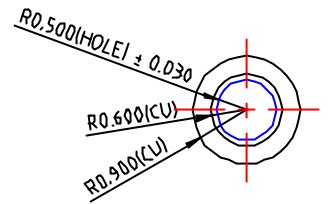
DETAIL A



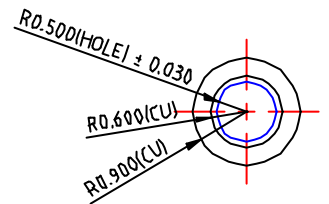
DETAIL B



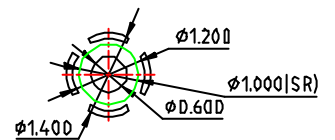
DETAIL C



DETAIL D



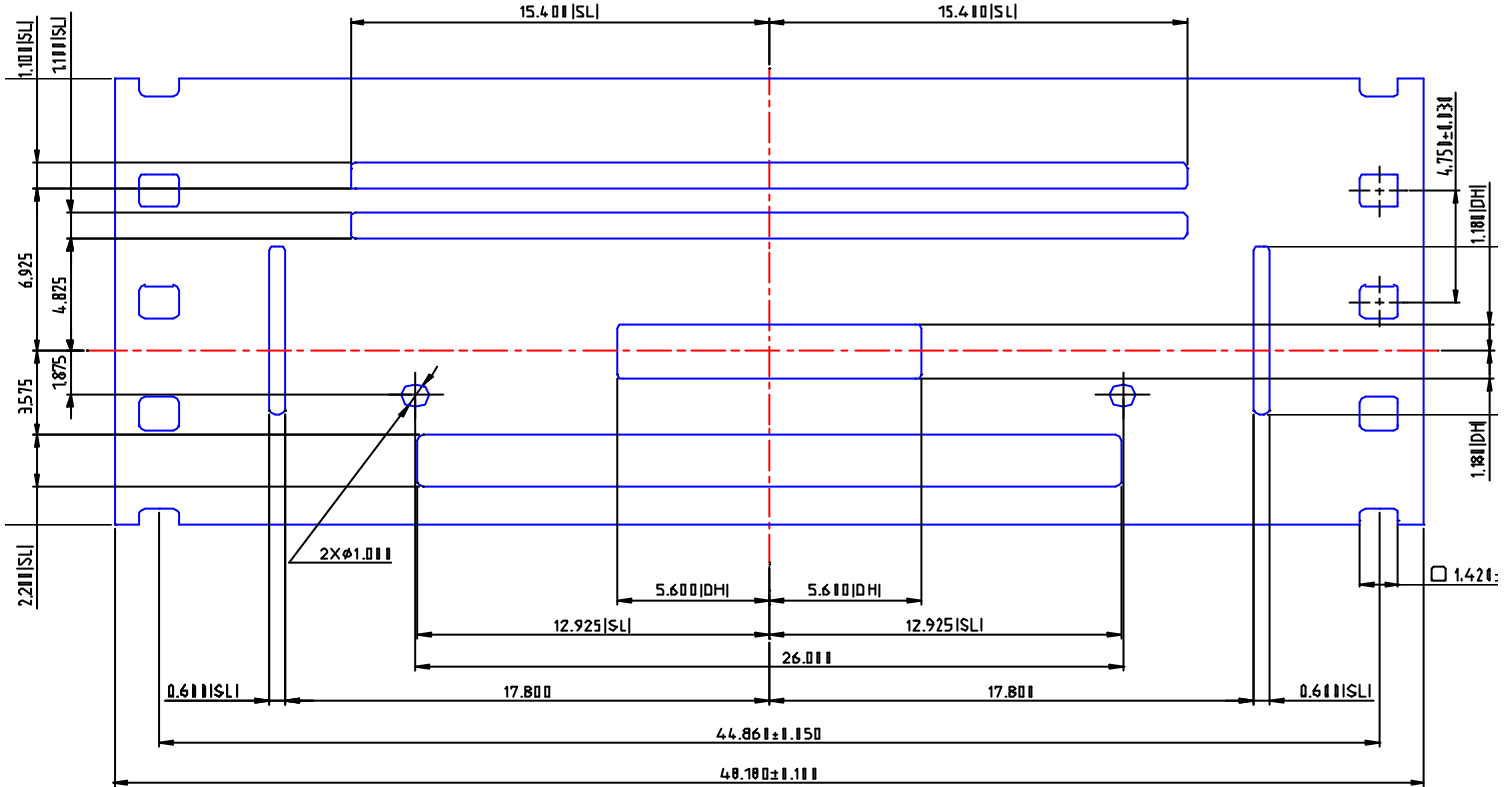
DETAIL E



S/R ALIGNMENT MARK

SSD1821T TAB PACKAGE DIMENSION (3 OF 3)

DO NOT SCALE THIS DRAWING



COPPER VIEW

MATERIAL	UPILEX-S	HARD TOOL	YES
PI FILM	75UM±6UM		NO
ADHESIVE	12UN±2UN(TORAY#7100)	PROTECT FILM	20UM
HOLE	HOLE NUMBER	NUMBER	
SQUARE	1.420x1.420	8	
	1.100x30.800	2	
	7.200x0.600	2	
	2.200x25.850	1	
	2.360x11.200	1	
CIRCLE	φ1.000	2	
ELLIPSE			

ALL OTHER CHAMFER IS R0.200mm
GENERAL TOLERANCE ±0.050mm

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