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SSD1870

Advance Information

SSD1870 MLA COLUMN (SEGMENT) DRIVER
CMOS

1. GENERAL DESCRIPTION

SSD1870 is an MLA (Multi Line Addressing) segment driver with 160 five-level outputs. SSD1870 can be used with row (common) driver SSD1881/1882 and MLA power chip SSD1730 to form an LCD display system which produce high speed and good contrast display quality. Besides, the power consumption of an MLA display system is lower than the display system using conventional driving method.

The SSD1870 has an on-chip 160 x 240 bits display RAM supporting maximum upto 240 MUX. With cascade configuration, higher display resolution can be produced. The driver stores display data in the display RAM and generates LCD driving signals. The display data transmission from the controller can be suspended when there is no change in the display, thereby enabling an ultra low power display system.

2. FEATURES

Power supply to logic system, 3.0V - 3.6V
Power supply to LCD system, 6.0V - 7.2V (referenced to VDD_COL)
Four line MLA driving
160 segment outputs
Maximum 240 Mux ratio
On chip 160 x 240 bit display RAM
4-bit / 8-bit display data input
Non-biased display off function
Output shift direction pin select supported
Cascade supported
Halt Write Function to save power consumption
Available in TAB (Tape Automated Bonding) Package

3. ORDERING INFORMATION

Table 1 - Ordering Information

Ordering Part Number	Output lead pitch (mm)	Package Form
SSD1870TZ	-	Gold Bump Die
SSD1870TR	0.16	TAB
SSD1870T1R1	0.14	TAB
SSD1870T2R	0.22	TAB

4. BLOCK DIAGRAM

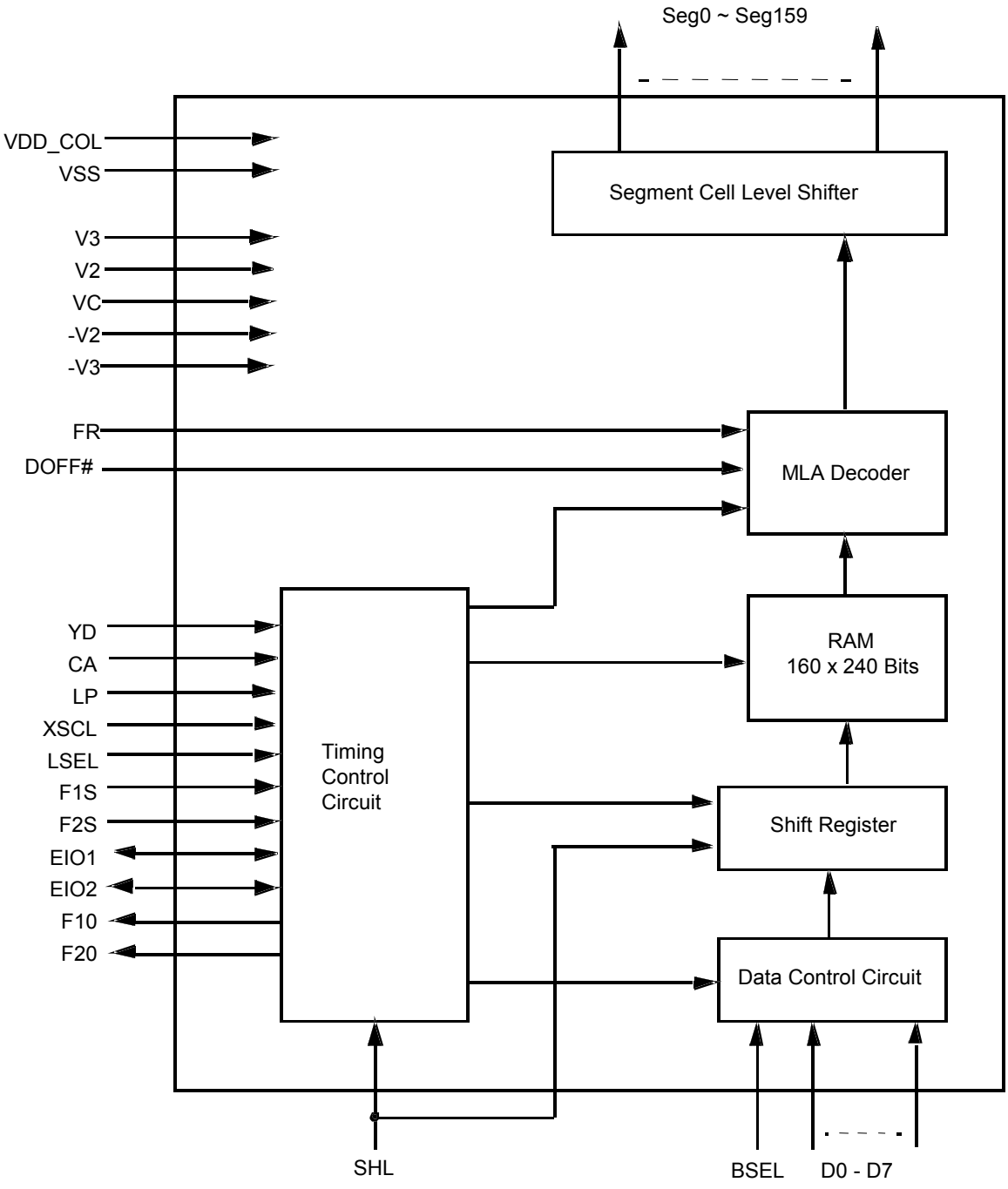
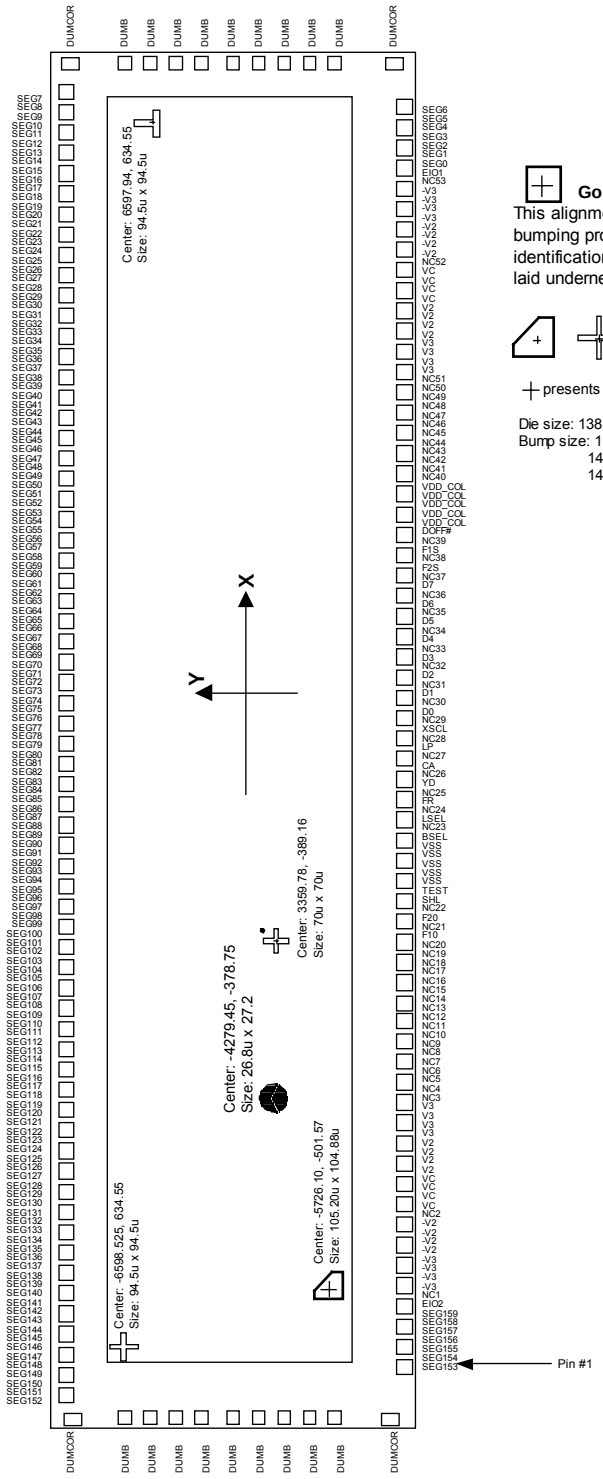


Figure 1 - Block Diagram

5. SSD1870Z DIE PAD ARRANGEMENT



Gold Bump Alignment Mark
This alignment mark contains gold nump for IC bumping process alignment and IC identifications. No conductive tracks should be laid underneath this mark to avoid short circuit.

presents the centre of the alignment mark

Die size: 13810um x 1963.3um
Bump size: 1 to 141, 153 to 298 -- 60.2um x 60.2um
142, 152, 299, 309 -- 42um x 60.2um
143 to 151, 300 to 309 -- 42 um x 42um

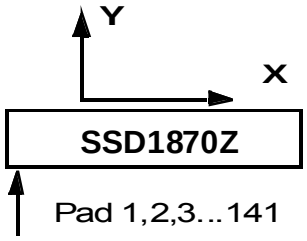
Figure 2 – SSD1870Z Die Pad Assignment

Table 2 - SSD1870Z Die Pad Coordinate

Pad #	Signal	X-pos	Y-pos
1	SEG153	-6459.80	-799.45
2	SEG154	-6370.70	-799.45
3	SEG155	-6281.60	-799.45
4	SEG156	-6192.50	-799.45
5	SEG157	-6103.40	-799.45
6	SEG158	-6014.30	-799.45
7	SEG159	-5925.20	-799.45
8	EIO2	-5613.30	-820.85
9	NC1	-5524.20	-820.85
10	-V3	-5435.10	-820.85
11	-V3	-5346.00	-820.85
12	-V3	-5256.90	-820.85
13	-V3	-5167.80	-820.85
14	-V2	-5078.70	-820.85
15	-V2	-4989.60	-820.85
16	-V2	-4900.50	-820.85
17	-V2	-4811.40	-820.85
18	NC2	-4722.30	-820.85
19	VC	-4633.20	-820.85
20	VC	-4544.10	-820.85
21	VC	-4455.00	-820.85
22	VC	-4365.90	-820.85
23	V2	-4276.80	-820.85
24	V2	-4187.70	-820.85
25	V2	-4098.60	-820.85
26	V2	-4009.50	-820.85
27	V3	-3920.40	-820.85
28	V3	-3831.30	-820.85
29	V3	-3742.20	-820.85
30	V3	-3653.10	-820.85
31	NC3	-3564.00	-820.85
32	NC4	-3474.90	-820.85
33	NC5	-3385.80	-820.85
34	NC6	-3296.70	-820.85
35	NC7	-3207.60	-820.85
36	NC8	-3118.50	-820.85
37	NC9	-3029.40	-820.85
38	NC10	-2940.30	-820.85
39	NC11	-2851.20	-820.85
40	NC12	-2762.10	-820.85
41	NC13	-2673.00	-820.85
42	NC14	-2583.90	-820.85
43	NC15	-2494.80	-820.85
44	NC16	-2405.70	-820.85
45	NC17	-2316.60	-820.85
46	NC18	-2227.50	-820.85
47	NC19	-2138.40	-820.85
48	NC20	-2049.30	-820.85
49	F10	-1960.20	-820.85
50	NC21	-1871.10	-820.85
51	F20	-1782.00	-820.85
52	NC22	-1692.90	-820.85
53	SHL	-1603.80	-820.85
54	TEST	-1514.70	-820.85
55	VSS	-1425.60	-820.85
56	VSS	-1336.50	-820.85
57	VSS	-1247.40	-820.85
58	VSS	-1158.30	-820.85
59	VSS	-1069.20	-820.85
60	BSEL	-980.10	-820.85
61	NC23	-891.00	-820.85
62	LSEL	-801.90	-820.85
63	NC24	-712.80	-820.85
64	FR	-623.70	-820.85
65	NC25	-534.60	-820.85
66	YD	-445.50	-820.85
67	NC26	-356.40	-820.85
68	CA	-267.30	-820.85
69	NC27	-178.20	-820.85
70	LP	-89.10	-820.85
71	NC28	0.00	-820.85
72	XSCL	89.10	-820.85
73	NC29	178.20	-820.85
74	D0	267.30	-820.85
75	NC30	356.40	-820.85
76	D1	445.50	-820.85
77	NC31	534.60	-820.85
78	D2	623.70	-820.85
79	NC32	712.80	-820.85
80	D3	801.90	-820.85
81	NC33	891.00	-820.85
82	D4	980.10	-820.85
83	NC34	1069.20	-820.85
84	D5	1158.30	-820.85
85	NC35	1247.40	-820.85
86	D6	1336.50	-820.85
87	NC36	1425.60	-820.85
88	D7	1514.70	-820.85
89	NC37	1603.80	-820.85
90	F2S	1692.90	-820.85
91	NC38	1782.00	-820.85
92	F1S	1871.10	-820.85
93	NC39	1960.20	-820.85
94	DOFF#	2049.30	-820.85
95	VDD_COL	2138.40	-820.85
96	VDD_COL	2227.50	-820.85
97	VDD_COL	2316.60	-820.85
98	VDD_COL	2405.70	-820.85
99	VDD_COL	2494.80	-820.85
100	NC40	2583.90	-820.85
101	NC41	2673.00	-820.85
102	NC42	2762.10	-820.85
103	NC43	2851.20	-820.85
104	NC44	2940.30	-820.85
105	NC45	3029.40	-820.85
106	NC46	3118.50	-820.85
107	NC47	3207.60	-820.85
108	NC48	3296.70	-820.85
109	NC49	3385.80	-820.85
110	NC50	3474.90	-820.85
111	NC51	3564.00	-820.85
112	V3	3653.10	-820.85
113	V3	3742.20	-820.85
114	V3	3831.30	-820.85
115	V3	3920.40	-820.85
116	V2	4009.50	-820.85
117	V2	4098.60	-820.85
118	V2	4187.70	-820.85
119	V2	4276.80	-820.85
120	VC	4365.90	-820.85
121	VC	4455.00	-820.85
122	VC	4544.10	-820.85
123	VC	4633.20	-820.85
124	NC52	4722.30	-820.85
125	-V2	4811.40	-820.85
126	-V2	4900.50	-820.85
127	-V2	4989.60	-820.85
128	-V2	5078.70	-820.85
129	-V3	5167.80	-820.85
130	-V3	5256.90	-820.85
131	-V3	5346.00	-820.85
132	-V3	5435.10	-820.85
133	NC53	5524.20	-820.85
134	EIO1	5613.30	-820.85
135	SEG0	5925.10	-799.45
136	SEG1	6014.20	-799.45
137	SEG2	6103.30	-799.45
138	SEG3	6192.40	-799.45
139	SEG4	6281.50	-799.45
140	SEG5	6370.60	-799.45
141	SEG6	6459.70	-799.45
142	DUMCOR1	6773.85	-799.45
143	NC54	6773.85	-337.05
144	NC55	6773.85	-247.95
145	NC56	6773.85	-158.85
146	NC57	6773.85	-69.75
147	NC58	6773.85	19.35
148	NC59	6773.85	108.45
149	NC60	6773.85	197.55
150	NC61	6773.85	286.65
151	NC62	6773.85	375.75
152	DUMCOR2	6773.85	799.45
153	SEG7	6459.70	799.45
154	SEG8	6370.60	799.45
155	SEG9	6281.50	799.45
156	SEG10	6192.40	799.45
157	SEG11	6103.30	799.45
158	SEG12	6014.20	799.45
159	SEG13	5925.10	799.45
160	SEG14	5836.00	799.45
161	SEG15	5746.90	799.45
162	SEG16	5657.80	799.45
163	SEG17	5568.70	799.45
164	SEG18	5479.60	799.45
165	SEG19	5390.50	799.45
166	SEG20	5301.40	799.45
167	SEG21	5212.30	799.45
168	SEG22	5123.20	799.45
169	SEG23	5034.10	799.45
170	SEG24	4945.00	799.45
171	SEG25	4855.90	799.45
172	SEG26	4766.80	799.45
173	SEG27	4677.70	799.45
174	SEG28	4588.60	799.45
175	SEG29	4499.50	799.45
176	SEG30	4410.40	799.45
177	SEG31	4321.30	799.45
178	SEG32	4232.20	799.45
179	SEG33	4143.10	799.45
180	SEG34	4054.00	799.45
181	SEG35	3964.90	799.45
182	SEG36	3875.80	799.45
183	SEG37	3786.70	799.45
184	SEG38	3697.60	799.45
185	SEG39	3608.50	799.45
186	SEG40	3519.40	799.45

Pad #	Signal	X-pos	Y-pos
187	SEG41	3430.30	799.45
188	SEG42	3341.20	799.45
189	SEG43	3252.10	799.45
190	SEG44	3163.00	799.45
191	SEG45	3073.90	799.45
192	SEG46	2984.80	799.45
193	SEG47	2895.70	799.45
194	SEG48	2806.60	799.45
195	SEG49	2717.50	799.45
196	SEG50	2628.40	799.45
197	SEG51	2539.30	799.45
198	SEG52	2450.20	799.45
199	SEG53	2361.10	799.45
200	SEG54	2272.00	799.45
201	SEG55	2182.90	799.45
202	SEG56	2093.80	799.45
203	SEG57	2004.70	799.45
204	SEG58	1915.60	799.45
205	SEG59	1826.50	799.45
206	SEG60	1737.40	799.45
207	SEG61	1648.30	799.45
208	SEG62	1559.20	799.45
209	SEG63	1470.10	799.45
210	SEG64	1381.00	799.45
211	SEG65	1291.90	799.45
212	SEG66	1202.80	799.45
213	SEG67	1113.70	799.45
214	SEG68	1024.60	799.45
215	SEG69	935.50	799.45
216	SEG70	846.40	799.45
217	SEG71	757.30	799.45
218	SEG72	668.20	799.45
219	SEG73	579.10	799.45
220	SEG74	490.00	799.45
221	SEG75	400.90	799.45
222	SEG76	311.80	799.45
223	SEG77	222.70	799.45
224	SEG78	133.60	799.45
225	SEG79	44.50	799.45
226	SEG80	-44.60	799.45
227	SEG81	-133.70	799.45
228	SEG82	-222.80	799.45
229	SEG83	-311.90	799.45
230	SEG84	-401.00	799.45
231	SEG85	-490.10	799.45
232	SEG86	-579.20	799.45
233	SEG87	-668.30	799.45
234	SEG88	-757.40	799.45
235	SEG89	-846.50	799.45
236	SEG90	-935.60	799.45
237	SEG91	-1024.70	799.45
238	SEG92	-1113.80	799.45
239	SEG93	-1202.90	799.45
240	SEG94	-1292.00	799.45
241	SEG95	-1381.10	799.45
242	SEG96	-1470.20	799.45
243	SEG97	-1559.30	799.45
244	SEG98	-1648.40	799.45
245	SEG99	-1737.50	799.45
246	SEG100	-1826.60	799.45
247	SEG101	-1915.70	799.45
248	SEG102	-2004.80	799.45

Pad #	Signal	X-pos	Y-pos
249	SEG103	-2093.90	799.45
250	SEG104	-2183.00	799.45
251	SEG105	-2272.10	799.45
252	SEG106	-2361.20	799.45
253	SEG107	-2450.30	799.45
254	SEG108	-2539.40	799.45
255	SEG109	-2628.50	799.45
256	SEG110	-2717.60	799.45
257	SEG111	-2806.70	799.45
258	SEG112	-2895.80	799.45
259	SEG113	-2984.90	799.45
260	SEG114	-3074.00	799.45
261	SEG115	-3163.10	799.45
262	SEG116	-3252.20	799.45
263	SEG117	-3341.30	799.45
264	SEG118	-3430.40	799.45
265	SEG119	-3519.50	799.45
266	SEG120	-3608.60	799.45
267	SEG121	-3697.70	799.45
268	SEG122	-3786.80	799.45
269	SEG123	-3875.90	799.45
270	SEG124	-3965.00	799.45
271	SEG125	-4054.10	799.45
272	SEG126	-4143.20	799.45
273	SEG127	-4232.30	799.45
274	SEG128	-4321.40	799.45
275	SEG129	-4410.50	799.45
276	SEG130	-4499.60	799.45
277	SEG131	-4588.70	799.45
278	SEG132	-4677.80	799.45
279	SEG133	-4766.90	799.45
280	SEG134	-4856.00	799.45
281	SEG135	-4945.10	799.45
282	SEG136	-5034.20	799.45
283	SEG137	-5123.30	799.45
284	SEG138	-5212.40	799.45
285	SEG139	-5301.50	799.45
286	SEG140	-5390.60	799.45
287	SEG141	-5479.70	799.45
288	SEG142	-5568.80	799.45
289	SEG143	-5657.90	799.45
290	SEG144	-5747.00	799.45
291	SEG145	-5836.10	799.45
292	SEG146	-5925.20	799.45
293	SEG147	-6014.30	799.45
294	SEG148	-6103.40	799.45
295	SEG149	-6192.50	799.45
296	SEG150	-6281.60	799.45
297	SEG151	-6370.70	799.45
298	SEG152	-6459.80	799.45
299	DUMCOR3	-6773.85	799.45
300	NC63	-6773.85	375.75
301	NC64	-6773.85	286.65
302	NC65	-6773.85	197.55
303	NC66	-6773.85	108.45
304	NC67	-6773.85	19.35
305	NC68	-6773.85	-69.75
306	NC69	-6773.85	-158.85
307	NC70	-6773.85	-247.95
308	NC71	-6773.85	-337.05
309	DUMCOR4	-6773.85	-799.45



Gold Bumps face up

6. SSD1870TR TAB PIN ASSIGNMENT

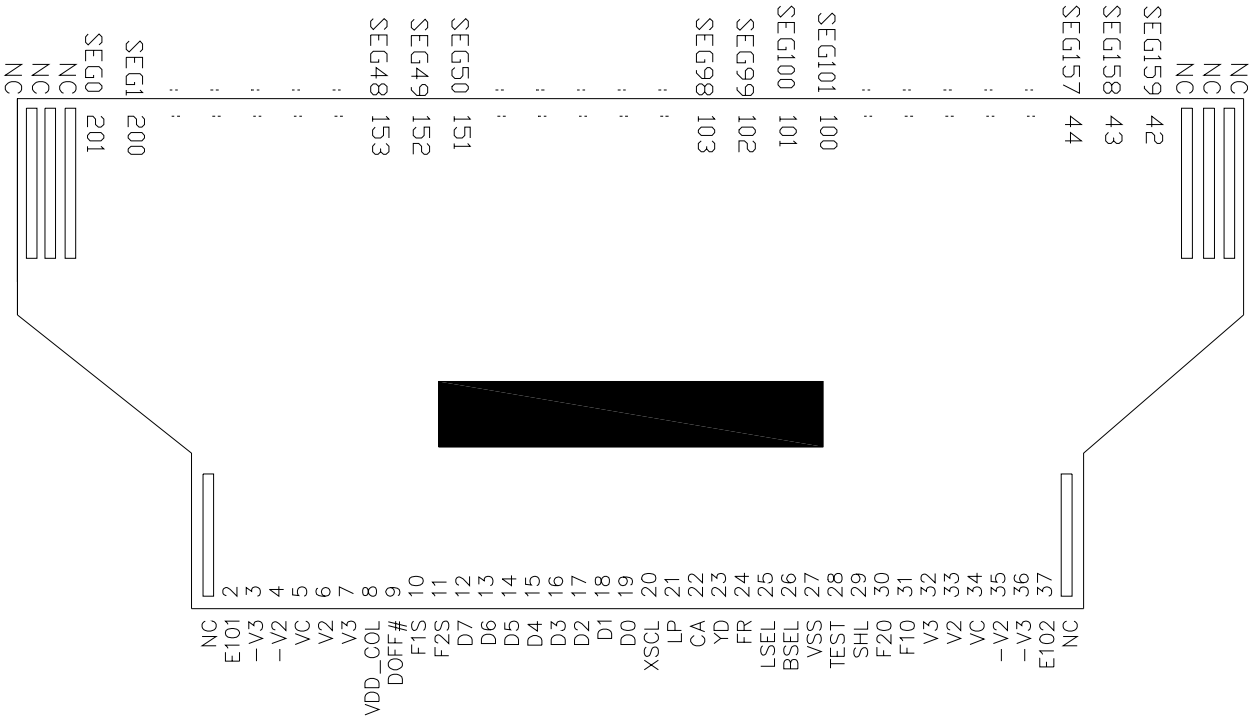
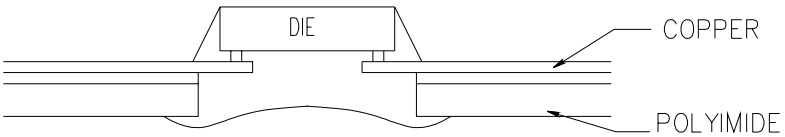


Figure 3 – SSD1870TR TAB Pin Assignment (Copper View, Mirror TAB Design)



MIRROR DESIGN

Table 3 - SSD1870TR Pin Assignment

Pin#	Pin Name
1	NC
2	EIO1
3	-V3
4	-V2
5	VC
6	V2
7	V3
8	VDD_COL
9	DOFF#
10	F1S
11	F2S
12	D7
13	D6
14	D5
15	D4
16	D3
17	D2
18	D1
19	D0
20	XSCL
21	LP
22	CA
23	YD
24	FR
25	LSEL
26	BSEL
27	VSS
28	TEST
29	SHL
30	F20
31	F10
32	V3
33	V2
34	VC
35	-V2
36	-V3
37	EIO2
38	NC
39	NC
40	NC
41	NC
42	SEG159
43	SEG158
44	SEG157
45	SEG156
46	SEG155
47	SEG154
48	SEG153
49	SEG152
50	SEG151
51	SEG150
52	SEG149
53	SEG148
54	SEG147
55	SEG146
56	SEG145
57	SEG144
58	SEG143
59	SEG142
60	SEG141

Pin#	Pin Name
61	SEG140
62	SEG139
63	SEG138
64	SEG137
65	SEG136
66	SEG135
67	SEG134
68	SEG133
69	SEG132
70	SEG131
71	SEG130
72	SEG129
73	SEG128
74	SEG127
75	SEG126
76	SEG125
77	SEG124
78	SEG123
79	SEG122
80	SEG121
81	SEG120
82	SEG119
83	SEG118
84	SEG117
85	SEG116
86	SEG115
87	SEG114
88	SEG113
89	SEG112
90	SEG111
91	SEG110
92	SEG109
93	SEG108
94	SEG107
95	SEG106
96	SEG105
97	SEG104
98	SEG103
99	SEG102
100	SEG101
101	SEG100
102	SEG99
103	SEG98
104	SEG97
105	SEG96
106	SEG95
107	SEG94
108	SEG93
109	SEG92
110	SEG91
111	SEG90
112	SEG89
113	SEG88
114	SEG87
115	SEG86
116	SEG85
117	SEG84
118	SEG83
119	SEG82
120	SEG81

Pin#	Pin Name
121	SEG80
122	SEG79
123	SEG78
124	SEG77
125	SEG76
126	SEG75
127	SEG74
128	SEG73
129	SEG72
130	SEG71
131	SEG70
132	SEG69
133	SEG68
134	SEG67
135	SEG66
136	SEG65
137	SEG64
138	SEG63
139	SEG62
140	SEG61
141	SEG60
142	SEG59
143	SEG58
144	SEG57
145	SEG56
146	SEG55
147	SEG54
148	SEG53
149	SEG52
150	SEG51
151	SEG50
152	SEG49
153	SEG48
154	SEG47
155	SEG46
156	SEG45
157	SEG44
158	SEG43
159	SEG42
160	SEG41
161	SEG40
162	SEG39
163	SEG38
164	SEG37
165	SEG36
166	SEG35
167	SEG34
168	SEG33
169	SEG32
170	SEG31
171	SEG30
172	SEG29
173	SEG28
174	SEG27
175	SEG26
176	SEG25
177	SEG24
178	SEG23
179	SEG22
180	SEG21

Pin#	Pin Name
181	SEG20
182	SEG19
183	SEG18
184	SEG17
185	SEG16
186	SEG15
187	SEG14
188	SEG13
189	SEG12
190	SEG11
191	SEG10
192	SEG9
193	SEG8
194	SEG7
195	SEG6
196	SEG5
197	SEG4
198	SEG3
199	SEG2
200	SEG1
201	SEG0
202	NC
203	NC
204	NC

7. SSD1870T1R1 TAB PIN ASSIGNMENT

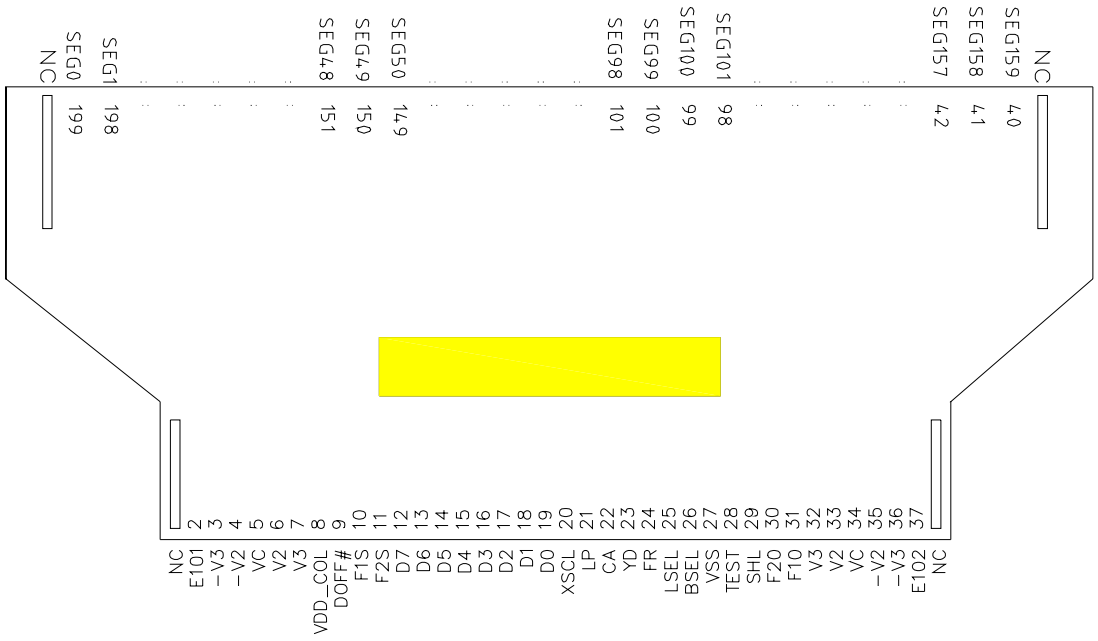
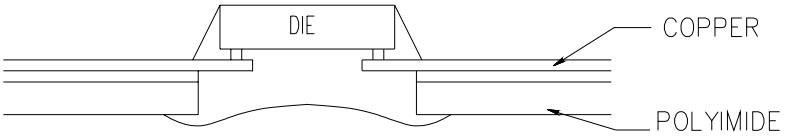


Figure 4 – SSD1870T1R1 TAB Pin Assignment (Copper View, Mirror TAB Design)



MIRROR DESIGN

Table 4 - SSD1870T1R1 Pin Assignment

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	NC	61	SEG138	121	SEG78	181	SEG18
2	EIO1	62	SEG137	122	SEG77	182	SEG17
3	-V3	63	SEG136	123	SEG76	183	SEG16
4	-V2	64	SEG135	124	SEG75	184	SEG15
5	VC	65	SEG134	125	SEG74	185	SEG14
6	V2	66	SEG133	126	SEG73	186	SEG13
7	V3	67	SEG132	127	SEG72	187	SEG12
8	VDD_COL	68	SEG131	128	SEG71	188	SEG11
9	DOFF#	69	SEG130	129	SEG70	189	SEG10
10	F1S	70	SEG129	130	SEG69	190	SEG9
11	F2S	71	SEG128	131	SEG68	191	SEG8
12	D7	72	SEG127	132	SEG67	192	SEG7
13	D6	73	SEG126	133	SEG66	193	SEG6
14	D5	74	SEG125	134	SEG65	194	SEG5
15	D4	75	SEG124	135	SEG64	195	SEG4
16	D3	76	SEG123	136	SEG63	196	SEG3
17	D2	77	SEG122	137	SEG62	197	SEG2
18	D1	78	SEG121	138	SEG61	198	SEG1
19	D0	79	SEG120	139	SEG60	199	SEG0
20	XSCL	80	SEG119	140	SEG59	200	NC
21	LP	81	SEG118	141	SEG58		
22	CA	82	SEG117	142	SEG57		
23	YD	83	SEG116	143	SEG56		
24	FR	84	SEG115	144	SEG55		
25	LSEL	85	SEG114	145	SEG54		
26	BSEL	86	SEG113	146	SEG53		
27	VSS	87	SEG112	147	SEG52		
28	TEST	88	SEG111	148	SEG51		
29	SHL	89	SEG110	149	SEG50		
30	F20	90	SEG109	150	SEG49		
31	F10	91	SEG108	151	SEG48		
32	V3	92	SEG107	152	SEG47		
33	V2	93	SEG106	153	SEG46		
34	VC	94	SEG105	154	SEG45		
35	-V2	95	SEG104	155	SEG44		
36	-V3	96	SEG103	156	SEG43		
37	EIO2	97	SEG102	157	SEG42		
38	NC	98	SEG101	158	SEG41		
39	NC	99	SEG100	159	SEG40		
40	SEG159	100	SEG99	160	SEG39		
41	SEG158	101	SEG98	161	SEG38		
42	SEG157	102	SEG97	162	SEG37		
43	SEG156	103	SEG96	163	SEG36		
44	SEG155	104	SEG95	164	SEG35		
45	SEG154	105	SEG94	165	SEG34		
46	SEG153	106	SEG93	166	SEG33		
47	SEG152	107	SEG92	167	SEG32		
48	SEG151	108	SEG91	168	SEG31		
49	SEG150	109	SEG90	169	SEG30		
50	SEG149	110	SEG89	170	SEG29		
51	SEG148	111	SEG88	171	SEG28		
52	SEG147	112	SEG87	172	SEG27		
53	SEG146	113	SEG86	173	SEG26		
54	SEG145	114	SEG85	174	SEG25		
55	SEG144	115	SEG84	175	SEG24		
56	SEG143	116	SEG83	176	SEG23		
57	SEG142	117	SEG82	177	SEG22		
58	SEG141	118	SEG81	178	SEG21		
59	SEG140	119	SEG80	179	SEG20		
60	SEG139	120	SEG79	180	SEG19		

8. SSD1870T2R TAB PIN ASSIGNMENT

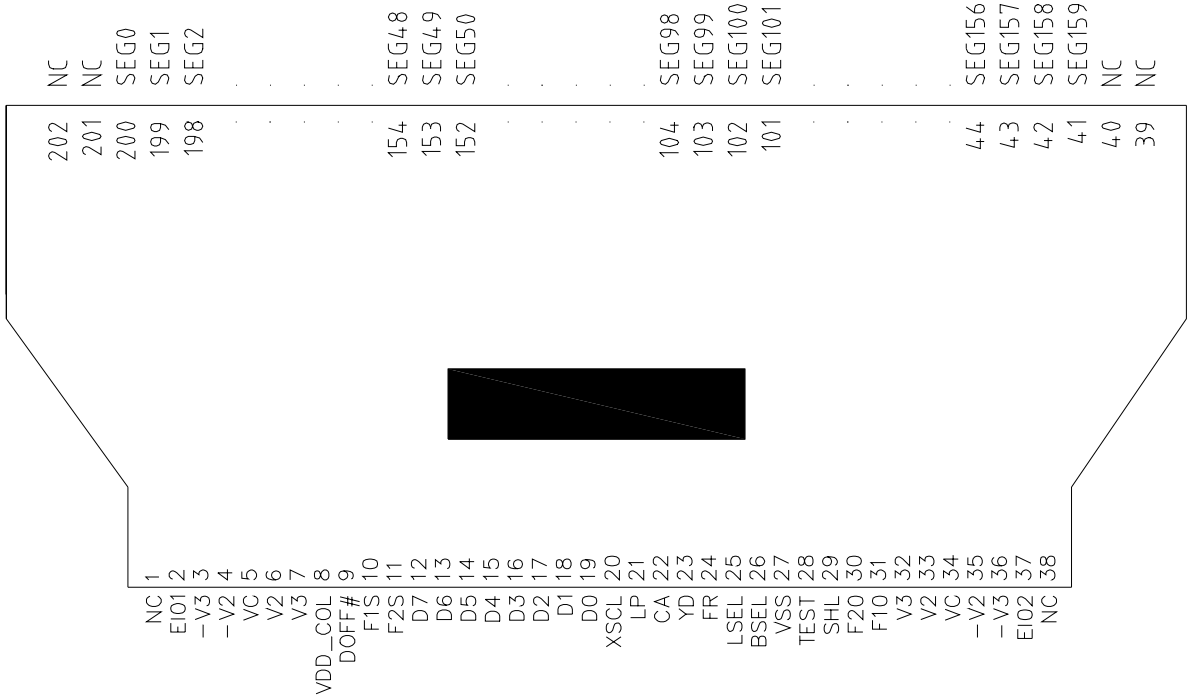
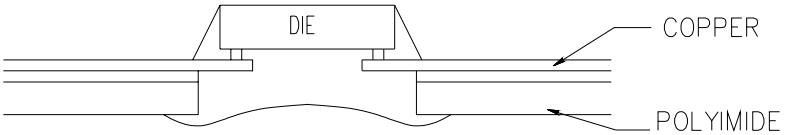


Figure 5 – SSD1870T2R TAB Pin Assignment (Copper View, Mirror TAB Design)



MIRROR DESIGN

Table 5 - SSD1870T2R Pin Assignment

Pin no.	Pin name
1	NC
2	EIO1
3	-V3
4	-V2
5	VC
6	V2
7	V3
8	VDD_COL
9	DOFF#
10	F1S
11	F2S
12	D7
13	D6
14	D5
15	D4
16	D3
17	D2
18	D1
19	D0
20	XSCL
21	LP
22	CA
23	YD
24	FR
25	LSEL
26	BSEL
27	VSS
28	TEST
29	SHL
30	F20
31	F10
32	V3
33	V2
34	VC
35	-V2
36	-V3
37	EIO2
38	NC
39	NC
40	NC
41	SEG159
42	SEG158
43	SEG157
44	SEG156
45	SEG155
46	SEG154
47	SEG153
48	SEG152
49	SEG151
50	SEG150
51	SEG149
52	SEG148
53	SEG147
54	SEG146
55	SEG145
56	SEG144
57	SEG143
58	SEG142
59	SEG141
60	SEG140

Pin no.	Pin name
61	SEG139
62	SEG138
63	SEG137
64	SEG136
65	SEG135
66	SEG134
67	SEG133
68	SEG132
69	SEG131
70	SEG130
71	SEG129
72	SEG128
73	SEG127
74	SEG126
75	SEG125
76	SEG124
77	SEG123
78	SEG122
79	SEG121
80	SEG120
81	SEG119
82	SEG118
83	SEG117
84	SEG116
85	SEG115
86	SEG114
87	SEG113
88	SEG112
89	SEG111
90	SEG110
91	SEG109
92	SEG108
93	SEG107
94	SEG106
95	SEG105
96	SEG104
97	SEG103
98	SEG102
99	SEG101
100	SEG100
101	SEG99
102	SEG98
103	SEG97
104	SEG96
105	SEG95
106	SEG94
107	SEG93
108	SEG92
109	SEG91
110	SEG90
111	SEG89
112	SEG88
113	SEG87
114	SEG86
115	SEG85
116	SEG84
117	SEG83
118	SEG82
119	SEG81
120	SEG80

Pin no.	Pin name
121	SEG79
122	SEG78
123	SEG77
124	SEG76
125	SEG75
126	SEG74
127	SEG73
128	SEG72
129	SEG71
130	SEG70
131	SEG69
132	SEG68
133	SEG67
134	SEG66
135	SEG65
136	SEG64
137	SEG63
138	SEG62
139	SEG61
140	SEG60
141	SEG59
142	SEG58
143	SEG57
144	SEG56
145	SEG55
146	SEG54
147	SEG53
148	SEG52
149	SEG51
150	SEG50
151	SEG49
152	SEG48
153	SEG47
154	SEG46
155	SEG45
156	SEG44
157	SEG43
158	SEG42
159	SEG41
160	SEG40
161	SEG39
162	SEG38
163	SEG37
164	SEG36
165	SEG35
166	SEG34
167	SEG33
168	SEG32
169	SEG31
170	SEG30
171	SEG29
172	SEG28
173	SEG27
174	SEG26
175	SEG25
176	SEG24
177	SEG23
178	SEG22
179	SEG21
180	SEG20

Pin no.	Pin name
181	SEG19
182	SEG18
183	SEG17
184	SEG16
185	SEG15
186	SEG14
187	SEG13
188	SEG12
189	SEG11
190	SEG10
191	SEG9
192	SEG8
193	SEG7
194	SEG6
195	SEG5
196	SEG4
197	SEG3
198	SEG2
199	SEG1
200	SEG0
201	NC
202	NC

9. PIN DESCRIPTIONS

VDD_COL, VSS

These are power supply pins to the logic system, VDD_COL is power supply pin and VSS is ground pin.

V3, V2, VC, -V2, -V3

These are power supply pins to the LCD driving system, V3>V2>VC>-V2>-V3.

YD

This is an input pin and the YD pulse signal is used to reset the column address for writing. The number of lines for writing are determined by the number of LP pulses in a single YD cycle.

LP

This is an input pin for displaying data latch clock. The display data is latched at the falling edge of LP from the data registers to the RAM.
When 1/2P operation is selected, the frequency of LP is twice as that in 1P normal operation.

CA

This is an input pin and the signal is generated by the row driver, eg, SSD1881. This signal inputs to the column driver at the start of each new field.

XSCL

This is an input pin for display data shift clock. Data (D0-D7) is read sequentially into the data register at the falling edge of XSCL.

FR

This is an input pin and is used to change the LCD driving waveform polarity.

F1S, F2S

These are input pins and are used to determine the changeover interval. There are 4 changeover intervals which can be selected by F1S and F2S.

F1S	F2S	Changeover Interval
1	1	4-line interval
0	1	2-line interval
1	0	8-line interval
0	0	Field

Table 6 - Relationship between changeover interval and F1S & F2S

DOFF#

This is an input pin to turn the display on/off. When it is set at “L” level, all segment outputs is forced to VC and the display RAM data is maintained. In normal display operation, it is set to “H” level.

EIO1, EIO2

These are I/O pins which can be configured as input or output depending on signal of SHL. When SHL is set to “L” level, EIO1 is output and EIO2 is input. When SHL is set to “H” level, EIO1 is input and EIO2 is output.

When only one segment driver is used, the EIO input must be tied to “L” level and the EIO output must be disconnected.

When multiple segment drivers are used, the EIO input of the leading driver is tied at “L” level and its EIO output is connected to the EIO input of the next segment driver, that means, the EIO of the other drivers are cascade connected. Once a pulse LP is sensed, all EIO outputs are reset to “H” level. Then, the enable control circuit automatically senses when 160 bits worth of data have been received and automatically sends the enable signal.

BSEL

This is an input pin to choose 4-bit or 8-bit data inputs. When this pin is set at “L” level, 4-bit input is chosen. When this pin is set at “H” level, 8-bit input is chosen.

LSEL

This is an input pin to select “1P operation” or “1/2P operation”. When it is set to “L” level, normal operation is selected. When it is set at “H” level, 1/2P operation is selected.

SHL

This is an input pin to determine the shift direction of the display data. The relationship between the display data and the segment output is shown in Table 7.

TEST

This is a reserved input pin and it must set to “L” level in the normal display operation.

D0-D7

This is data-bus for data transferring. D0-D7 are used when 8-bit input is selected. When 4-bit input is selected, only D0-D3 are used and D4-D7 must be tied to VSS or VDD_COL.

F10, F20

These are output pins to the field signal of row driver.

SEG0-SEG159

These are output pins and provide segment driving signals to the LCD panel. Output transition occurs at the falling edge of LP.

10. FUNCTIONAL BLOCK DESCRIPTIONS

Timing Control Circuit

This circuit is used to determine the self refresh rate which enables the shift register to write the display data to the RAM and output the column address and perform field control on the MLA decoder. When only one segment driver is used, the EIO is set to a disable state ("H" level). At this disable state, the internal clock signal and the data bus are fixed at "L" level and the chip is in power save mode. However, when multiple segment drivers are used, the EIO of the first driver is connect to "VSS" and the EIO of the other drivers are cascade connected. Then, the enable control circuit automatically senses when 160 bits data have been received and automatically sends the enable signal.

Data Control Circuit

This receives the display data input and sends them to the shift register. In addition, this circuit controls the number of input data interface selected by BSEL. When this pin is set at "L" level, 4-bit input is chosen. When this pin is set at "H" level, 8-bit input is chosen.

Shift Register

This is a 160-bit register with four lines. It controls the writing of the display RAM and the order of display data which is determined by the SHL input. At each falling edge of the LP signal, it receives display data from one line and writes to the RAM after it has stored 4 lines of data. The shift direction of the display data is determined by SHL pin, Table 7 shows the relationship between the display data and the segment for both 4-bit input data and 8-bit input data.

For example, when BSEL is set to "L", ie, 4-bit (D0-D3) data input is selected and the order of the display data input to (D3, D2, D1, D0) is (a, b, c, d) (e, f, g, h) ... (s, t, u, v) (w, x, y, z). Similarly, when BSEL is set to "H", ie, 8-bit (D0-D7) input data is selected and the order of the display data input to (D7, D6, D5, D4, D3, D2, D1, D0) is (a, b, c, d, e, f, g, h) ... (s, t, u, v, w, x, y, z). Then the display data will be shifted to the segment output according to the setting of SHL and EIO.

SHL	SEGMENT OUTPUT																	EIO	
	159	158	157	156	155	154	153	152	.....	7	6	5	4	3	2	1	0	1	2
L	a	b	c	d	e	f	g	h	.....	s	t	u	v	w	x	y	z	Output	Input
H	z	y	x	w	v	u	t	s	.....	h	g	f	e	d	c	b	a	Input	Output

Table 7 - Relationship between the display data and the segment outputs

RAM

This consists of 160 x 240 bits static RAM for storing LC display data.

MLA Decoder

The decoder outputs a signal to select five voltage levels among V3, V2, VC, -V2 & -V3. The signal is controlled by the display data, FR, F10, F20 and DOFF#.

Segment Cell Level Shifter

This is a level interface circuit which is used to translate the low voltage output signal to the high signal voltage.

11. HALT WRITE FUNCTION

This function is used to put the segment driver in the “Halt Write Mode”. Halt Write Mode defines a situation where the transmission of display data from the display controller to the SSD1870 is suspended when the content of the display does not change. At the same time, the SSD1870 automatically senses this status and enters a power down display mode.
In order to put the SSD1870 in the Halt Write Mode, the XSCL clock is stopped during four horizontal display periods after the completion of the input of the display data of an r+3 line. When the XSCL clock is suspended, the power is reduced and the latching of data D0-D7 are suspended. However, the display controller must send LP, YD and FR signals to the SSD1870 periodically so that the SSD1870 can read display data from the internal RAM and refreshes the display
In order to get out of the “Halt Write Mode”, the display controller inputs the XSCL clock to the SSD1870 for four or more horizontal display periods with the timing of the data transmission from the falling edge of the LP signal at the time of an r+3 line. After the fourth horizontal period after getting out of the “Halt Write Mode”, the display data transmitted during the four horizontal display intervals is written to frame memory at the falling edge of the LP signal.

12. RELATIONSHIP BETWEEN OUTPUT VOLTAGE & DISPLAY DATA

In order to drive an MLA module, for example, a 160 Mux LCD module system formed by a row (common) driver such as SSD1881 & a column (segment) driver such as SSD1870, there is a relationship between the common/segment output voltages, the input pin settings and the display data to drive the module. If it is a 160 Mux MLA module, the relationship between line# and Common shows in Table 8.

Line#	Formula	Common
r	Multiples of 4	0, 4, 8, 12, ... , 148, 152, 156
r + 1	1 + multiples of 4	1, 5, 9, 13, ... , 149, 153, 157
r + 2	2 + multiples of 4	2, 6, 10, 14, ... ,150, 154, 158
r + 3	3 + multiples of 4	3, 7, 11, 15, ... , 151, 155, 159

Table 8 - Relationship between line# and Common

Common Output Voltage

The following two tables show the relationships between the common voltage and F10 & F20. The common voltage relation is +V1>VC>-V1 and VC is the mid-level voltage. Table 9 shows their relationship when FR is set to “L” level and Table 10 shows their relationship when FR is set to “H” level.

When FR = L

F10 F20	1 1	0 1	1 0	0 0
line r	V1	V1	-V1	V1
Line (r + 1)	-V1	V1	V1	V1
Line (r + 2)	V1	-V1	V1	V1
Line (r + 3)	V1	V1	V1	-V1

Table 9 - Relationship between common voltage and F10 & F20 when FR = L

When FR = H

F10 F20	1 1	0 1	1 0	0 0
line r	-V1	-V1	V1	-V1
Line (r + 1)	V1	-V1	-V1	-V1
Line (r + 2)	-V1	V1	-V1	-V1
Line (r + 3)	-V1	-V1	-V1	V1

Table 10 - Relationship between common voltage and F10 & F20 when FR = H

In each field, the order of F10 & F20 is shown in Table 11. In Table 11, the first place in the bracket represents F10 and the second place in the bracket represents F20, i.e., (F10, F20). The changeover interval for each field is determined by the setting of F1S & F2S and Table 6 in the pin descriptions section.

Field# 1	(1,1) → (0,1) → (1,0) → (0,0) → (1,1) → (0,1) → (1,0) → (0,0)
Field# 2	(0,1) → (1,0) → (0,0) → (1,1) → (0,1) → (1,0) → (0,0) → (1,1)
Field# 3	(1,0) → (0,0) → (1,1) → (0,1) → (1,0) → (0,0) → (1,1) → (0,1)
Field# 4	(0,0) → (1,1) → (0,1) → (1,0) → (0,0) → (1,1) → (0,1) → (1,0)

Table 11 - The order of F10 & F20 in each field in 1P operation mode.

Segment Output Voltage

The following two tables show the relationships between the segment output voltages, the setting of FR, F10 & F20 and the display data when DOFF# is set at "H" level. All segment voltages are tied to the VC level when DOFF# is set at "L" level.

In these two tables, "0" in display line represents "not lit" while "1" in display line represents "lit". Table 7 shows their relationship when FR is set at "L" level and Table 8 shows that when FR is set at "H" level.

When FR = L

Line#		Display Data (0 = not lit; 1 = lit)															
R		1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
r + 1		1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
r + 2		1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
r + 3		1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
F10	F20	Segment Voltage Level															
1	1	-V2	V_C	V_C	V2	-V3	-V2	-V2	V_C	V_C	V2	V2	V3	-V2	V_C	V_C	V2
0	1	-V2	V_C	-V3	-V2	V_C	V2	-V2	V_C	V_C	V2	-V2	V_C	V2	V3	V_C	V2
1	0	-V2	V_C	V_C	V2	V_C	V2	V2	V3	-V3	-V2	-V2	V_C	-V2	V_C	V_C	V2
0	0	-V2	-V3	V_C	-V2	V_C	-V2	V2	V_C	V_C	-V2	V2	V_C	V2	V_C	V3	V2

Table 12 - Relationship between the segment voltages and the display data when FR = L

When FR = H

Line#		Display Data (0 = not lit; 1 = lit)															
R		1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
r + 1		1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
r + 2		1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
r + 3		1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
F10	F20	Segment Voltage Level															
1	1	V2	V_C	V_C	-V2	V3	V2	V2	V_C	V_C	-V2	-V2	-V3	V2	V_C	V_C	-V2
0	1	V2	V_C	V3	V2	V_C	-V2	V2	V_C	V_C	-V2	V2	V_C	-V2	-V3	V_C	-V2
1	0	V2	V_C	V_C	-V2	V_C	-V2	-V2	-V3	V3	V2	V2	V_C	V2	V_C	V_C	-V2
0	0	V2	V3	V_C	V2	V_C	V2	-V2	V_C	V_C	V2	-V2	V_C	-V2	V_C	-V3	-V2

Table 13 - Relationship between the segment voltages and the display data when FR = H

1P Operation Mode and 1/2P Operation Mode

In SSD1870, there are two operation modes:

1) 1P Operation Mode and
2) 1/2P Operation Mode.

These operation modes are determined by the setting of LSEL. When LSEL is set to "L", 1P operation mode is selected. However, when LSEL is set to "H", 1/2P operation mode is selected. In 1/2P operation mode, the LP frequency is twice of that in 1P operation. The field data changes in each LP, thus the output changes at the center point of the 1P interval. However, writing display data to the RAM and reading the display data from the RAM are the same as in the 1P operation. The row driver output changes according to the field data output by the column driver with each LP pulse, causing a transition at the center point of the 1P interval; however, the transition of the driving line occurs at each 1P, just as in the 1P operation.

In addition, during 1/2P operation, the changes of the F10 and F20 in each field are as shown in Table 14. In Table 14, the first place in the bracket represents F10 and the second place in the bracket represents F20, i.e., (F10, F20). Besides, explanation of the first half cycle and the second half cycle is shown in Figure 6.

	1st half cycle	2nd half cycle	1st half cycle	2ndhalf cycle	1st half cycle	2nd half cycle	1st half cycle	2nd half cycle
Field# 1	(0,0) →	(1,1) →	(1,1) →	(0,0) →	(0,0) →	(1,1) →	(1,1) →	(0,0)
Field# 2	(1,1) →	(0,0) →	(0,0) →	(1,1) →	(1,1) →	(0,0) →	(0,0) →	(1,1)
Field# 3	(1,0) →	(0,1) →	(0,1) →	(1,0) →	(1,0) →	(0,1) →	(0,1) →	(1,0)
Field# 4	(0,1) →	(1,0) →	(1,0) →	(0,1) →	(0,1) →	(1,0) →	(1,0) →	(0,1)

Table 14- The order of F10 & F20 in each field in the 1/2 P operation mode

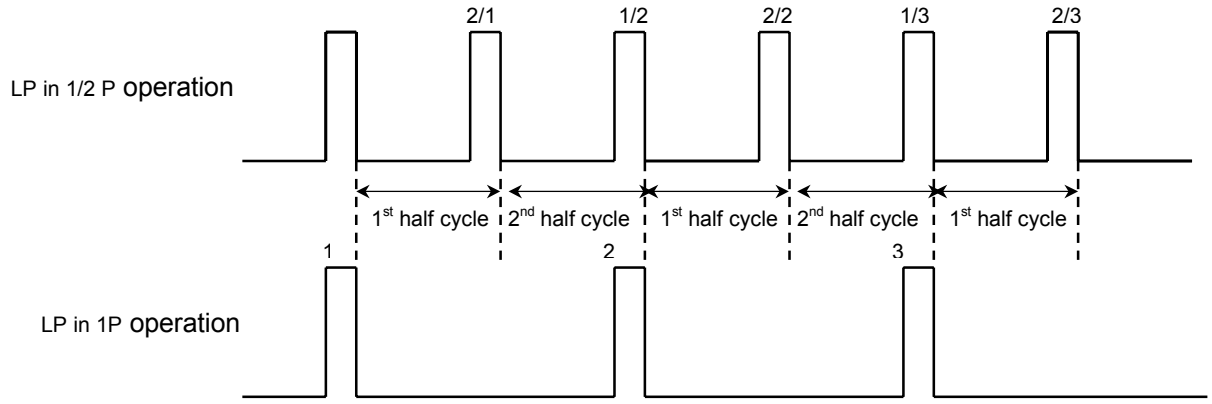
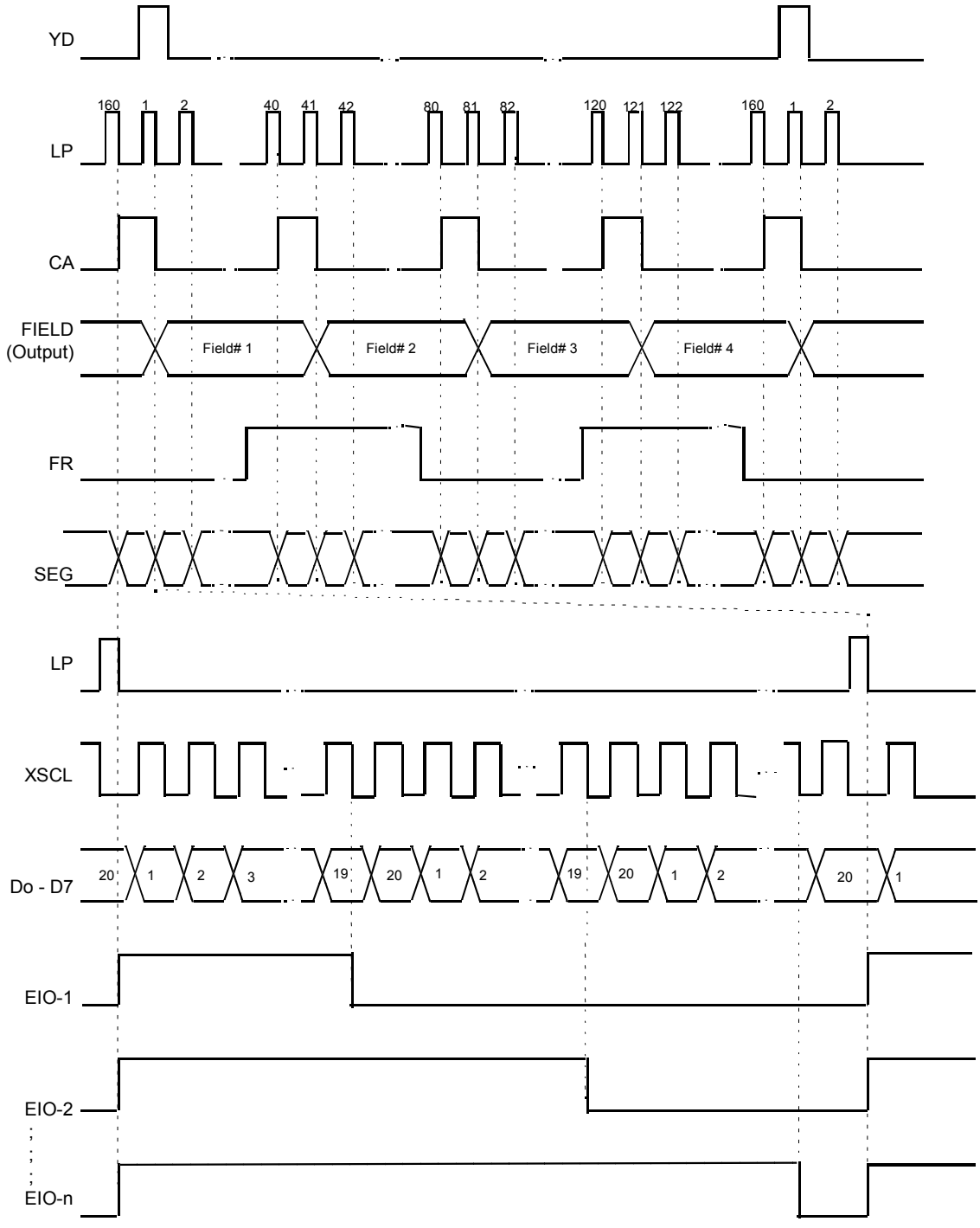


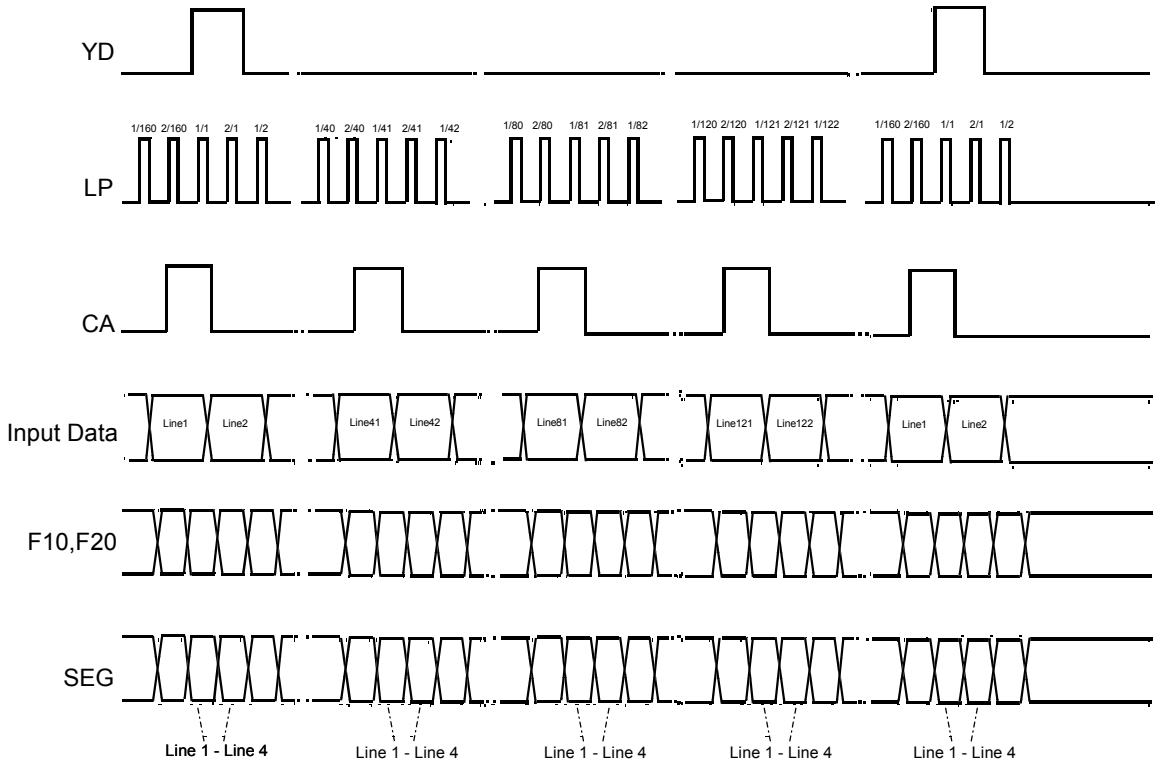
Figure 6 - LP in 1/2P operation mode and 1P operation mode

In 1/2P operation mode, the inputs of F1S and F2S are ignored and, for the segment output voltages, there is no difference between these two modes.

Timing Diagram For 1/160 duty and 1P operation



Timing Diagram For 1/160 duty and 1/2P operation



13. MAXIMUM RATINGS

Table 15 - Maximum Ratings

Symbol	Parameter	Value	Unit
VDD_COL	Power Voltage	4.0	V
-V3		-4.0	V
V_{IN}	Input Voltage	VSS -0.3 to VDD_COL+0.3	V
V_0	Output Voltage	VSS -0.3 to VDD_COL+0.3	V
I	Output current at EIO	20	mA
T_A	Operating temperature	-30 to +85	°C
T_{stg}	Storage temperature	-65 to +150	°C

Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits shown in the DC characteristics section.

This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. All dummy and NC pins must be left open & unconnected. Don't group the NC pins together. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

14. DC CHARACTERISTICS

VSS = 0.0V, T_A = 25°C

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDD_COL	Power supply voltage		2.4	3.3	3.6	V
V3	Power supply voltage	VDD_COL = 2.4V to 3.6V	-	VDD_COL	-	V
V2			-	0.5xV3	-	V
VC			-	VSS	-	V
-V2			-	-0.5xV3	-	V
-V3			-	-V3	-	
I_{T1}	Current drain from Pin VDD_COL in the data transfer mode	VSS=0.0V, V3=VDD_COL=3.3V, V2=1.65V, VC=0.0V, -V2=-1.65V, -V3=-3.3V, V_{IN}=VDD_COL or V_{SS}, f_{XSCL}=480kHz, f_{LP}=12kHz, f_{FR}=30Hz, Input data (Checkboard pattern), 8-bit input, 160 x 160, no loading	-	80	100	uA
I_{T2}	Current drain from Pin -V3 in the data transfer mode		-	10	20	uA
I_R	Current drain from Pin VDD_COL in the write halt mode	VSS=0.0V, V3=VDD_COL=3.3V, V2=1.65V, VC=0.0V, -V2=-1.65V, -V3=-3.3V, V_{IN}=VDD_COL or V_{SS}, f_{LP}=12kHz, f_{FR}=30Hz, Input data (Checkboard pattern), 8-bit input, 160 x 160, no loading, XSCL tie to VC	-	30	70	uA
I_{S1}	Static current drain from Pin VDD_COL	V_{IN} = VDD_COL or VSS	-	-	10.0	uA
I_{S2}	Static current drain from Pin -V3	VSS=0.0V, V3=VDD_COL=3.3V, V2=1.65V, VC=0.0V, -V2=-1.65V, -V3=-3.3V, V_{IN}=VDD_COL or V_{SS}	-	-	5.0	uA
V_{IH}	Input High voltage at pins: EIO1, EIO2, SHL, BSEL, LSEL, FR, YD, CA, LP, XSCL, D0-D7, F1S, F2S & DOFF#	VDD_COL = 2.4V to 3.6V	0.8*VDD_COL	-	VDD_COL	V
V_{IL}	Input Low voltage at pins: EIO1, EIO2, SHL, BSEL, LSEL, FR, YD, CA, LP, XSCL, D0-D7, F1S, F2S & DOFF#		-	-	0.2*VDD_COL	V
V_{OH}	Output High voltage at pins: EIO1, EIO2, F10 & F20	VDD_COL = 2.4V to 3.6V, I_{Out} = -0.6mA	0.9*VDD_COL	-	VDD_COL	V

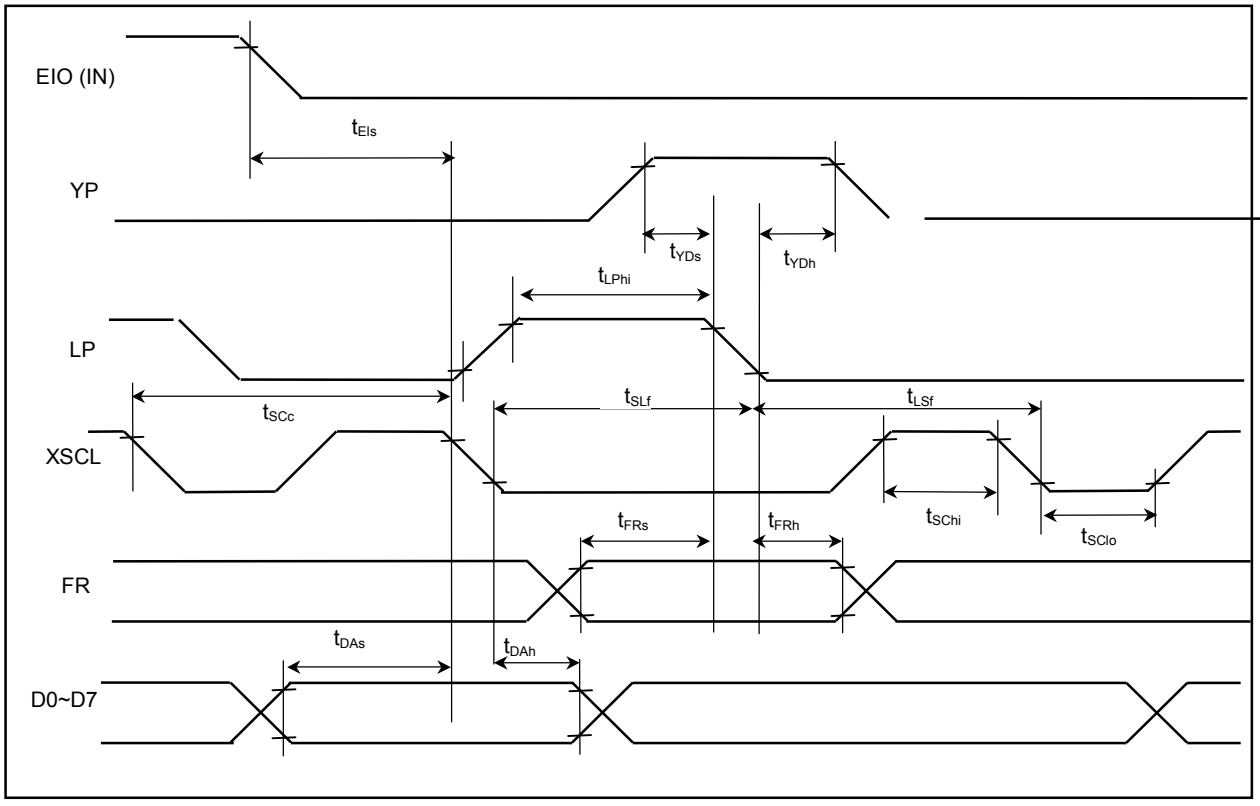
V_{OL}	Output Low voltage at pins: EIO1, EIO2, F10 & F20		-	-	0.1*VDD_COL	V
I_{L1}	Input leakage current at pins: SHL, BSEL, LSEL, FR, YD, CA, LP, XSCL, D0-D7, F1S, F2S & DOFF#		-	-	5.0	uA
I_{L2}	I/O leakage current at pins: EIO1 & EIO2		-	-	5.0	uA
R_{Out}	Output resistance of pins: SEG0 - SEG159	VSS=0.0V, V3=VDD_COL=3.3V, V2=1.65V, VC=0.0V, -V2=-1.65V and -V3=-3.3V	-	0.8	1.5	kΩ

15. AC CHARACTERISTICS

Input Timing Characteristics

VSS = VC = 0.0V, V3 = VDD_COL = 3.3V, V2 = 1.65V, -V2 = -1.65V and -V3 = -3.3V, $T_A = 25^oC$

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCc}	XSCL period	150	-	-	ns
t_{SChi}	XSCL pulse width (High level)	20	-	-	ns
t_{SClo}	XSCL pulse width (Low level)	20	-	-	ns
t_{LPhi}	LP pulse width (High level)	100	-	-	ns
t_{YDs}	YD setup time	50	-	-	ns
t_{YDh}	YD hold time	50	-	-	ns
t_{FRs}	FR setup time	25	-	-	ns
t_{FRh}	FR hold time	10	-	-	ns
t_{EIs}	EIO setup time	30	-	-	ns
t_{SLf}	Fall time between XSCL & LP	10	-	-	ns
t_{LSf}	Fall time between LP & XSCL	150	-	-	ns
t_{DAs}	Data setup time	10	-	-	ns
t_{DAh}	Data hold time	10	-	-	ns



(VSS = VC = 0.0V, V3 = VDD_COL = 3.3V, V2 = 1.65V, -V2 = -1.65V and -V3 = -3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{EIre}	EIO reset time	-	-	80	ns
t_{EId}	EIO output delay time	-	-	90	ns
t_{SGd}	Segment output delay time	-	-	400	ns
t_{Fd}	F10 & F20 output delay time	-	-	3000	ns

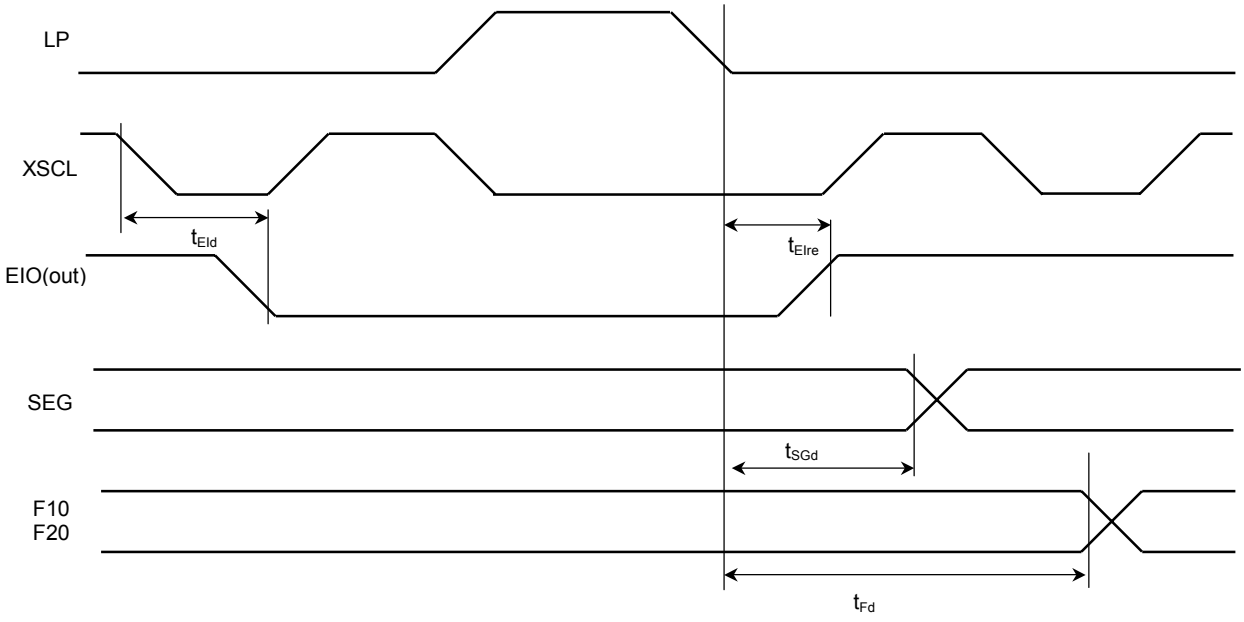
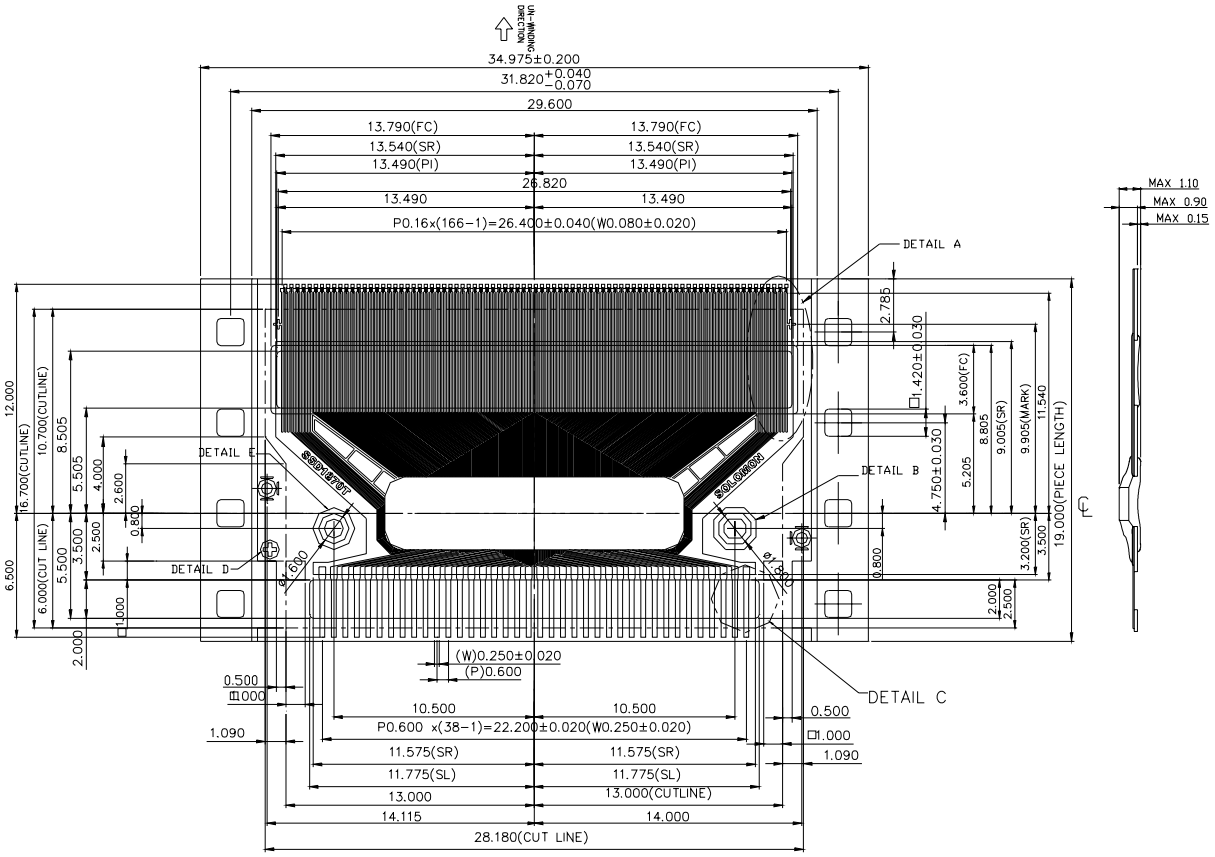
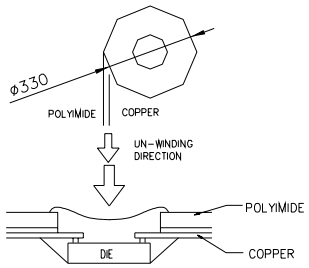


Figure 8 - Output Timing Characteristics

17. PACKAGE DIMENSION

SSD1870TR TAB Package Dimension – 1

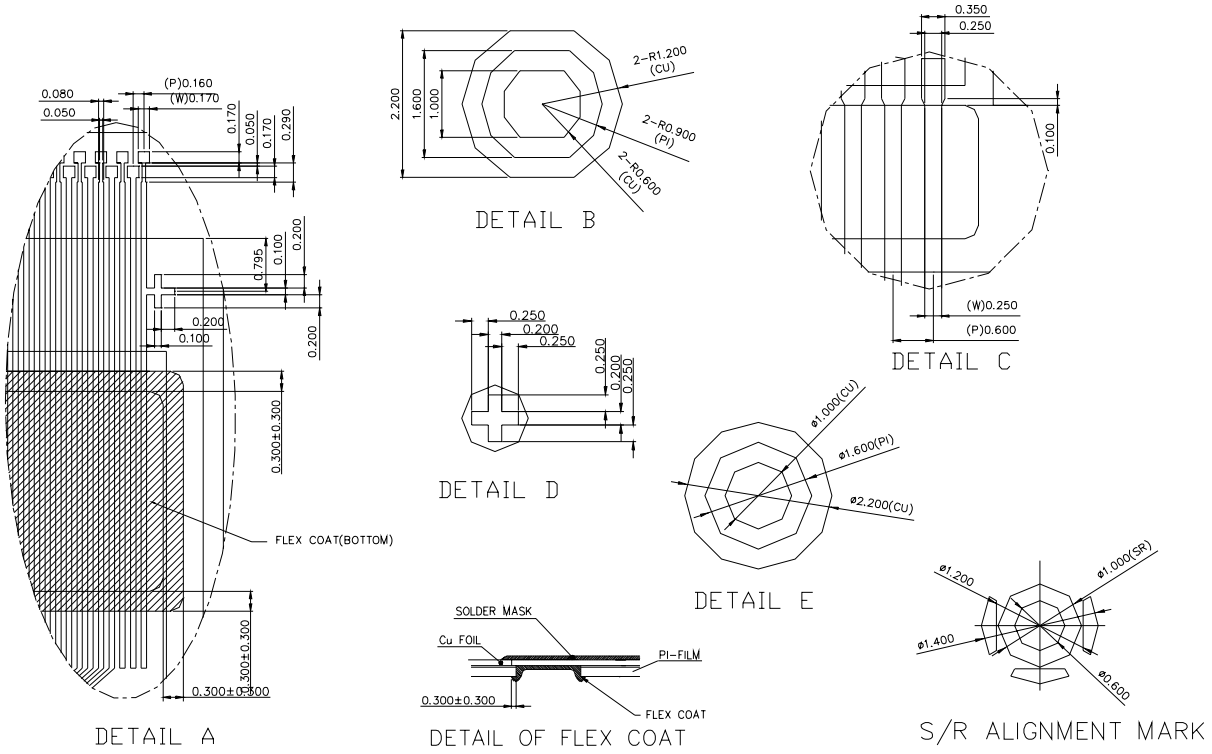




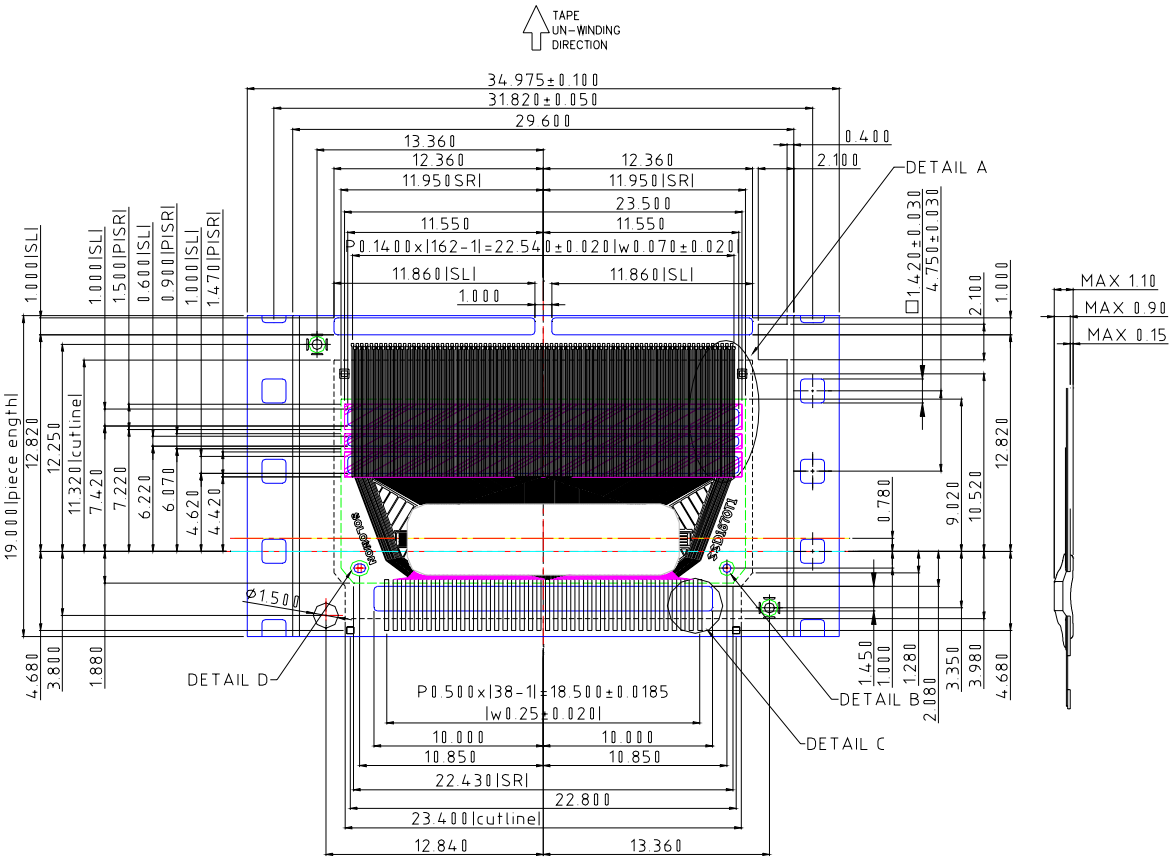
DIE SIZE: 13.660 X 1.8133 mm
4 SPROCKET HOLES (19.00mm) FOR 1 TAPE

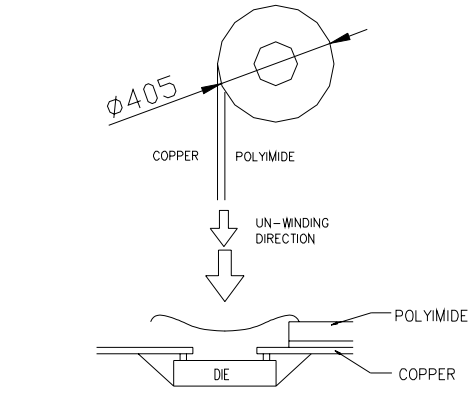
1. GENERAL TOLERANCE:±0.050MM
2. ALL CHAMFER IS R0.20
3. MATERIAL
   POLYIMIDE:UPILEX-S 75um±6 THICKNESS
   ADHESIVE :TORAY #7100 12um±2 THICKNESS
   CU : ED-SLP 35um
   FLEX COATING : FS-100 L22 MAX .0.700
   SOLDER RESIST : AE-70-M11 26±14um
   SOLDER RESIST GENERAL TOLERANCE ±0.300mm
4. PLATING OTHER TOLERANCE±0.300
   PLATING SN: 0.35±0.05um
   ALL CHAMFER IS R0.200mm
   GENERAL TOLERANCE ±0.050mm

SSD1870TR TAB Package Dimension – 2



SSD1870T1R1 TAB Package Dimension – 1

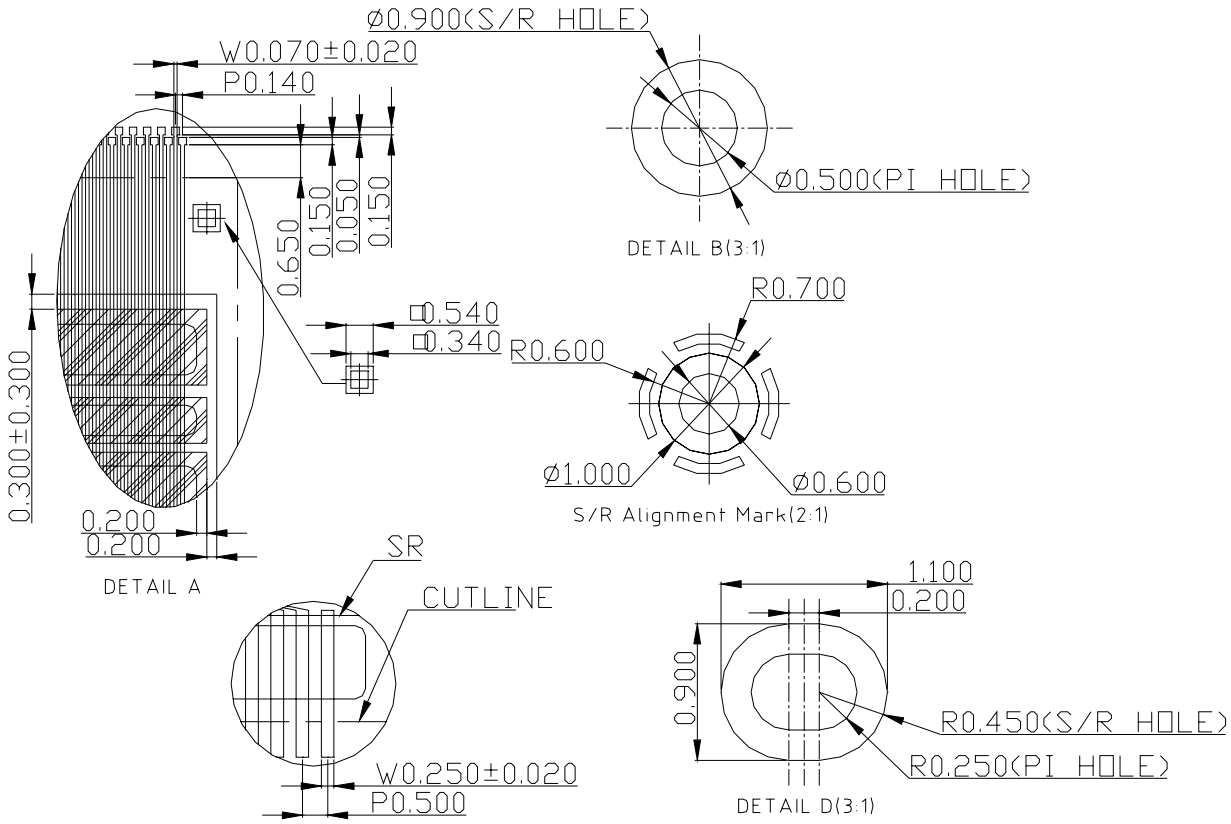




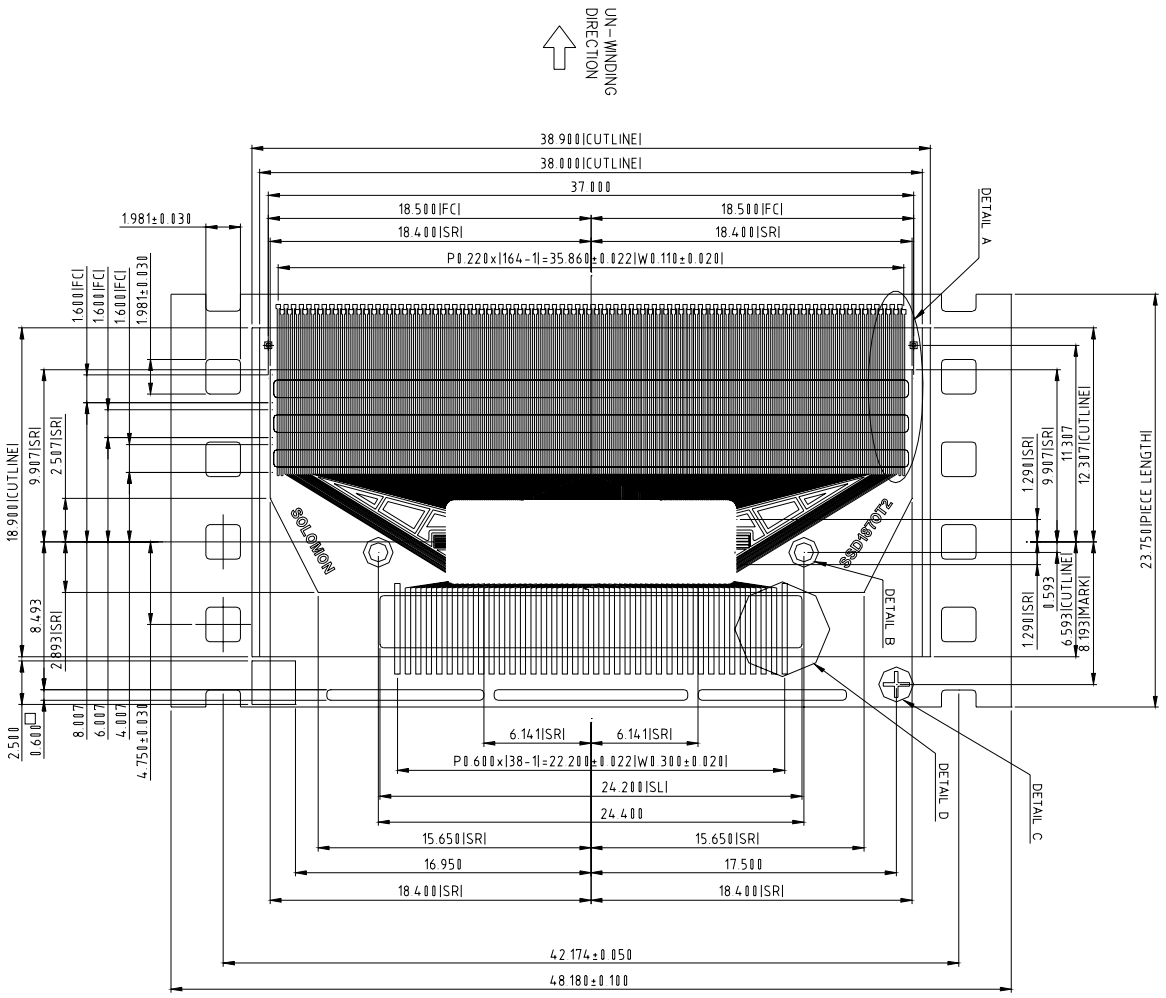
4 SPROCKET HOLES (19.00mm) FOR 1 TAPE

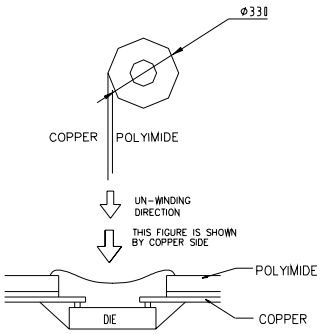
NOTE:
1. GENERAL TOLERANCE: ±0.050mm
2. MATERIALS
   PI: 75UM±6 THICKNESS
   ADHESIVE: UPILEX-S
   CU: SLP 25um
   FLEX COATING: FS-100L
   SOLDER RESIST: AE-70-M11
   OTHER TOLERANCE±0.200mm
3. PLATING SN: 0.35±0.05um
4. TAPSITE:4 SPROCKET HOLES,19.00mm
5. ALL CHAMFER IS R0.200mm

SSD1870T1R1 TAB Package Dimension – 2



SSD1870T2R TAB Package Dimension – 1





NOTE:

1. GENERAL TOLERANCE: ±0.050mm
2. MATERIALS
   PI: 75UM±6 THICKNESS
   ADHESIVE: TORAY#7100 12um±2 THICKNESS
   CU: FQ-VLP 18UM
   FLEX COATING: FS-100L
   SOLDER RESIST: AE-70-M11 26±14
   OTHER TOLERANCE ±0.300mm
3. PLATING SN: 0.350±0.050um
4. TAPSITE: 5 SPROCKET HOLES, 23.750mm
5. ALL CHAMFER IS R0.200mm

SSD1870T2R TAB Package Dimension – 2