

RoHS Compliant Product  
A suffix of "-C" specifies halogen free

## DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide Low  $R_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

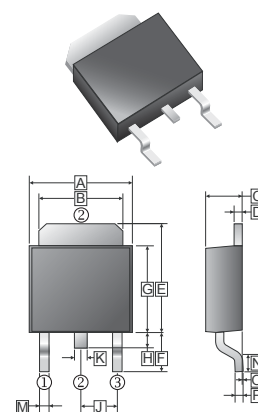
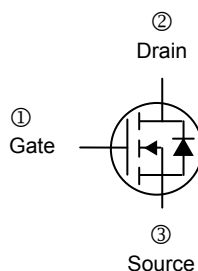
**TO-252(D-Pack)**

## FEATURES

- Low  $R_{DS(on)}$  provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe DPAK saves board space.
- Fast switching speed.
- High performance trench technology.

## PRODUCT SUMMARY

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$V_{DS}(V)$	$R_{DS(on)}$ m( $\Omega$ )	$I_D(A)$
150	255@ $V_{GS}=10V$	12
	290@ $V_{GS}=5.5V$	11



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.4	6.8	J	2.30	REF.
B	5.20	5.50	K	0.70	0.90
C	2.20	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.6
E	6.8	7.3	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.2			
H	0.8	1.20			

## ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	$V_{DS}$	150	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>a</sup>	$I_D @ T_C=25^\circ C$	12	A
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	36	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	30	A
Total Power Dissipation <sup>a</sup>	$P_D @ T_C=25^\circ C$	50	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 ~ 175	$^\circ C$
THERMAL RESISTANCE RATINGS			
Maximum Thermal Resistance Junction-Ambient <sup>a</sup>	$R_{\theta JA}$	50	$^\circ C / W$
Maximum Thermal Resistance Junction-Case	$R_{\theta JC}$	3.0	$^\circ C / W$

Notes :

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature.

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ C$  unless otherwise specified)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
<b>Static</b>						
Gate-Threshold Voltage	$V_{GS(th)}$	1.0	-	-	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
Gate-Body Leakage	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{DS} = 0V, V_{GS} = 20V$
Zero Gate Voltage Drain Current	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS} = 120V, V_{GS} = 0V$
		-	-	25		$V_{DS} = 120V, V_{GS} = 0V, T_J = 55^\circ C$
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	34	-	-	A	$V_{DS} = 5V, V_{GS} = 10V$
Drain-Source On-Resistance <sup>a</sup>	$R_{DS(ON)}$	-	-	255	m $\Omega$	$V_{GS} = 10V, I_D = 9.2 A$
		-	-	290		$V_{GS} = 5.5V, I_D = 6.1 A$
Forward Transconductance <sup>a</sup>	$g_{fs}$	-	4.4	-	S	$V_{DS} = 40V, I_D = 5.5 A$
Diode Forward Voltage	$V_{SD}$	-	1.1	-	V	$I_S = 9 A, V_{GS} = 0 V$
<b>Dynamic <sup>b</sup></b>						
Total Gate Charge	$Q_g$	-	19	-	nC	$V_{DS} = 25 V$ $V_{GS} = 10 V$ $I_D = 9 A$
Gate-Source Charge	$Q_{gs}$	-	3	-		
Gate-Drain Charge	$Q_{gd}$	-	9.5	-		
Turn-on Delay Time	$T_{d(on)}$	-	25	-	nS	$V_{DD} = 100 V$ $I_D = 9 A$ $V_{GEN} = 10 V$ $R_L = 25 \Omega$
Rise Time	$T_r$	-	60	-		
Turn-off Delay Time	$T_{d(off)}$	-	65	-		
Fall Time	$T_f$	-	45	-		

Notes

- a. Pulse test : Pulse width  $\leq 300 \mu s$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.