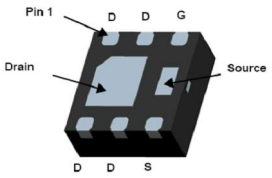
SSF1221J2

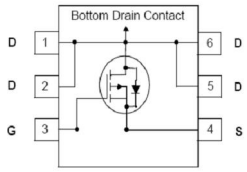
12V P-Channel MOSFET

Main Product Characteristics

V_{DSS}	-12V
R_{DS}(on)	14.4 mΩ(typ.)
I_D	-12A



DFN2x2-6L Pin Assignment



Schematic Diagram

Features and Benefits

- Advanced trench MOSFET process technology
- Special designed for battery charge, load switching in cellular handset and general ultraportable applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150℃ operating temperature
- Lead free product

Description:

It utilizes the latest trench processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in battery charge and load switching in cellular handset and a wide variety of other ultraportable applications.

Absolute Max Rating

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 4.5V①	-12	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 4.5V①	-7.4	
I_{DM}	Pulsed Drain Current②	-28	
P_D @T_C = 25°C	Power Dissipation③	2.4	W
V_{DS}	Drain-Source Voltage	-12	V
V_{GS}	Gate-to-Source Voltage	± 8	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case	6.9	8	℃/W
$R_{\theta JA}$	Junction-to-ambient (t ≤ 10s) ④	52	62.5	℃/W

Electrical Characteristics @T_A=25℃ unless otherwise specified

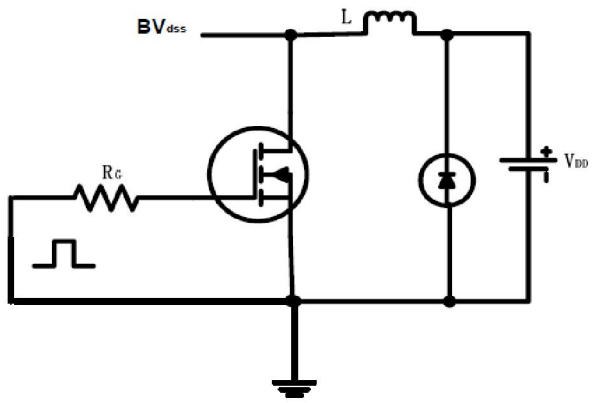
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	-12	—	—	V	V_{GS} = 0V, ID = 250μA
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	14.4	16	mΩ	V_{GS} =-4.5V, I_D =-10A
		—	18.9	21		V_{GS} =-2.5V, I_D =-8.9A
		—	26.4	38		V_{GS} =-1.8V, I_D =-4.5A
$V_{GS(th)}$	Gate threshold voltage	-0.4	—	-1	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source leakage current	—	—	-1	μA	V_{DS} = -12V,V_{GS} = 0V
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	V_{GS} = 8V
		—	—	-100		V_{GS} = -8V
g_{FS}	Forward Transconductance	-3	—	—	S	V_{DS} = -5V, I_D =-10A
Q_g	Total gate charge	—	21	—	nC	I_D = -10A,
Q_{gs}	Gate-to-Source charge	—	2.5	—		V_{DD}=-6V,
Q_{gd}	Gate-to-Drain("Miller") charge	—	6	—		V_{GS} = -4.5V
$t_{d(on)}$	Turn-on delay time	—	30	—	ns	V_{GS}=-4.5V,
t_r	Rise time	—	48	—		V_{DD}=-6V,
$t_{d(off)}$	Turn-Off delay time	—	97	—		I_D = -10A,
t_f	Fall time	—	65	—		R_{GEN}=6Ω
C_{iss}	Input capacitance	—	2138	—	pF	V_{GS} = 0V
C_{oss}	Output capacitance	—	685	—		V_{DS} = -6V
C_{rss}	Reverse transfer capacitance	—	650	—		f = 1MHz

Source-Drain Ratings and Characteristics

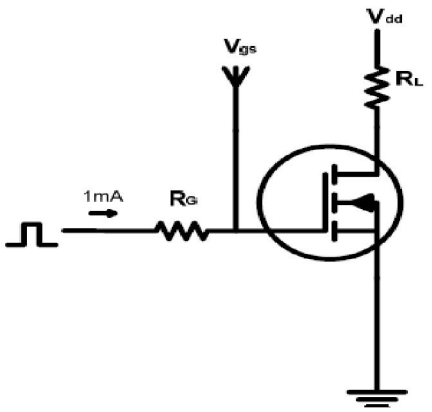
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-12	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)	—	—	-28	A	
V_{sd}	Diode Forward Voltage	—	-0.77	-1.2	V	I_S=-2A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	—	16	—	ns	T_J = 25°C, I_F =-10A, di/dt = 100A/μs
Q_{rr}	Reverse Recovery Charge	—	5.9	—	uC	

Test Circuits and Waveforms

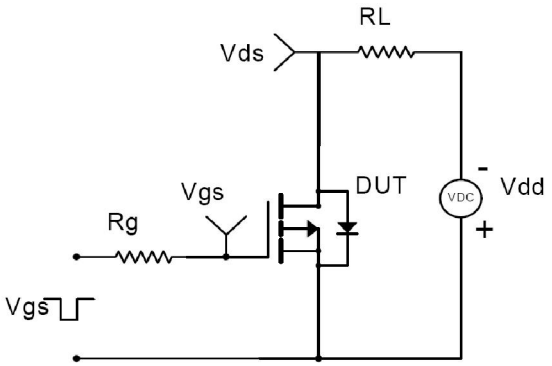
EAS test circuits:



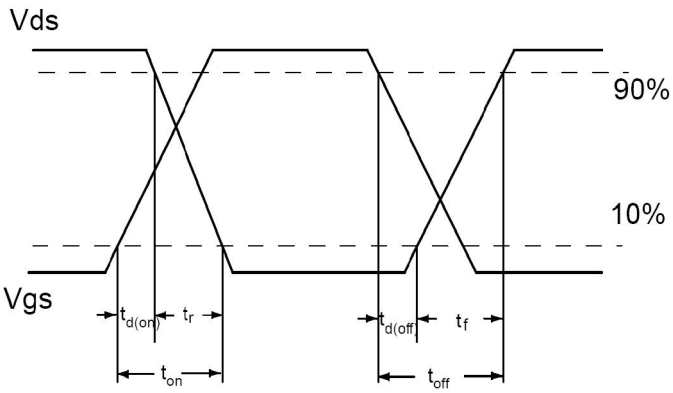
Gate charge test circuit:



Switch time test circuit:



Switch Waveforms:



Notes:

①The maximum current rating is limited by bond-wires.

②Repetitive rating; pulse width limited by max. junction temperature.

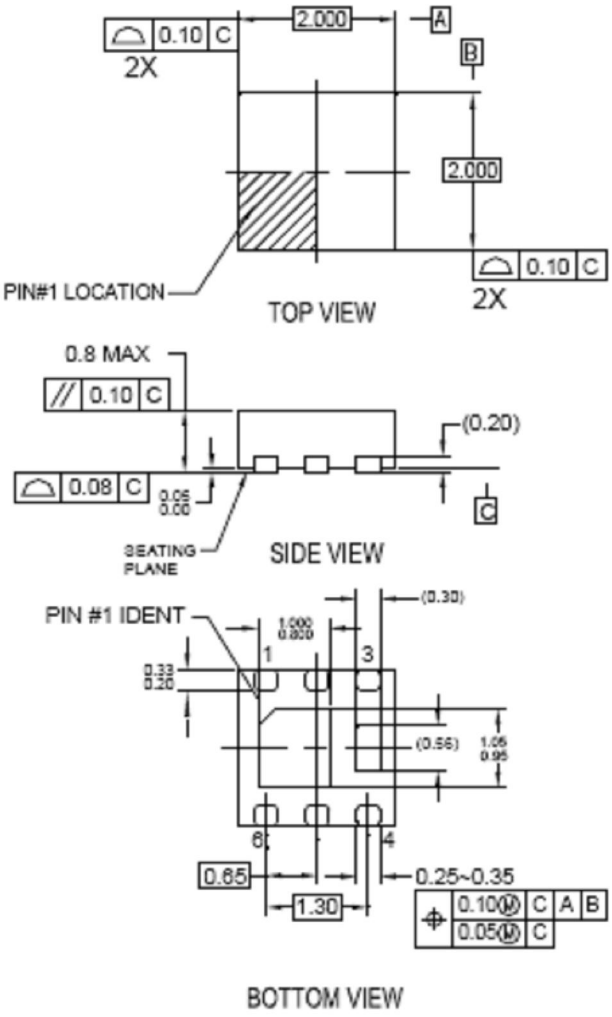
③The power dissipation PD is based on max. junction temperature, using junction-to-ambient thermal resistance.

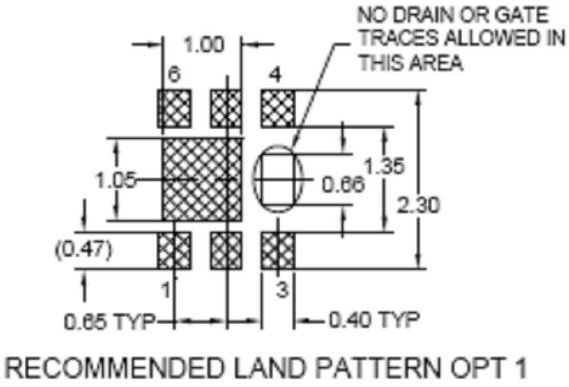
④The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C

⑤These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C.

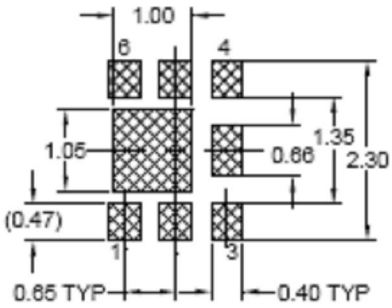
Mechanical Data

DFN 2 x 2-6L PACKAGE INFORMATION





RECOMMENDED LAND PATTERN OPT 1



RECOMMENDED LAND PATTERN OPT 2

Notes:

①Does not fully conform to JEDEC registration MO-229 dated Aug/2003.
②Dimensions are in millimeters.
③Dimensions and tolerances per ASME Y14.5M. 1994.

Ordering and Marking Information

Device Marking: 1221

Package (Available)
DFN 2x2-6L
Operating Temperature Range
C : -55 to 150 °C

Devices per Unit

Package Type	Units/ Tape	Tapes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
DFN2x2-6L	3000pcs	10pcs	15000pcs	4pcs	60000pcs

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	T_j=125℃ or 150℃ @ 80% of Max V_{DSS}/V_{CES}/VR	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	T_j=125℃ or 150℃ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices