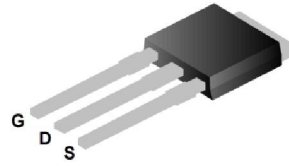
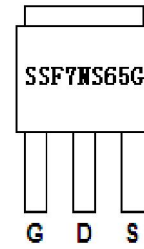


Main Product Characteristics

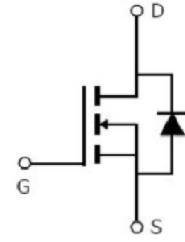
V_{DSS}	650V
$R_{DS(on)}$	0.58 Ω (typ.)
I_D	7A ①



TO-251



Marking and Pin Assignment



Schematic Diagram

Features and Benefits

- High dv/dt and avalanche capabilities
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Lead free product



Description

The SSF7NS65G series MOSFET is a new technology, which combines an innovative super junction technology and advance process. This new technology achieves low $R_{DS(ON)}$, energy saving, high reliability and uniformity, superior power density and space saving.

Absolute Max Rating

Symbol	Parameter	Max.	Units
$I_D @ TC = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	7 ①	A
$I_D @ TC = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	5 ①	
I_{DM}	Pulsed Drain Current ②	28	
$P_D @ TC = 25^\circ C$	Power Dissipation ③	83	W
	Linear Derating Factor	0.67	W/ $^\circ C$
V_{DS}	Drain-Source Voltage	650	V
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy @ L=15.2mH	68	mJ
I_{AR}	Avalanche Current @ L=15.2mH	3	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ C$

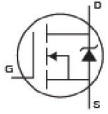
Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	1.5	$^{\circ}C/W$
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ④	—	83	$^{\circ}C/W$

Electrical Characteristics @ $T_A=25^{\circ}C$ unless otherwise specified

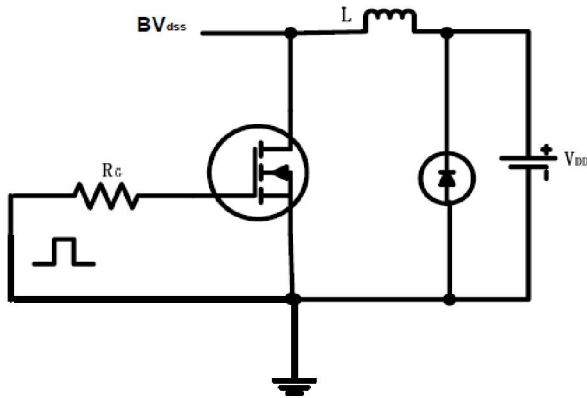
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions	
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	650	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$	
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	0.58	0.65	Ω	$V_{GS}=10V, I_D = 2.1A$ $T_J = 125^{\circ}C$	
		—	1.29	—			
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$ $T_J = 125^{\circ}C$	
		—	2.75	—			
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 650V, V_{GS} = 0V$ $T_J = 125^{\circ}C$	
		—	—	50			
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 30V$	
		—	—	-100		$V_{GS} = -30V$	
Q_g	Total gate charge	—	12.8	—	nC	$I_D = 3.2A,$ $V_{DS}=480V,$ $V_{GS} = 10V$	
Q_{gs}	Gate-to-Source charge	—	1.8	—			
Q_{gd}	Gate-to-Drain("Miller") charge	—	6.2	—			
$t_{d(on)}$	Turn-on delay time	—	10.5	—	ns	$V_{GS}=10V, V_{DS} = 400V,$ $R_L=125\Omega,$ $R_{GEN}=6.8\Omega$ $I_D = 3.2A$	
t_r	Rise time	—	5.8	—			
$t_{d(off)}$	Turn-Off delay time	—	29	—			
t_f	Fall time	—	16	—			
C_{iss}	Input capacitance	—	470	—	pF	$V_{GS} = 0V$ $V_{DS} = 100V$ $f = 1MHz$	
C_{oss}	Output capacitance	—	26.5	—			
C_{rss}	Reverse transfer capacitance	—	3.07	—			
$C_{o(er)}$	Effective output capacitance, energy related⑤	—	20	—			$V_{GS}=0V,$ $V_{DS}=0...480V$
$C_{o(tr)}$	Effective output capacitance, time related⑥	—	85	—			$I_D=constant, V_{GS}=0V$ $V_{DS}=0...480V$

Source-Drain Ratings and Characteristics

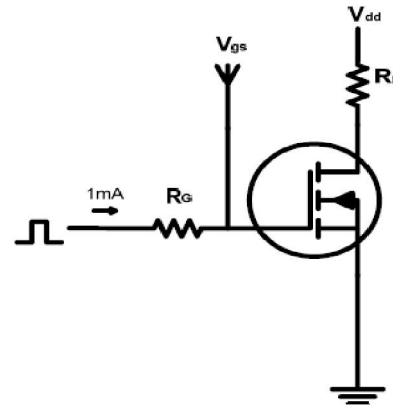
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	7 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	28	A	
V_{SD}	Diode Forward Voltage	—	0.85	1.2	V	$I_S=4.6A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	—	169	—	nS	$T_J = 25^{\circ}C, I_F = 1.2A,$ $di/dt = 100A/\mu s$
Q_{rr}	Reverse Recovery Charge	—	723	—	nC	

Test Circuits and Waveforms

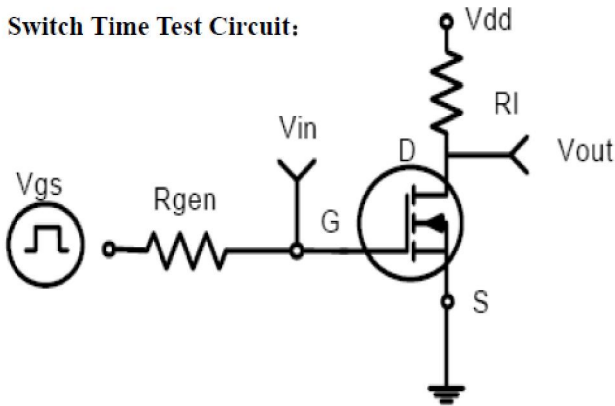
EAS test circuits:



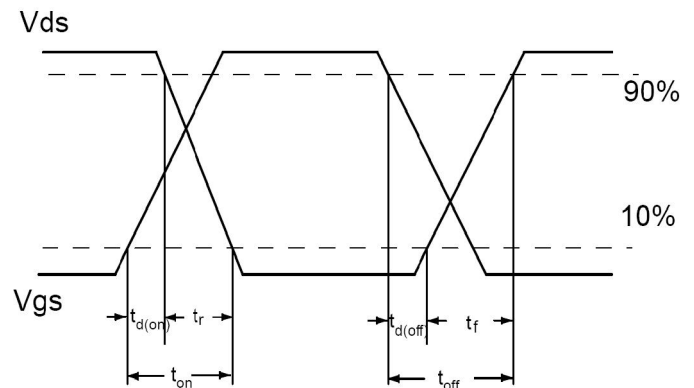
Gate charge test circuit:



Switch Time Test Circuit:



Waveforms:



Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$
- ⑤ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while VDS is rising from 0 to 80% $V_{(BR)DSS}$
- ⑥ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while VDS is rising from 0 to 80% $V_{(BR)DSS}$

Typical Electrical and Thermal Characteristics

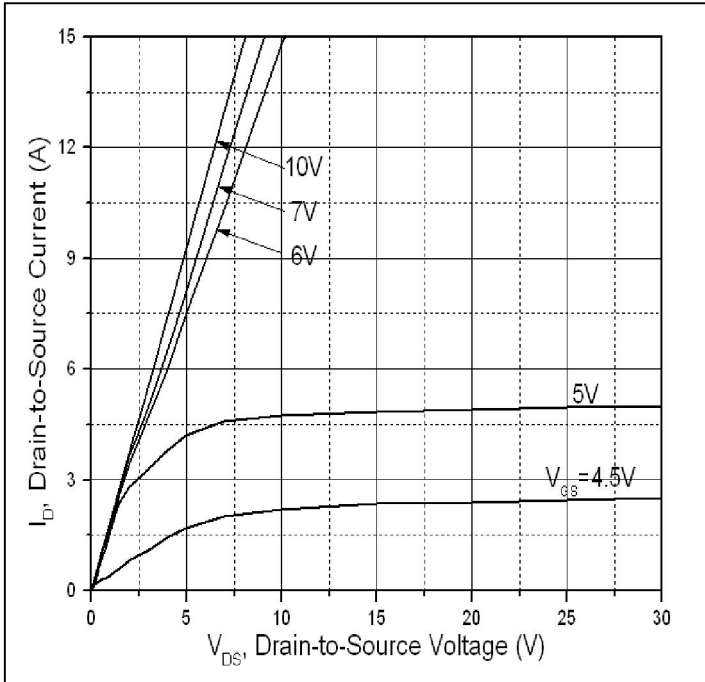


Figure 1: Typical Output Characteristics

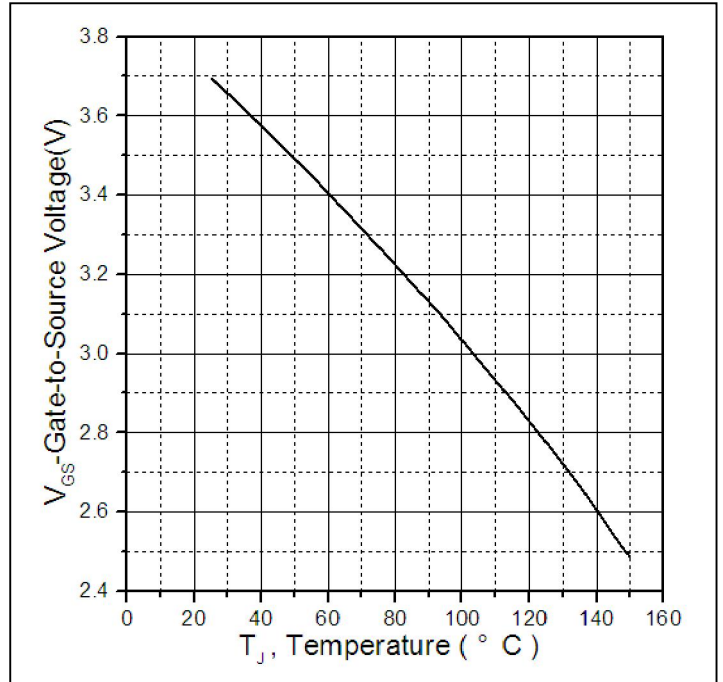


Figure 2: Gate to source cut-off voltage

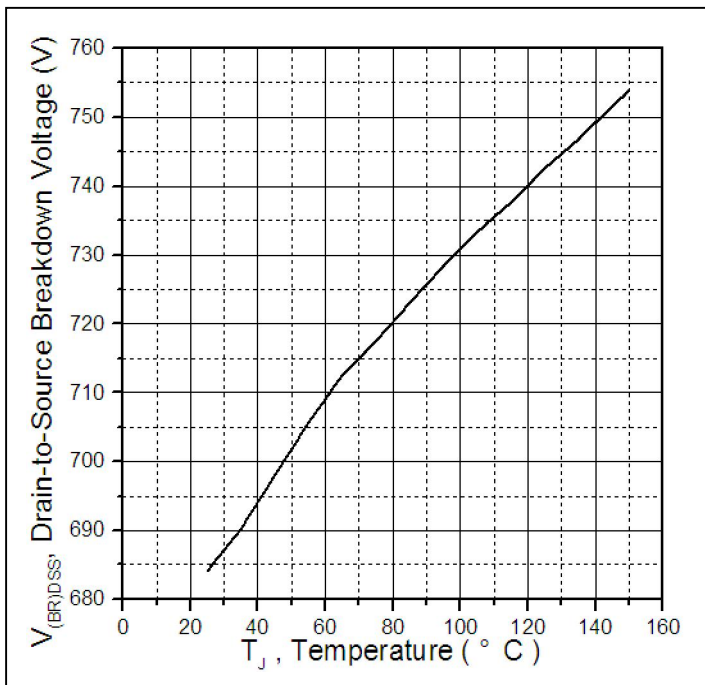


Figure 3: Drain-to-Source Breakdown Voltage Vs. Case Temperature

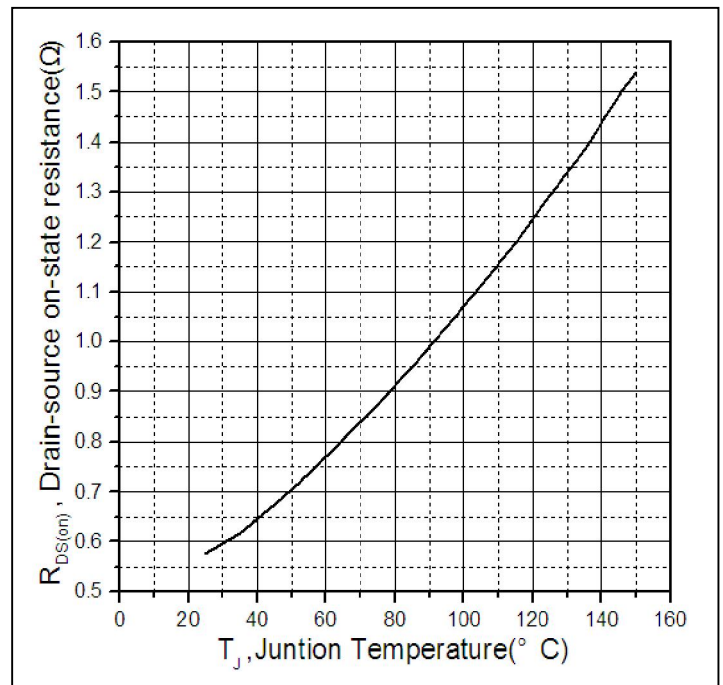


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical Electrical and Thermal Characteristics

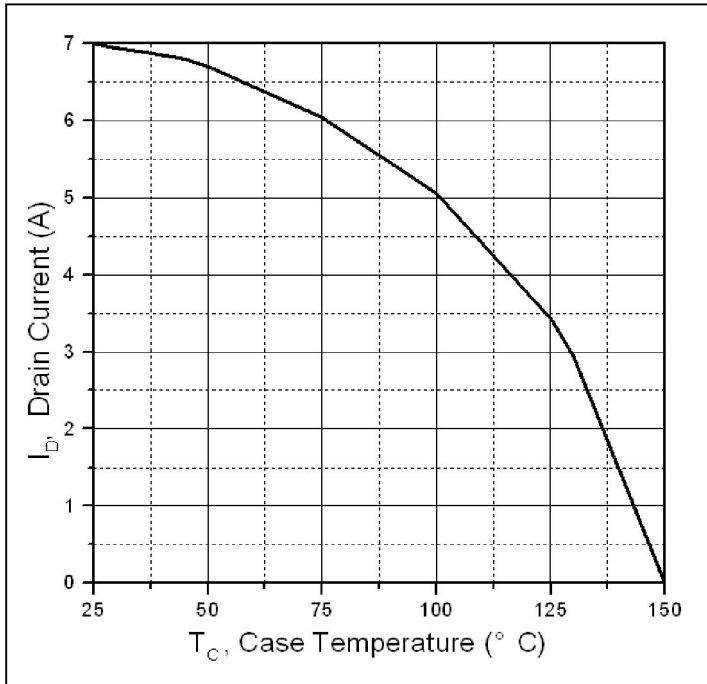


Figure 5. Maximum Drain Current Vs. Case Temperature

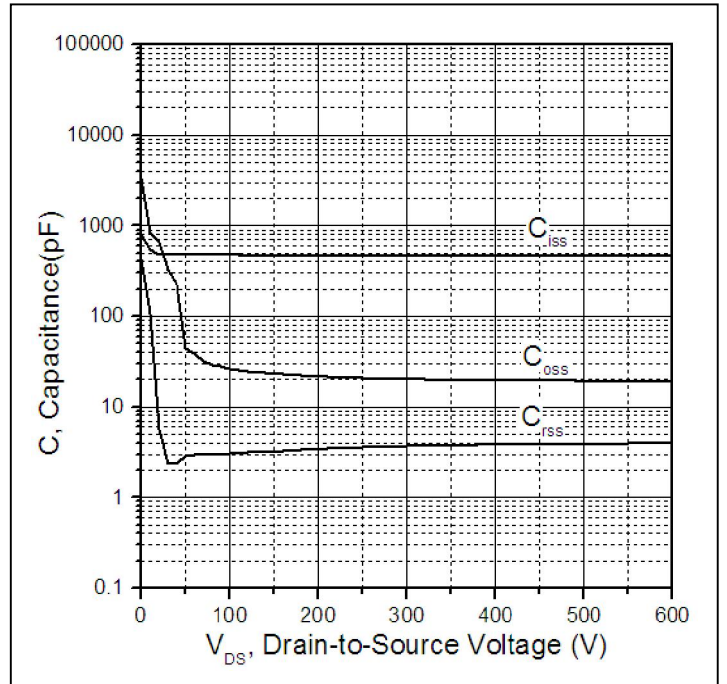


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

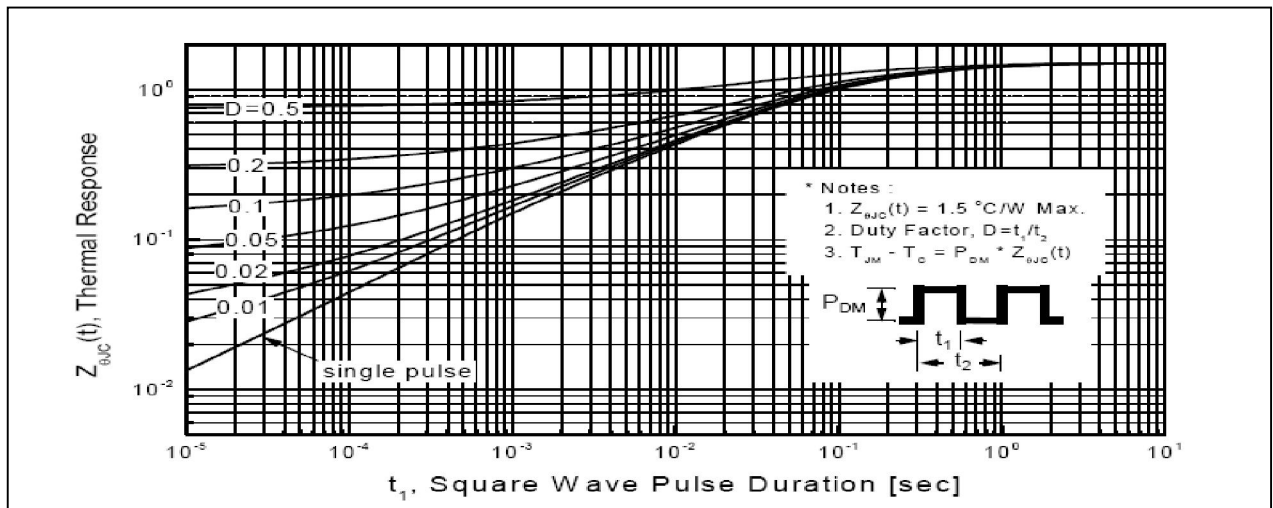
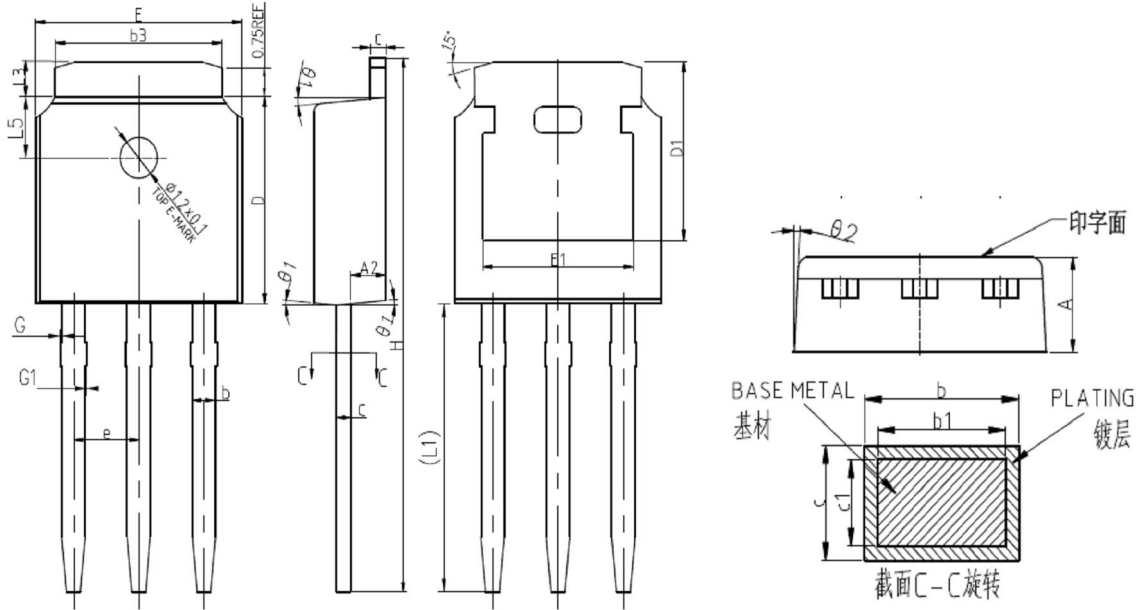


Figure7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data

TO-251 PACKAGE OUTLINE DIMENSION



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.200	2.300	2.380	0.087	0.091	0.094
A2	0.970	1.070	1.170	0.038	0.042	0.046
b	0.720	0.780	0.850	0.028	0.031	0.033
b1	0.710	0.760	0.810	0.028	0.030	0.032
b3	5.230	5.330	5.460	0.206	0.210	0.215
c	0.470	0.530	0.580	0.019	0.021	0.023
c1	0.460	0.510	0.560	0.018	0.020	0.022
D	6.000	6.100	6.200	0.236	0.240	0.244
D1	5.300REF			0.209REF		
E	6.500	6.600	6.700	0.256	0.260	0.264
E1	4.700	4.830	4.920	0.185	0.190	0.194
e	2.286BSC			0.090BSC		
H	16.100	16.400	16.600	0.634	0.646	0.654
L1	9.200	9.400	9.600	0.362	0.370	0.378
L3	0.900	1.020	1.250	0.035	0.040	0.049
L5	1.700	1.800	1.900	0.067	0.071	0.075
θ1	5°	7°	9°	5°	7°	9°
θ2	5°	7°	9°	5°	7°	9°
G	0.000		0.076	0.000	0.000	0.003
G1	0.000		0.076	0.000	0.000	0.003



Ordering and Marking Information

Device Marking: SSF7NS65G

Package (Available)
TO-251(IPAK)
Operating Temperature Range
C : -55 to 150 °C

Devices per Unit

Package Type	Units/ Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-251	80	60	4800	5	24000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to 150°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices