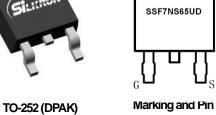
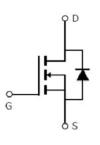


Main Product Characteristics

V _{DSS}	650V
R _{DS} (on)	0.65Ω (typ.)
I _D	7A ①







Schematic Diagram

Features and Benefits

- High dv/dt and avalanche capabilities
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



Assignment

Description

The SSF7NS65UD series MOSFETs is a new technology, which combines an innovative technology and advance process. This new technology achieves low Rdson, energy saving, high reliability and uniformity, superior power density and space saving.

Absolute Max Rating

Symbol	Parameter	Max.	Units	
I _D @ TC = 25°C	Continuous Drain Current, V _{GS} @ 10V	7 ①		
I _D @ TC = 100°C	Continuous Drain Current, V _{GS} @ 10V	5①	Α	
I _{DM}	Pulsed Drain Current ②	28		
D 070 0500	Power Dissipation ③	42	W	
P _D @TC = 25°C	Linear Derating Factor	0.33	W/°C	
V _{DS}	Drain-Source Voltage	650	V	
V _{GS}	V _{GS} Gate-to-Source Voltage		V	
E _{AS} Single Pulse Avalanche Energy @ L=100mH		480	mJ	
I _{AS}	Avalanche Current @ L=100mH	3.1	А	
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C	



Thermal Resistance

Symbol	Characteristics	Тур.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	_	3.0	°C/W
$R_{\theta JA}$	Junction-to-ambient (t \leq 10s) \oplus	_	62	°C/W

Electrical Characteristics $@T_A=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	650	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$
		_	0.65	0.75	Ω	V _{GS} =10V,I _D = 1A
D	Static Drain-to-Source on-resistance	_	1.38	_	122	T _J = 125°C
$R_{DS(on)}$	Static Dialific-Source of Fesistance	_	0.77	0.85	Ω	$V_{GS}=10V, I_{D}=4.8A$
		_	2.0	_	22	T _J = 125°C
$V_{GS(th)}$	Gate threshold voltage	2	_	4	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
V GS(th)	Gate threshold voltage	_	2.2	_	V	T _J = 125°C
1	Drain to Source leakage ourrent	1	1		$V_{DS} = 650 \text{V}, V_{GS} = 0 \text{V}$	
I _{DSS}	Drain-to-Source leakage current	_	_	50	μΑ	T _J = 125°C
1	Gate-to-Source forward leakage	_	_	100	nA	V _{GS} =30V
I _{GSS}	Gale-to-Source forward leakage	_	_	-100		V _{GS} = -30V
Q_g	Total gate charge	_	13	_		$I_D = 5A$,
Q_{gs}	Gate-to-Source charge	_	2.6	_	nC	V _{DS} =200V,
Q_{gd}	Gate-to-Drain("Miller") charge	_	3.1	_		$V_{GS} = 10V$
t _{d(on)}	Turn-on delay time	_	9.6	_		
t _r	Rise time	_	6	_	ns	V_{GS} =10V, V_{DS} =400V,
t _{d(off)}	Turn-Off delay time	_	26	_		$R_{GEN}=10.2\Omega, I_{D}=2.2A$
t _f	Fall time	_	10	_		
C _{iss}	Input capacitance	_	500	_		V _{GS} = 0V
Coss	Output capacitance	_	24	_	pF	V _{DS} = 100V
C _{rss}	Reverse transfer capacitance	_	3	_		f = 1MHz

Source-Drain Ratings and Characteristics

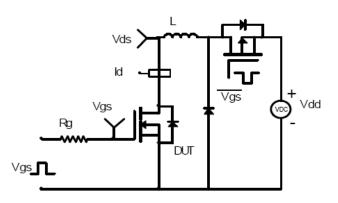
Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
	Continuous Source Current			7 ①	А	MOSFET symbol
I _S	(Body Diode)	_				showing the
I _{SM}	Pulsed Source Current		_	28	А	integral reverse
	(Body Diode)	_				p-n junction diode.
V _{SD}	Diode Forward Voltage	_	0.85	1.2	V	I _S =4.8A, V _{GS} =0V
t _{rr}	Reverse Recovery Time	_	111	_	nS	$T_J = 25^{\circ}C, I_F = 2.2A,$
Q _{rr}	Reverse Recovery Charge	_	639	_	nC	di/dt = 100A/µs

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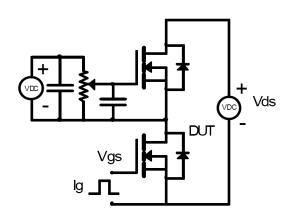


Test circuits and Waveforms

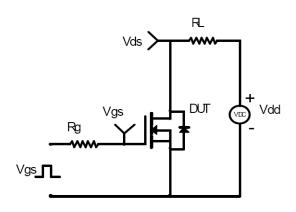
EAS Test Circuit:



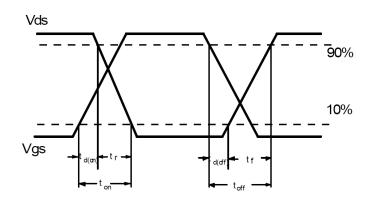
Gate charge test circuit:



Switching Time Test Circuit:



Switching Waveforms:

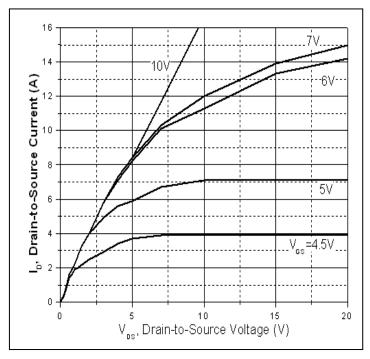


Notes:

- ①Calculated continuous current based on maximum allowable junction temperature.
- ②Repetitive rating; pulse width limited by max. junction temperature.
- ③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- 4The value of $R_{\texttt{9JA}}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C



Typical electrical and thermal characteristics



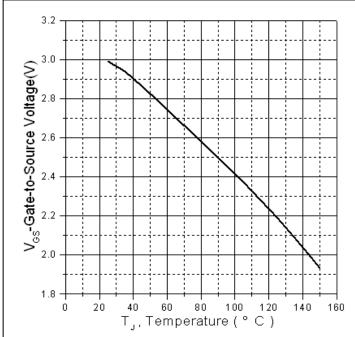


Figure 1.Typical Output Characteristics

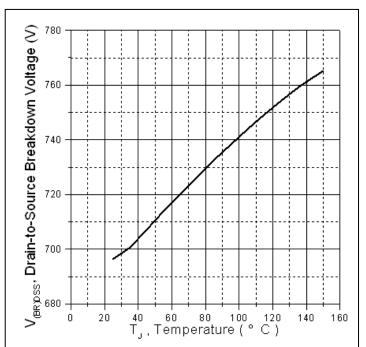


Figure 3. Drain-to-Source Breakdown Voltage Vs.

Case Temperature

Figure 2. Gate to source cut-off voltage

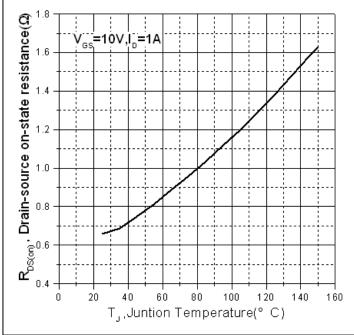


Figure 4.Normalized On-Resistance Vs. Case Temperature



Typical electrical and thermal characteristics

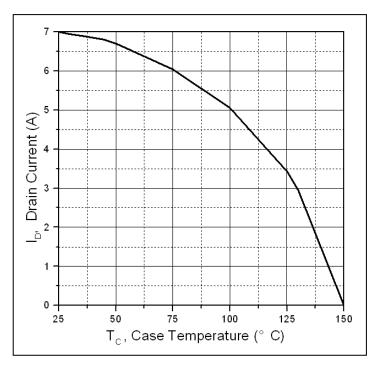


Figure 5. Maximum Drain Current Vs. Case Temperature

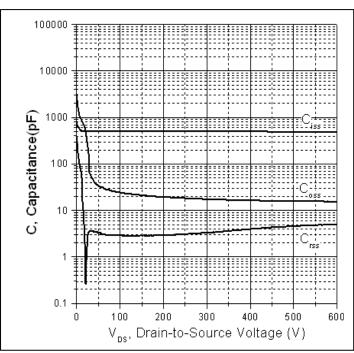


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

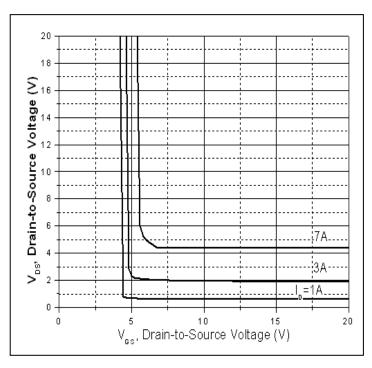


Figure7. Drain-to-Source Voltage Vs. Gate-to-Source Voltage

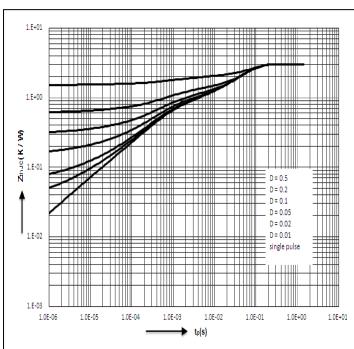
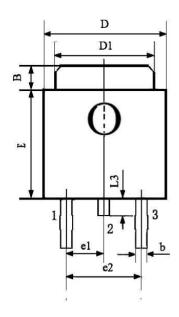


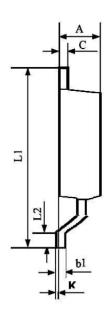
Figure8. Maximum Effective Transient Thermal Impedance, Junction-to-Case



Mechanical Data

TO-252 PACKAGE OUTLINE DIMENSION





Symbol	Dimension In Millimeters			Dimension In Inches		
Symbol	Min	Nom	Max	Min	Nom	Max
Α	2.200	-	2.400	0.087	-	0.094
В	0.950	-	1.250	0.037	-	0.049
b	0.500	-	0.700	0.020	-	0.028
b1	0.450	-	0.550	0.018	-	0.022
С	0.450	-	0.550	0.018	-	0.022
D	6.450	-	6.750	0.254	-	0.266
D1	5.200	-	5.400	0.205	-	0.213
Е	5.950	-	6.250	0.234	-	0.246
e1	2.240	-	2.340	0.088	-	0.092
e2	4.430	-	4.730	0.174	-	0.186
L1	9.450	-	9.950	0.372	-	0.392
L2	1.250	-	1.750	0.049	-	0.069
L3	0.600	-	0.900	0.024	-	0.035
K	0.000	-	0.100	0.000	-	0.004





Ordering and Marking Information

Device Marking: SSF7NS65UD

Package (Available)
TO-252(DPAK)
Operating Temperature Range
C: -55 to 150 °C

Devices per Unit (options)

Package	Units/Tape	Tapes/Inner	Units/Inner	Inner	Units/Carton
Type		Box	Box	Boxes/Carton	Box
				Box	
TO-252	2500	2	5000	7	35000
TO-252	2500	1	2500	10	25000
TO-252	800	5	4000	8	32000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High	T _j =125℃ to 150℃ @	168 hours	3 lots x 77 devices
Temperature	80% of Max	500 hours	
Reverse	V _{DSS} /V _{CES} /VR	1000 hours	
Bias(HTRB)			
High	T _j =150℃ @ 100% of	168 hours	3 lots x 77 devices
Temperature	Max V _{GSS}	500 hours	
Gate		1000 hours	
Bias(HTGB)			

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