

**FEATURES**

- Filterless mono, digital input Class-D amplifier**
- I<sup>2</sup>C control interface**
- Serial digital audio interface supports common formats (I<sup>2</sup>S, PCM, LJ, RJ, TDM1-16, PDM)**
- Supports wide range of sample rates: 8.0 kHz to 96.0 kHz**
- MCLK and BCLK can be provided by built-in phase-locked loop (PLL)**
- Supports single power supply mode; DVDD can be provided by built-in low dropout (LDO) regulator**
- 2.5 V to 5.5 V SPKVDD operating supply voltage**
- 1.08 V to 1.98 V DVDD operating supply voltage**
- Support off-chip volume control without I<sup>2</sup>C**
- 2.4 W into 4  $\Omega$  and 1.4 W into 8  $\Omega$  at 5 V supply with <1% THD + N**
- Available in a 16-ball, 1.92 mm  $\times$  1.94 mm, 0.4 mm pitch WLCSP**
- Efficiency 95% at full scale into 8  $\Omega$**
- Signal-to-noise ratio (SNR): 103 dB, A-weighted**
- Power supply rejection ratio (PSRR): >80 dB at 217 Hz**
- Digital volume control: -70 dB to +24 dB in 0.375 dB steps**
- Ultralow idle current**
- Autosample rate detection**
- Pop-and-click suppression**
- Short-circuit and thermal protection with programmable autorecovery**
- Supports smart power-down when no input signal is detected**
- Power-on reset and UVLO voltage monitoring**
- Selectable ultralow EMI emission mode**
- Supports SPKVDD voltage monitor**
- Digital audio processing**
  - 7-band programmable equalizer**
  - Programmable dynamic range compression (DRC) with noise gate, expander, compressor, and limiter**

**APPLICATIONS**

- Mobile phones**
- Portable media players**
- Laptop PCs**
- Wireless speakers**
- Portable gaming**
- Navigation systems**

**GENERAL DESCRIPTION**

The **SSM2529** is a digital input, Class-D power amplifier that combines a digital-to-analog converter (DAC), a low power audio specific digital signal processor, and a sigma-delta ( $\Sigma$ - $\Delta$ ) Class-D modulator.

This unique architecture enables extremely low real-world power consumption from digital audio sources with excellent audio performance. The **SSM2529** is ideal for power sensitive applications, such as mobile phones and portable media players, where system noise can corrupt small analog signals that are sent to an analog input audio amplifier.

Using the **SSM2529**, audio data can be transmitted to the amplifier over a standard digital audio serial interface, thereby significantly reducing the effect of noise sources such as GSM interference or other digital signals on the transmitted audio. The closed-loop digital input design retains the benefits of an all-digital amplifier, yet enables very good PSRR and audio performance. The three-level,  $\Sigma$ - $\Delta$  Class-D modulator is designed to provide the least amount of EMI, the lowest quiescent power dissipation, and the highest audio efficiency without sacrificing audio quality.

The audio input is provided via a serial audio interface that can be programmed to accept all common audio formats, including I<sup>2</sup>S, TDM, and PDM. Control of the IC is provided via an I<sup>2</sup>C control interface. An alternative to I<sup>2</sup>C control is standalone operation mode, which allows several settings that are adjusted by off-chip external resistors. The **SSM2529** can accept a variety of input MCLK frequencies and can use BCLK as the clock source in some configurations. An integrated PLL can also provide the device master clock.

The integrated DSP includes soft digital volume control circuits; a de-emphasis, high-pass filter; a seven-band programmable equalizer; and a programmable digital dynamic range compressor. In addition, the part includes a feedforward speaker temperature prediction module to protect the loudspeaker.

The **SSM2529** supports single-supply mode, where DVDD is provided by the on-chip LDO regulator, eliminating the need for an external digital core supply.

The digital interface is very flexible and convenient. It can offer a better system solution for other products whose sole audio source is digital, such as wireless speakers, laptop PCs, portable digital televisions, and navigation systems.

The **SSM2529** is specified over the industrial temperature range of -40°C to +85°C. It has built-in thermal shutdown and output short-circuit protection. It is available in a 16-ball, 1.92 mm  $\times$  1.94 mm wafer level chip scale package (WLCSP).

**Rev. 0**

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**REVISION HISTORY**

7/12—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

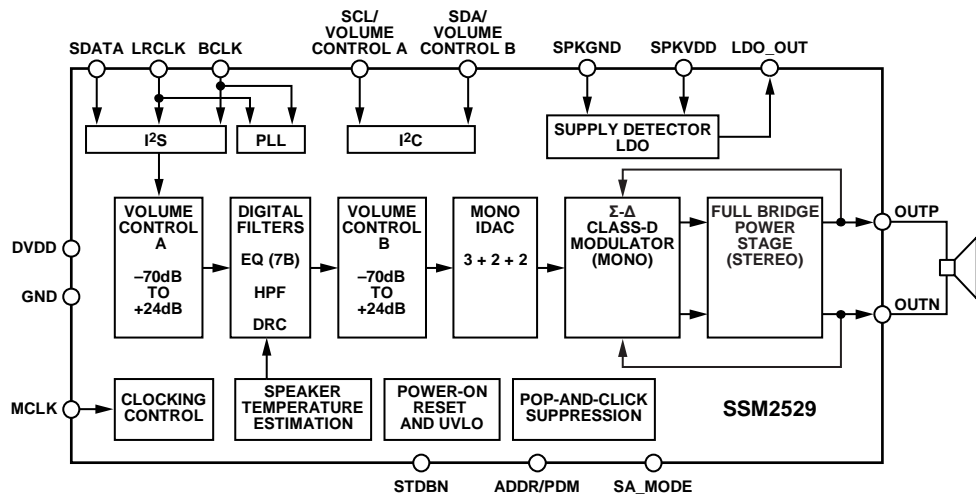


Figure 1.

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## SPECIFICATIONS

Standard test condition: SPKVDD = 4.2 V; DVDD = 1.8 V;  $f_s = 48$  kHz; MCLK =  $128 \times f_s$ ;  $T_A = 25^\circ\text{C}$ ;  $R_L = 8 \Omega + 33 \mu\text{H}$ ; LP\_MODE = 0; 0 dB volume control setting, unless otherwise noted.

### PERFORMANCE SPECIFICATIONS

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power	$P_{\text{OUT}}$	f = 1 kHz, BW = 20 kHz				
		$R_L = 4 \Omega$ , THD = 1%, SPKVDD = 5.0 V		2.4		W
		$R_L = 4 \Omega$ , THD = 10%, SPKVDD = 5.0 V		3.1		W
		$R_L = 8 \Omega$ , THD = 1%, SPKVDD = 5.0 V		1.4		W
		$R_L = 8 \Omega$ , THD = 10%, SPKVDD = 5.0 V		1.8		W
		$R_L = 4 \Omega$ , THD = 1%, SPKVDD = 4.2 V		1.7		W
		$R_L = 4 \Omega$ , THD = 10%, SPKVDD = 4.2 V		2.2		W
		$R_L = 8 \Omega$ , THD = 1%, SPKVDD = 4.2 V		0.95		W
		$R_L = 8 \Omega$ , THD = 10%, SPKVDD = 4.2 V		1.2		W
		$R_L = 4 \Omega$ , THD = 1%, SPKVDD = 3.6 V		1.2		W
		$R_L = 4 \Omega$ , THD = 10%, SPKVDD = 3.6 V		1.6		W
		$R_L = 8 \Omega$ , THD = 1%, SPKVDD = 3.6 V		0.7		W
		$R_L = 8 \Omega$ , THD = 10%, SPKVDD = 3.6 V		0.9		W
		$R_L = 4 \Omega$ , THD = 1%, SPKVDD = 2.5 V		0.55		W
		$R_L = 4 \Omega$ , THD = 10%, SPKVDD = 2.5 V		0.72		W
		$R_L = 8 \Omega$ , THD = 1%, SPKVDD = 2.5 V		0.32		W
		$R_L = 8 \Omega$ , THD = 10%, SPKVDD = 2.5 V		0.42		W
Efficiency	$\eta$	$P_{\text{OUT}} = 2$ W into 4 $\Omega$ , SPKVDD = 5.0 V		91		%
		$P_{\text{OUT}} = 1.4$ W into 8 $\Omega$ , SPKVDD = 5.0 V, normal operation		95		%
		$P_{\text{OUT}} = 1.4$ W into 8 $\Omega$ , SPKVDD = 5.0 V, ultralow EMI operation		86		%
Total Harmonic Distortion Plus Noise	THD + N	$P_{\text{OUT}} = 1$ W into 8 $\Omega$ , f = 1 kHz, SPKVDD = 5.0 V		0.03		%
		$P_{\text{OUT}} = 0.7$ W into 8 $\Omega$ , f = 1 kHz, SPKVDD = 4.2 V		0.03		%
		$P_{\text{OUT}} = 0.5$ W into 8 $\Omega$ , f = 1 kHz, SPKVDD = 3.6 V		0.03		%
Average Switching Frequency	$f_{\text{SW}}$			280		kHz
Differential Output Offset Voltage	$V_{\text{OOS}}$			2.0		mV
Power Supply Rejection Ratio	PSRR (DC)	SPKVDD = 2.5 V to 5.0 V	70	80		dB
	PSRR <sub>GSM</sub>	$V_{\text{RIPPLE}} = 100$ mV rms at 217 Hz, dither input		80		dB
Supply Current	$I_{\text{SPKVDD}}$	Dither input, SPKVDD = 5.0 V		3.0		mA
		Dither input, SPKVDD = 4.2 V		2.8		mA
		Dither input, SPKVDD = 3.6 V		2.7		mA
		Dither input, SPKVDD = 2.5 V		2.4		mA
		Power-down		100		nA
Supply Current	$I_{\text{DVDD}}$	Dither input, DVDD = 1.8 V		0.6		mA
		Dither input, DVDD = 1.08 V		0.3		mA
		Power-down		2		$\mu\text{A}$
Output Voltage Noise	$e_n$	f = 20 Hz to 20 kHz, dither input		22		$\mu\text{V}$
Signal-to-Noise Ratio	SNR	A-weighted reference to 0 dBFS, SPKVDD = 4.2 V		103		dB
Mute Attenuation		Soft mute on	100			dB

**POWER SUPPLY REQUIREMENTS**

Table 2.

Parameter	Min	Typ	Max	Unit
SPKVDD	2.5	4.2	5.5	V
DVDD	1.08	1.8	1.98	V

**DIGITAL INPUT/OUTPUT**

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Input Voltage, High	$V_{IH}$		$0.7 \times DVDD$		3.6	V
Input Voltage, Low	$V_{IL}$		-0.3		$+0.3 \times DVDD$	V
Input Leakage Current, High	$I_{IH}$	Excluding MCLK			1	$\mu A$
Input Leakage Current, Low	$I_{IL}$	Excluding MCLK and bidirectional pins			1	$\mu A$
MCLK Input Leakage, High	$I_{IH}$				3	$\mu A$
MCLK Input Leakage, Low	$I_{IL}$				3	$\mu A$
Input Capacitance					5	pF

**DIGITAL INTERPOLATION FILTER**

Table 4.

Parameter	Mode	Factor	Min	Typ	Max	Unit
Pass Band (-3 dB)	48 kHz mode, typical at 48 kHz	$0.423 f_s$		20		kHz
Pass-Band Ripple	48 kHz mode, typical at 48 kHz	$0.5 f_s$			$\pm 0.03$	dB
Transition Band	48 kHz mode, typical at 48 kHz			24		kHz
Stop Band	48 kHz mode, typical at 48 kHz	$0.582 f_s$		28		kHz
Stop Band Attenuation	48 kHz mode, typical at 48 kHz		60			dB
Group Delay	48 kHz mode, typical at 48 kHz	$14/f_s$		292		$\mu s$

**DIGITAL TIMING**

All timing specifications are given for the default setting (I<sup>2</sup>S mode) of the serial input port.

Table 5.

Parameter	Limit		Unit	Description
	$T_{MIN}$	$T_{MAX}$		
MASTER CLOCK (See Figure 2)				
$t_{BP}$	74	136	ns	MCLK period, 256 $f_s$ mode
$t_{BP}$	148	271	ns	MCLK period, 128 $f_s$ mode
SERIAL PORT (See Figure 2)				
$t_{BIL}$	40		ns	BCLK low pulse width
$t_{BIH}$	40		ns	BCLK high pulse width
$t_{LIS}$	10		ns	LRCLK setup; time to BCLK rising
$t_{LIH}$	10		ns	LRCLK hold; time from BCLK rising
$t_{SIS}$	10		ns	SDATA setup; time to BCLK rising
$t_{SIH}$	10		ns	SDATA hold; time from BCLK rising

Parameter	Limit		Unit	Description
	T <sub>MIN</sub>	T <sub>MAX</sub>		
<b>I<sup>2</sup>C PORT (See Figure 3)</b>				
f <sub>SCL</sub>		400	kHz	SCL frequency (not shown in Figure 3)
t <sub>SCLH</sub>	0.6		μs	SCL high
t <sub>SCLL</sub>	1.3		μs	SCL low
t <sub>SCS</sub>	0.6		μs	Setup time, relevant for repeated start condition
t <sub>SCH</sub>	0.6		μs	Hold time; after this period, the first clock is generated
t <sub>DS</sub>	100		ns	Data setup time
t <sub>SCR</sub>		300	ns	SCL rise time
t <sub>SCF</sub>		300	ns	SCL fall time
t <sub>SDR</sub>		300	ns	SDA rise time (not shown in Figure 3)
t <sub>SDF</sub>		300	ns	SDA fall time (not shown in Figure 3)
t <sub>BFT</sub>	0.6		μs	Bus-free time; time between stop and start

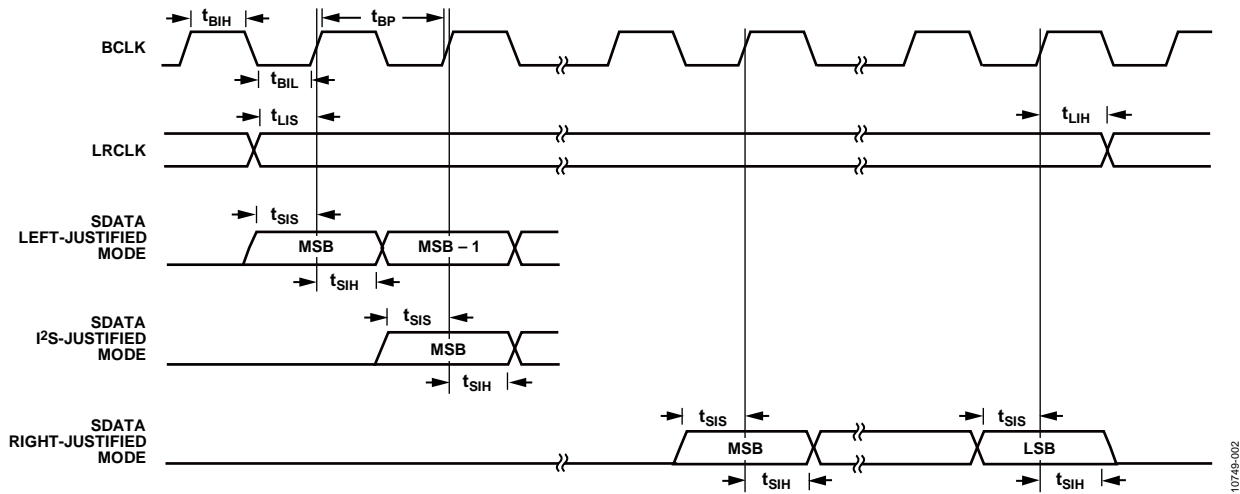


Figure 2. Serial Input Port Timing

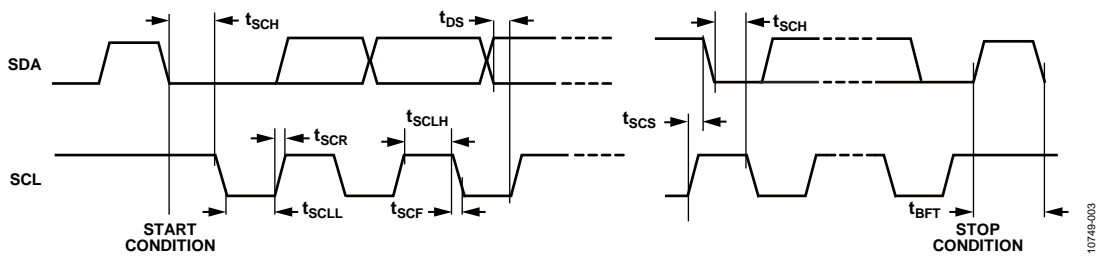


Figure 3. I<sup>2</sup>C Port Timing

## ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
SPKVDD Supply Voltage	−0.3 V to +5.5 V
DVDD Supply Voltage	−0.3 V to +1.98 V
Input Voltage (Signal Source)	−0.3 V to +3.6 V
ESD Susceptibility	4 kV
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	$\theta_{JA}$	Unit
16-Ball, 1.92 mm × 1.94 mm WLCSP	56.1	°C/W

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

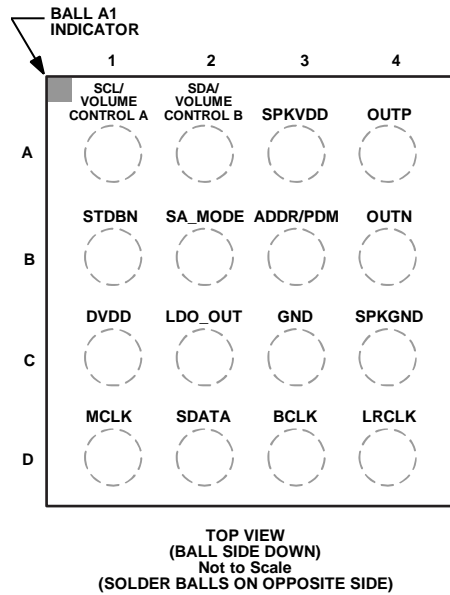


Figure 4. Pin Configuration

Table 8. Pin Function Descriptions

Pin Number	Mnemonic	Function	Description
A1	SCL/VOLUME CONTROL A	Input	I <sup>2</sup> C Clock in I <sup>2</sup> C Mode/Volume Controller A in Standalone Mode
A2	SDA/VOLUME CONTROL B	Input/Output	I <sup>2</sup> C Data in I <sup>2</sup> C Mode/Volume Controller B in Standalone Mode
A3	SPKVDD	Power	2.5 V to 5.5 V Amplifier Power
A4	OUTP	Output	Positive Output
B1	STDBN	Input	Power-Down Control; Active Low
B2	SA_MODE	Input	Standalone and Hardware Selection; 1 = Standalone Mode
B3	ADDR/PDM	Input	I <sup>2</sup> C Chip Address Select/Input Interface Select in Standalone Mode
B4	OUTN	Output	Negative Output
C1	DVDD	Power	Digital Power
C2	LDO_OUT	Power	LDO Output
C3	GND	Power	Digital and Analog Ground
C4	SPKGND	Power	Amplifier Ground
D1	MCLK	Input	Serial Audio Interface Master Clock and I <sup>2</sup> S/TDM/PDM Channel Select
D2	SDATA	Input	I <sup>2</sup> S Serial Data/PDM Data
D3	BCLK	Input	I <sup>2</sup> S Bit Clock/PDM Clock
D4	LRCLK	Input	I <sup>2</sup> S Left-Right Frame Clock

TYPICAL PERFORMANCE CHARACTERISTICS

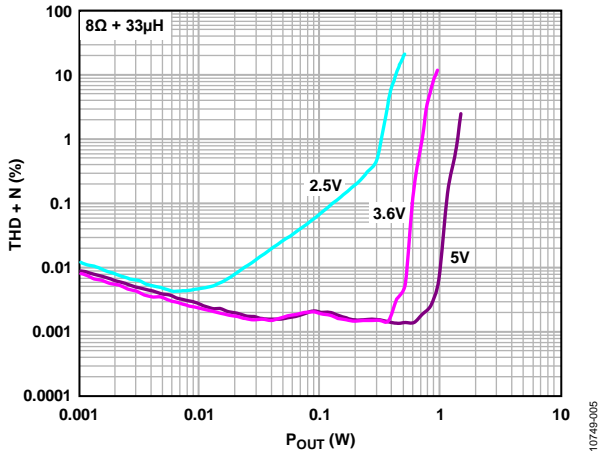


Figure 5. THD + N vs. Output Power into 8Ω, 5.0 V Gain Setting

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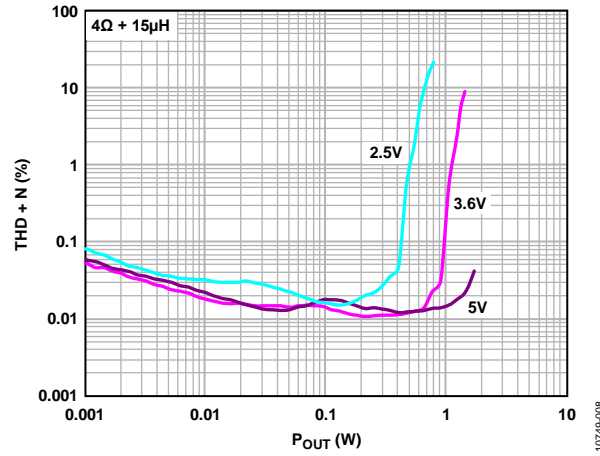


Figure 8. THD + N vs. Output Power into 4Ω, 3.6 V Gain Setting

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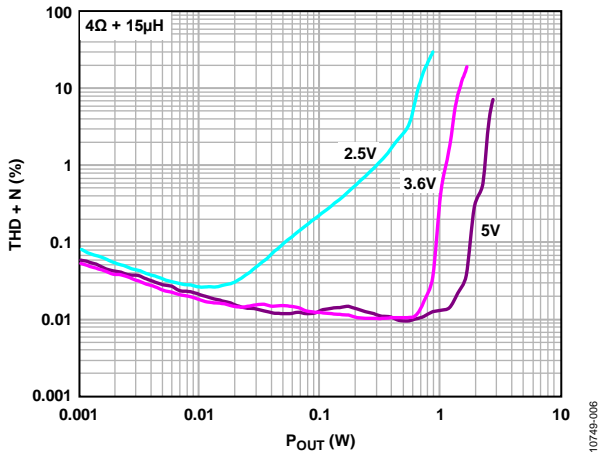


Figure 6. THD + N vs. Output Power into 4Ω, 5.0 V Gain Setting

10749-006

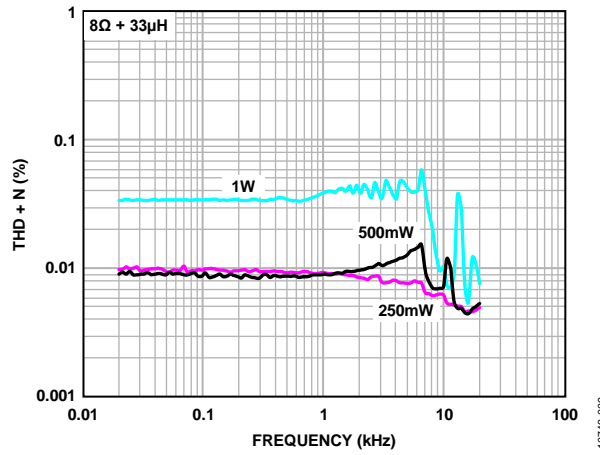


Figure 9. THD + N vs. Frequency into 8Ω, SPKVDD = 5.0 V

10749-009

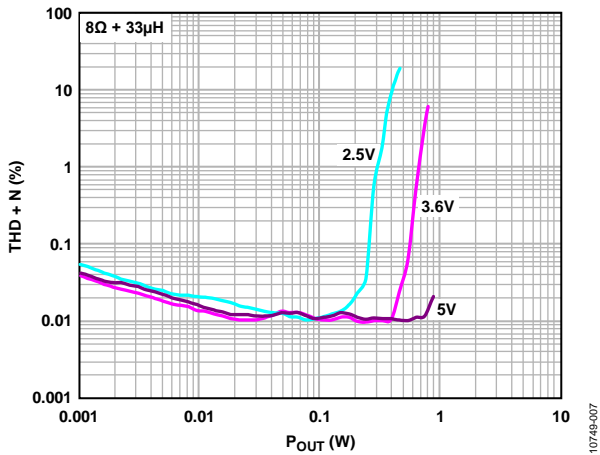


Figure 7. THD + N vs. Output Power into 8Ω, 3.6 V Gain Setting

10749-007

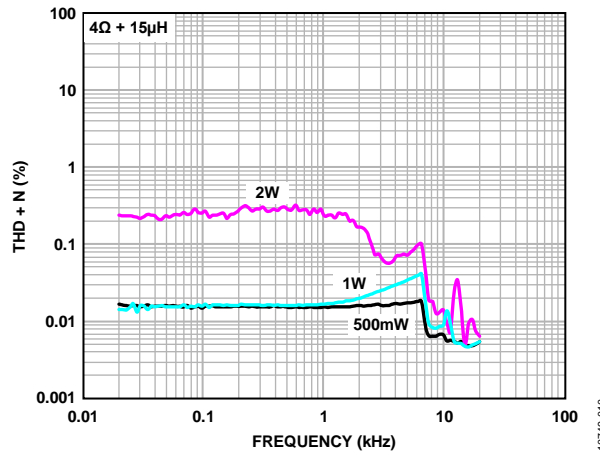


Figure 10. THD + N vs. Frequency into 4Ω, SPKVDD = 5.0 V

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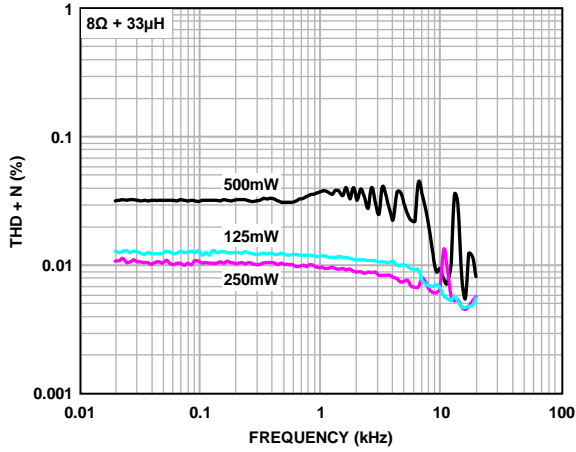


Figure 11. THD + N vs. Frequency into 8 Ω, SPKDD = 3.6 V

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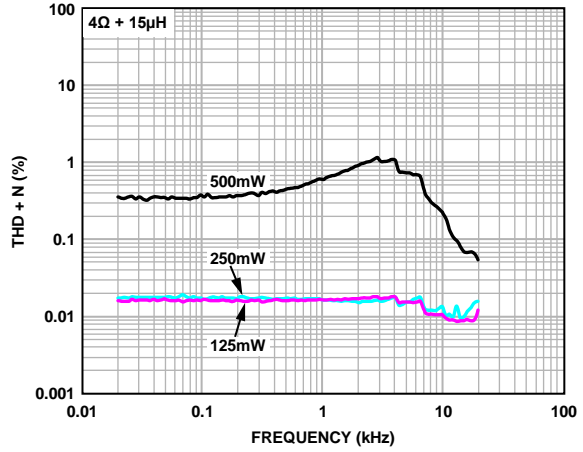


Figure 14. THD + N vs. Frequency into 4 Ω, SPKDD = 2.5 V

10749-014

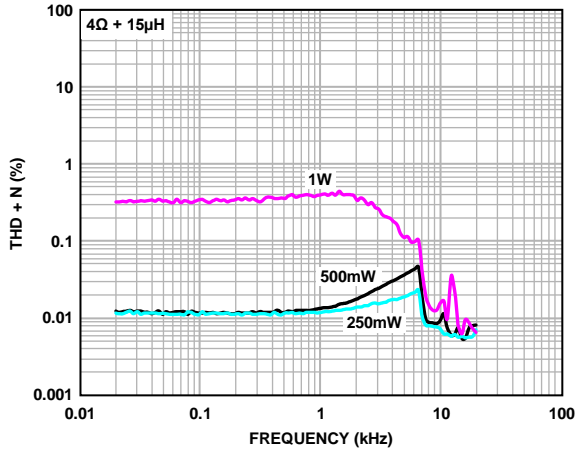


Figure 12. THD + N vs. Frequency into 4 Ω, SPKDD = 3.6 V

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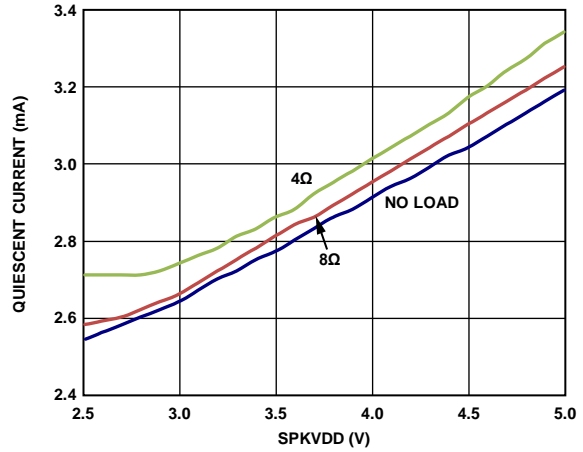


Figure 15. Quiescent Current (Power Stage) vs. Supply Voltage

10749-015

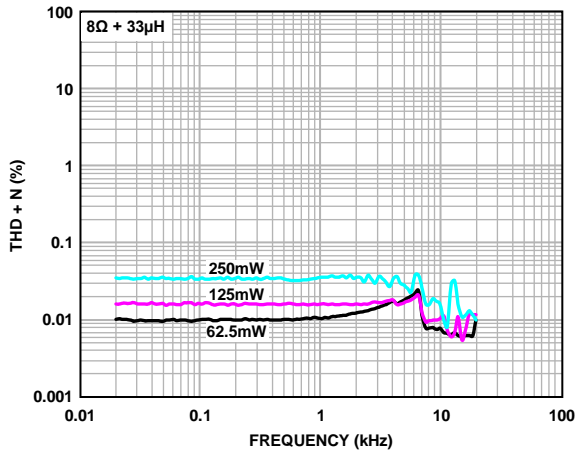


Figure 13. THD + N vs. Frequency into 8 Ω, SPKDD = 2.5 V

10749-013

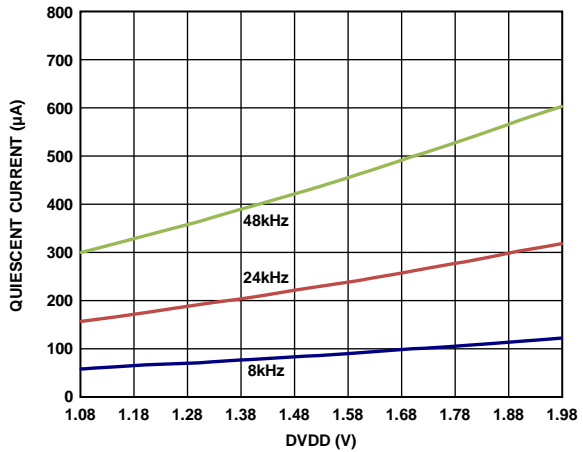


Figure 16. Quiescent Current (Digital Core) vs. Supply Voltage

10749-017

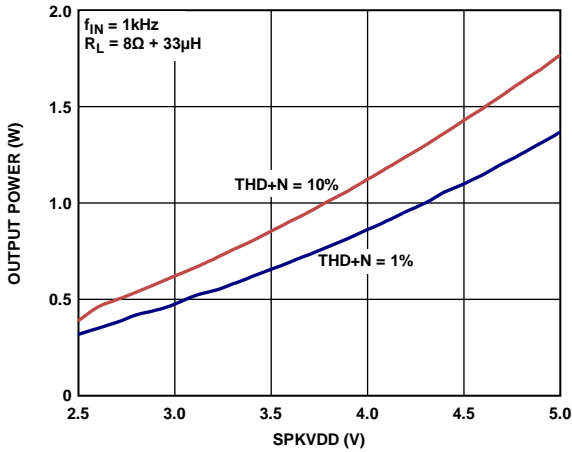


Figure 17. Maximum Output Power vs. Supply Voltage,  $R_L = 8 \Omega$

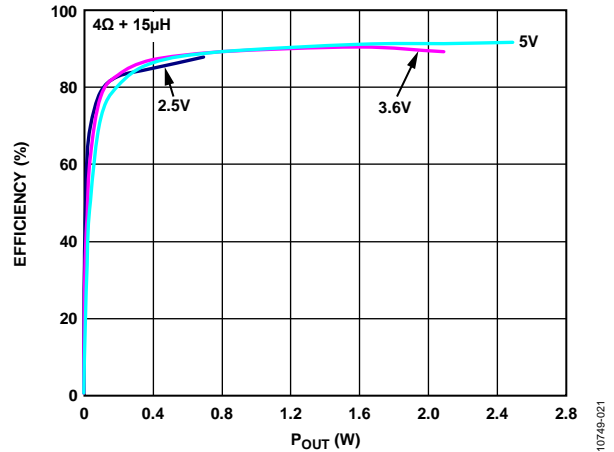


Figure 20. Efficiency vs. Output Power into  $4 \Omega$

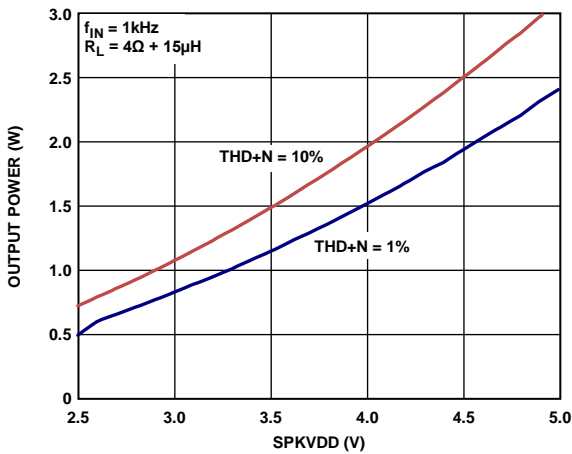


Figure 18. Maximum Output Power vs. Supply Voltage,  $R_L = 4 \Omega$

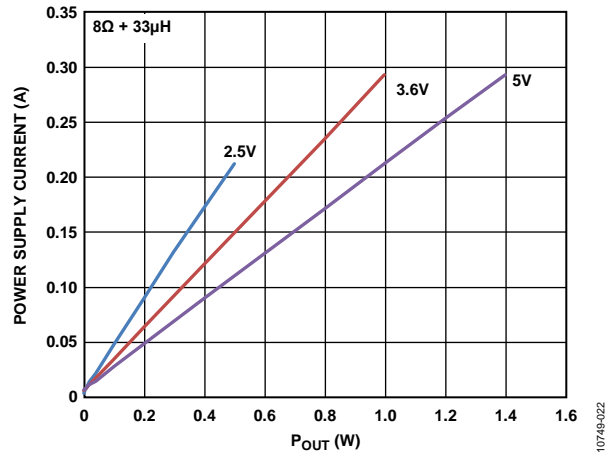


Figure 21. Power Supply Current vs. Output Power,  $R_L = 8 \Omega$

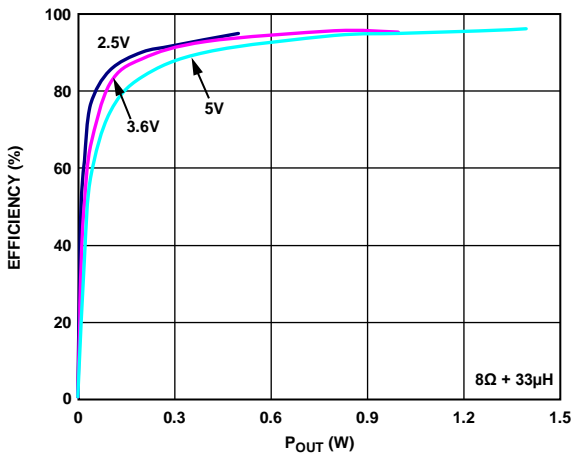


Figure 19. Efficiency vs. Output Power into  $8 \Omega$

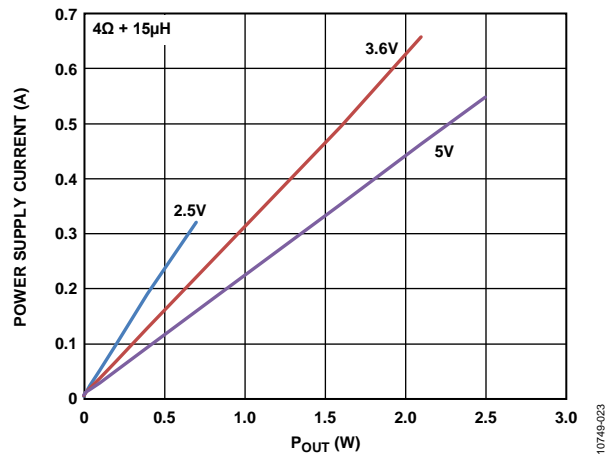


Figure 22. Power Supply Current vs. Output Power,  $R_L = 4 \Omega$

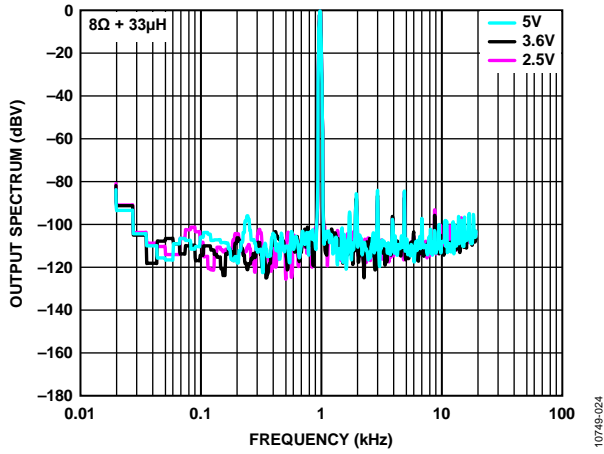


Figure 23. Output Spectrum vs. Frequency  
(FFT with 100 mW Output Power into 8 Ω Load)

10749-024

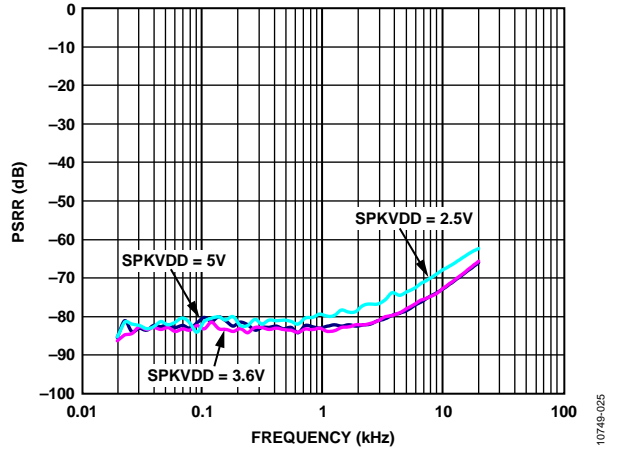


Figure 24. PSRR vs. Frequency

10749-025

## THEORY OF OPERATION

### OVERVIEW

The [SSM2529](#) is a fully integrated, mono, digital switching audio amplifier. The [SSM2529](#) receives digital audio inputs and produces the PDM differential switching outputs using the internal power stage. The part has built-in protections for overtemperature and overcurrent conditions. The [SSM2529](#) also has built-in soft turn-on and soft turn-off for pop-and-click suppression. The part has programmable register control via the I<sup>2</sup>C port.

### MASTER CLOCK

In master mode, the built-in PLL can provide the master clock. In slave mode, the [SSM2529](#) receives an external clock at the MCLK or BCLK input pin. The external clock must be fully synchronous with the incoming digital audio on the serial interface. The internal clock for the [SSM2529](#) always runs at 5.6448 MHz to 8.192 MHz, depending on the input sample rate. The three options for providing the master clock to the part are as follows:

- Using the clock generated by the built-in PLL
- Using the BCLK pin
- Using the MCLK pin

The MCLK option can use the built-in PLL or the BCLK pin to generate the internal clock as long as the clock is provided at the same rate that is required by the MCLK pin. By setting the PLEN bit in Register 0x0E, this is enabled. In this case, there is no need to provide the master clock to the MCLK pin, which in turn saves a pin connection from the audio source. If using the MCLK pin, various multiples of the sample frequency can be used for MCLK. See Table 48 for all available options and settings. When the [SSM2529](#) enters its power-down state, it is possible to gate this clock to further conserve system power. However, an MCLK must be present for the audio amplifier to operate. The input MCLK rate is determined by setting the MCS bits in Register 0x00. For more information, see Table 48.

### INTERNAL CLOCK GENERATOR

The digital core clock can be derived directly from the external clock, or it can be generated using the PLL. Clocks for the DSPs, the serial ports, and the converters are derived from the core clock. The core clock rate is always an integer multiple of the sample rate used for the part.

The clock generation block is composed of a digital PLL and an analog PLL. The analog PLL can accept input frequencies in the 8 MHz to 27 MHz range. To support lower frequencies (8 kHz to 8 MHz), the chip provides a digital PLL. It can boost the input clock frequency by  $2^N$ , where  $N = 1$  to 10.

Figure 25 shows the clock generation block diagram.

For the digital PLL, the source clock is selected by the DPLL\_REF\_SEL bits (Register 0x08), and the frequency relationship between the DPLL input and the output clock is defined by the DPLL\_NDIV bit.

The frequency relationship between the APLL input and output is

$$f_{PLL} = f_{IN} \times (R + (N/M)) / X$$

where  $R$ ,  $N$ ,  $M$ , and  $X$  are defined by the corresponding PLL registers (Register 0x09 to Register 0x0D).

### DIGITAL INPUT SERIAL AUDIO INTERFACE

The [SSM2529](#) includes a standard serial audio interface that is slave only. The interface is capable of receiving I<sup>2</sup>S, left justified, right justified, PCM/TDM, or PDM input formats. The number of data bits must be set when in right-justified mode only.

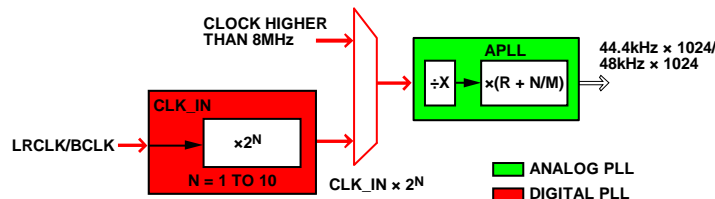


Figure 25. Clock Generation Block Diagram

**PDM MODE SETUP AND CONTROL**

If the ADDR pin is tied to DVDD while in standalone mode, or the PDM\_MODE bit (Register 0x01, Bit 7) is set to 1 while in I<sup>2</sup>C mode, the SSM2529 operates in PDM mode. In PDM mode, the SDATA pin receives the 1-bit PDM input to the DAC, and the BCLK pin provides the system clock for registering the input data. The PDM data input is registered directly on each clock edge.

The left or right data can be registered on either the rising or falling BCLK edge in both standalone mode or in I<sup>2</sup>C mode by setting the BCLK\_EDGE bit (Register 0x03, Bit 0).

When the part is in standalone mode and the PDM interface is selected, pull the MCLK pin to logic level low to register the left channel data (L data) on the rising BCLK edge, and the right channel data (R data) on the falling BCLK edge. When the MCLK pin is connected to logic high, the R data is registered on the rising BCLK edge, and the L data is registered on the falling BCLK edge.

When this part is in I<sup>2</sup>C PDM mode, if BCLK\_EDGE = 0, the L data is registered on the rising BCLK edge and the R data is registered on the falling BCLK edge. If BCLK\_EDGE = 1, the L data is registered on the falling BCLK edge, and the R data is registered on the rising BCLK edge.

**Table 9. PDM Timing Parameters**

Parameter	Limit		Unit	Description
	T <sub>MIN</sub>	T <sub>MAX</sub>		
t <sub>FALL</sub>		10	ns	Clock fall time
t <sub>RISE</sub>		10	ns	Clock rise time
t <sub>SETUP</sub>	10		ns	Data setup time
t <sub>HOLD</sub>	7		ns	Data hold time

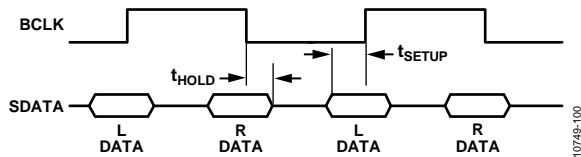


Figure 26. PDM Input Format

**HIGH-PASS FILTER**

The audio processing block contains a configurable first-order, high-pass filter. When the high-pass filter is enabled, the dc values are continuously calculated and subtracted from the input signal. By setting HPFOR (Register 0x15, Bit 1), the last calculated dc value is stored. When the high-pass filter is disabled, the stored value is still subtracted from the input signal until the HPFOR is cleared to 0.

The high-pass filter can work in audio mode or application mode, as configured by the HPF\_CTRL register. In audio mode, the high-pass filter's 3 dB cutoff frequency is 3.7 Hz when the

sampling rate is 48 kHz. In application mode, the 3 dB cutoff frequency varies from 50 Hz to 750 Hz, which is selected by using the HPFCUT bits (Register 0x15, Bits[5:2]).

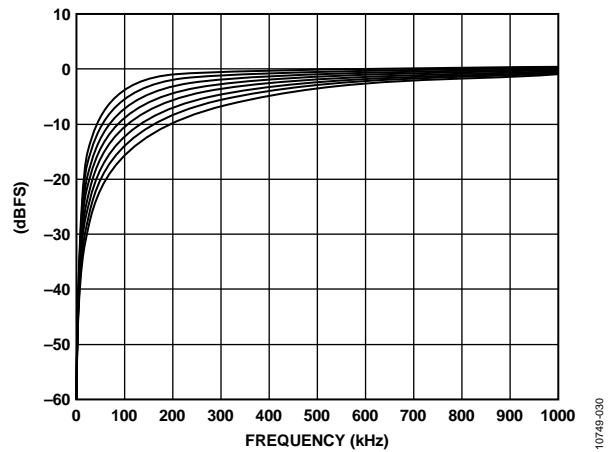


Figure 27. High-Pass Filter Response from HPFCUT Adjustment

**Table 10. HPF\_CTRL Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		HPFCUT			HPFOR		HPFEN

**Table 11. Bit Description of HPF\_CTRL Register**

Bit Name	Description	Settings
HPFCUT[3:0]	HPF cut-off frequency selection	See the Table 66
HPFOR	HPF mode selection	0: audio mode (cutoff frequency is 3.7 Hz) 1: application mode (cutoff frequency selectable)
HPFEN	HPF enable	0: disable 1: enable

**FULLY PROGRAMMABLE SEVEN-BAND EQUALIZER**

The programmable seven-band equalizer comprises five biquad filters (Band 1 to Band 5) and two first-order IIR filters (Band 6 and Band 7). Figure 28 shows the system block diagram.

All filter coefficients are programmable via the corresponding registers. When not all five midfrequency bands are needed, the filter bank can be configured as other filters, such as de-emphasis and notch filters.

To operate as a seven-band equalizer, the two first-order IIR filters are usually configured as one low-pass shelving filter and one high-pass shelving filter, and the biquad filters are configured as peak filters. By using the coefficient registers, the cutoff frequencies and peak gains of the shelving filters and the center frequencies and bandwidths of the peak filters are programmable. For frequency bands lower than 200 Hz, the low-pass shelving filter is suggested.

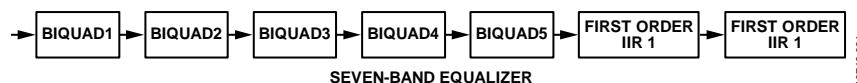


Figure 28. System Block Diagram

The common biquad filter transfer function is

$$H(z) = \frac{P0 + P1 \times Z^{-1} + P2 \times Z^{-2}}{1 - D1 \times Z^{-1} - D2 \times Z^{-2}}$$

The first-order IIR filter transfer function is

$$H(z) = \frac{P0 + P1 \times Z^{-1}}{1 - D1 \times Z^{-1}}$$

In normal mode, the supported coefficients range from  $-4$  to approximately  $+4$ . For equalizer mode, this range means that the cutoff and center frequencies can vary from 40 Hz to 12 kHz when the input sampling rate is 48 kHz, and the peak gain varies from  $-18$  dB to  $+18$  dB.

The EQ\_FORMAT bit in Register 0x54 defines the coefficient format. The default value is 0, and the corresponding format is Q3.13. Setting this bit to 1 achieves a larger coefficient range (from  $-8$  to approximately  $+8$ ), which enables a larger gain boost or decreases the range.

Online coefficient update is supported. If the filter bank coefficients are updated when the EQ is operating, set the EQ\_UPD bit after the coefficient is written. The coefficient update procedure requires approximately 0.05 ms to complete. The read only bit, EQ\_UPDING, in the EQ\_CTRL1 register represents the coefficient update status. If the system clock is removed during this period, the update procedure cannot be finished, and the EQ\_UPD\_CLR bit must be set to cancel this update.

The filter bank can be disabled, and all seven bands can be bypassed separately to save power. The corresponding bits are EQEN and EQBP1 to EQBP7 in Register 0x55.

**Table 12. EQ Coefficients Registers**

Register Address	Register Name	Description
0x16	EQ1_COEF0_HI[15:8]	EQ Band 1, Coefficient 0 MSB
0x17	EQ1_COEF0_LO[7:0]	EQ Band 1, Coefficient 0 LSB
0x18	EQ1_COEF1_HI[15:8]	EQ Band 1, Coefficient 1 MSB
0x19	EQ1_COEF1_LO[7:0]	EQ Band 1, Coefficient 1 LSB
0x1A	EQ1_COEF2_HI[15:8]	EQ Band 1, Coefficient 2 MSB
0x1B	EQ1_COEF2_LO[7:0]	EQ Band 1, Coefficient 2 LSB
...	...	...
0x52	EQ7_COEF2_HI[15:8]	EQ Band 7, Coefficient 2 MSB
0x53	EQ7_COEF2_LO[7:0]	EQ Band 7, Coefficient 2 LSB

**Table 13. EQ\_CTRL1 Register**

D7	D6	D5	D4	D3	D2	D1	D0
EQ_RESERVED				EQ_UPDING	EQ_UPD_CLR	EQ_FORMAT	EQ_UPD

**Table 14. Bit Description of EQ\_CTRL1 Register**

Bit Name	Description	Settings
EQ_RESERVED	Reserved	
EQ_UPDING	EQ coefficient updating flag	0: EQ coefficients updating 1: None
EQ_UPD_CLR	EQ coefficient update clear	0: normal operation 1: interrupt coefficient update
EQ_FORMAT	EQ coefficient format selection	0: normal 1: large gain
EQ_UPD	EQ coefficient registers update flag	1: update 0: none

**Table 15. EQ\_CTRL2 Register**

D7	D6	D5	D4	D3	D2	D1	D0
EQEN	EQBP7	EQBP6	EQBP5	EQBP4	EQBP3	EQBP2	EQBP1

**Table 16. Bit Description of EQ\_CTRL2 Register**

Bit Name	Description	Settings
EQEN	EQ enabled	0: EQ disabled 1: EQ enabled
EQBP7	EQ Band 7 bypass when EQ enabled	0: no bypass 1: bypass EQ Band 7
EQBP6	EQ Band 6 bypass when EQ enabled	0: no bypass 1: bypass EQ Band 6
EQBP5	EQ Band 5 bypass when EQ enabled	0: no bypass 1: bypass EQ Band 5
EQBP4	EQ Band 4 bypass when EQ enabled	0: no bypass 1: bypass EQ Band 4
EQBP3	EQ Band 3 bypass when EQ enabled	0: no bypass 1: bypass EQ Band 3
EQBP2	EQ Band 2 bypass when EQ enabled	0: no bypass 1: bypass EQ Band 2
EQBP1	EQ Band 1 bypass when EQ enabled	0: no bypass 1: bypass EQ Band 1

The typical characteristic of each EQ band is shown in Figure 29 to Figure 36.

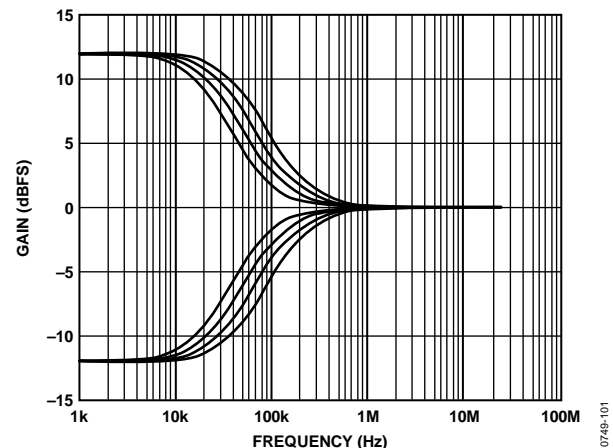


Figure 29. Low-Pass Shelving Filter Frequency Response Across Bandwidth Settings



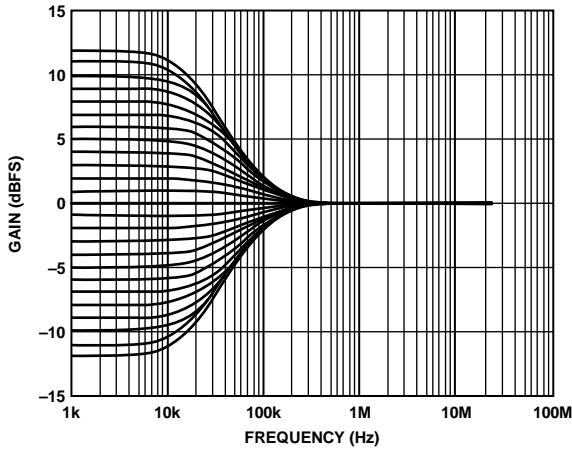


Figure 30. Low-Pass Shelving Filter Frequency Response Across Gain Settings

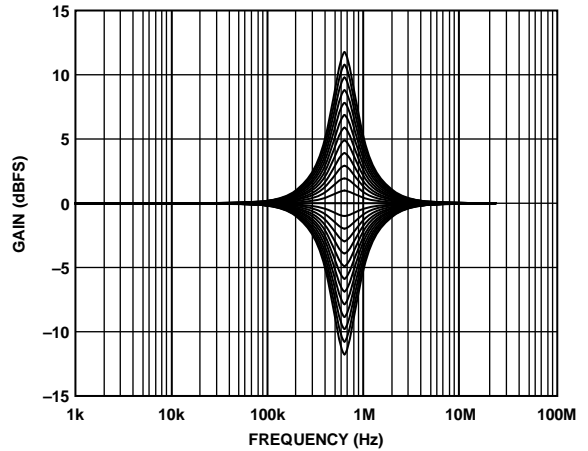


Figure 33. Peak Filter Frequency Response Across Gain Settings

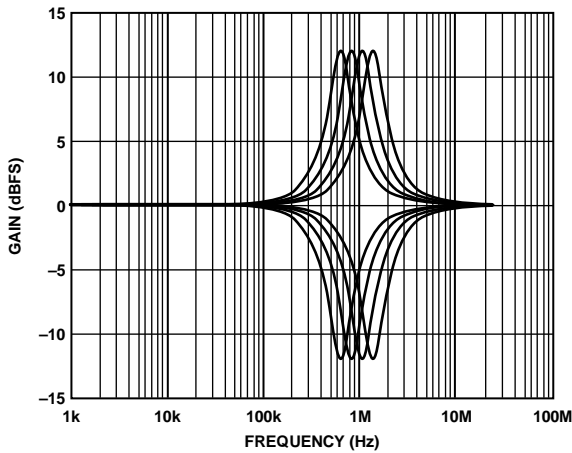


Figure 31. Peak Filter Frequency Response with Different Center Frequencies

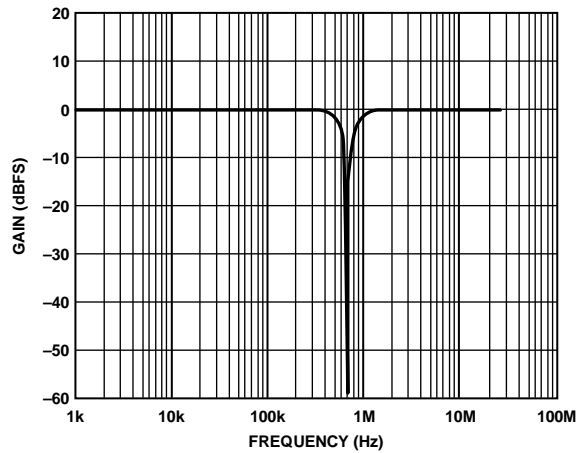


Figure 34. Notch Filter Response ( $A_0 = +1982$  to  $+2048$ ,  $A_1 = -2041$  to  $+2048$ , Bandwidth = 251 Hz, Center Frequency = 631 Hz)

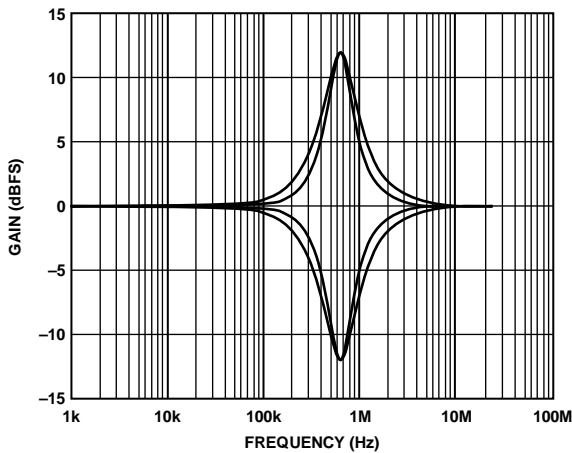


Figure 32. Peak Filter Frequency Response Across Bandwidth Settings

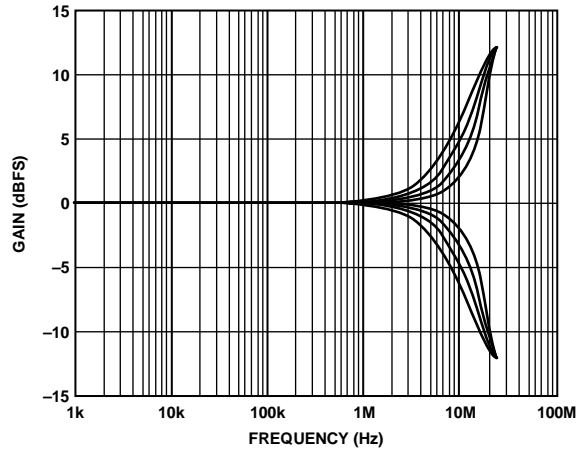


Figure 35. Treble Band Frequency Response Across Bandwidth Settings

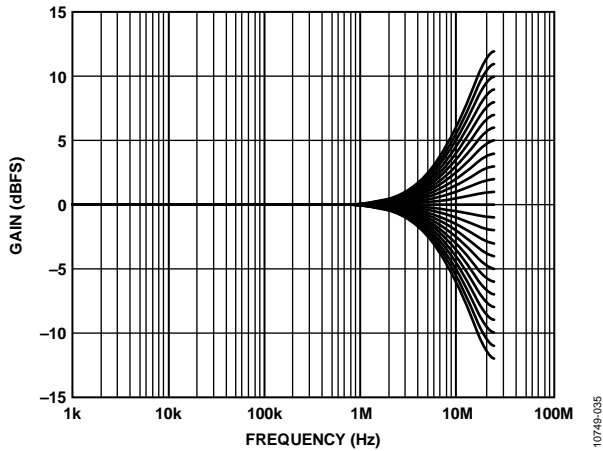


Figure 36. Treble Band Frequency Response Across Gain Settings

## DYNAMIC RANGE CONTROL

The dynamic range control function is used to alter (usually reduce) the dynamic range of the audio signal so that a loud signal can be heard without disturbing the hearing perception, and a weak signal can still be heard. In addition, very large signals and very weak signals are usually treated with different methods to ensure the overall sound quality. The DRC functions include the following:

- Limiter
- Compressor
- Expander
- Noise Gate

The dynamic range is not altered when the signal level is in the middle. These functions can be enabled or disabled individually.

### Limiter

If the input audio samples are large, the output is clipped at a predefined level so that the speakers are not overdriven.

If the ADC power tracking function is enabled, the maximum output level is set automatically to correspond to the speaker SPKVDD power.

### Compressor

The compressor is used to reduce the signal dynamic range when the input level is large and within predefined boundaries. This helps reduce the loudness when the signal level is high.

### Expander

The expander is used to increase the signal dynamic range when the input signal level is small and within predefined upper and lower boundaries. This helps increase the loudness when the signal is weak.

### Noise Gate

When the signal level is lower than a predefined threshold level, it is treated as noise. Under this condition, the output is set to zero.

The overall DRC characteristics are illustrated in Figure 37. A number of threshold levels (referred to the input) are used, which are defined as the limiter threshold (LT), compressor threshold (CT), expander threshold (ET), noise gate threshold (NT), maximum output signal amplitude (SMAX), and minimum output signal amplitude (SMIN). The corresponding bits are DRC\_LT, DRC\_CT, DRC\_ET, DRC\_NT, DRC\_SMAX, and DRC\_SMIN and can be found in Register 0x59 to Register 0x5D.

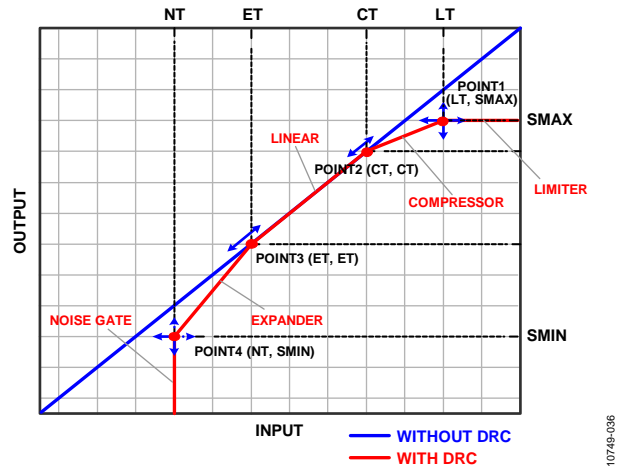


Figure 37. DRC Input/Output Relationship

## DRC MODE CONTROL

The DRC\_EN bits in Register 0x60 control the DRC. The noise gating function can be disabled by setting the NG\_EN bit in Register 0x60.

Table 17. DRC Mode Control Register

D7	D6	D5	D4	D3	D2	D1	D0
VBAT_EN	LIM_SRC	LIM_EN	COMP_EN	EXP_EN	NG_EN	DRC_EN	

Table 18. Bit Description of DRC Mode Control Register

Bit Name	Description	Settings
VBAT_EN	VBAT tracking enabled	0: disable 1: enable
LIM_SRC	Limiter source selection	0: peak 1: RMS
LIM_EN	Limiter enabled	0: disable 1: enable
COMP_EN	Compressor disabled	0: disable 1: enable
EXP_EN	Expander enabled	0: disable 1: enable
NG_EN	Noise gating enabled	0: disable 1: enable
DRC_EN	DRC enabled	0: disable 1: enable

Figure 38 shows a high level system block diagram of the DRC function.

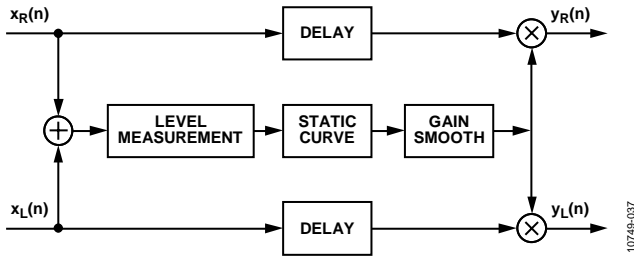


Figure 38. DRC Block Diagram

**Level Measurement**

The DRC level measurement includes the peak and rms value measurements. The parameters that affect the peak measurement are attack time and release time (AT and RT). The parameter that affects the rms measurement is average time ( $T_{AV}$ ). The attack time can vary from 0 ms to 1.536 sec; the release time and average time can vary from 0 ms to 24.576 sec. The corresponding bits are PEAK\_ATT, PEAK\_REL, and DRCLTAV and can be found in Register 0x56 and Register 0x57.

Table 19. DRC\_CTRL1 Register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				DRCLTAV[3:0]			

Table 20. Bit Description of DRC\_CTRL1 Register

Bit Name	Description	Settings
DRCLTAV[3:0]	DRC rms detector average time	0000: 0 ms 0001: 0.075 ms 0011: 0.30 ms (default) 1111: 24.576 sec

Table 21. DRC\_CTRL2 Register

D7	D6	D5	D4	D3	D2	D1	D0
PEAK_ATT[3:0]				PEAK_REL[3:0]			

Table 22. Bit Description of DRC\_CTRL2 Register

Bit Name	Description	Settings
PEAK_ATT[3:0]	DRC peak detector attack time	0000: 0 ms 0001: 0.09 ms 0010: 0.19 ms 0011: 0.37 ms 0100: 0.75 ms 0101: 1.5 ms 0110: 3.0 ms 0111: 6.0 ms ... 1111: 1.536 sec
PEAK_REL[3:0]	DRC peak detector decay time	0000: 0 ms 0001: 1.5 ms 0010: 3 ms 0011: 6 ms 0100: 12 ms ... 1111: 24.576 sec

**Static Curve**

The static curve is the DRC core function used to define the targeted input and output relationship. The role for the DRC block is to find the appropriate gain values with the various signal levels. To change the dynamic range of the original audio signal, the gain values vary with the input signal level.

An example of such a static curve is given in Figure 39, which shows the input and output signal levels. The blue line shows a linear relationship where the output dynamic range is identical to the input dynamic range. The red line shows a different output dynamic range from the input. Furthermore, this curve indicates that the signal dynamic range is larger when the input signal is low.

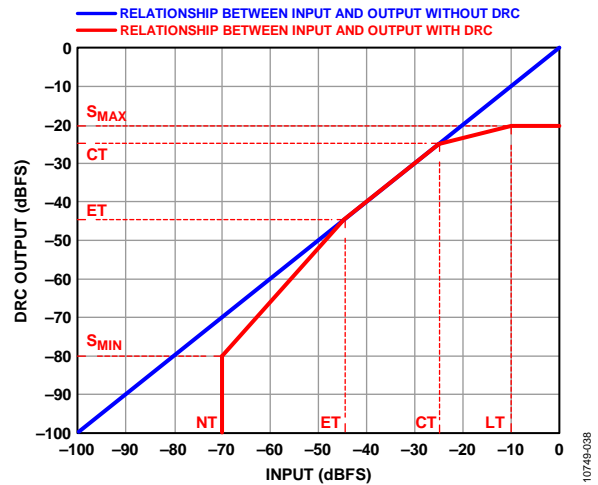


Figure 39. DRC Output vs. Input

Figure 40 shows the gain values at various input signal levels.

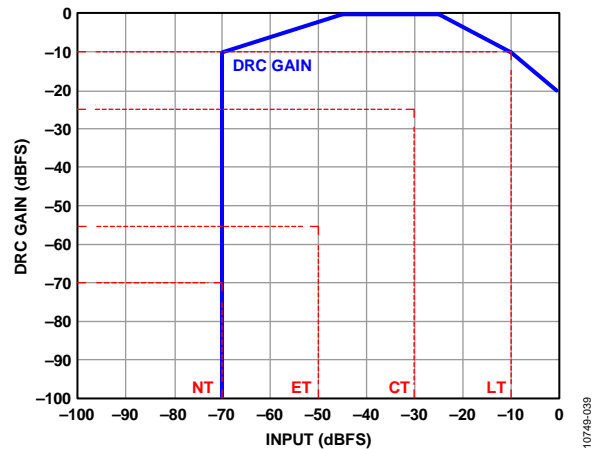


Figure 40. DRC Gain vs. Input

**DRC Static Curve Function**

A number of threshold levels (referred to the input) are used in Figure 39 and Figure 40; these levels are defined as the limiter threshold (LT), compressor threshold (CT), expander threshold (ET), noise gate threshold (NT), maximum output signal amplitude (SMAX), and minimum output signal amplitude (SMIN). The corresponding bits, DRC\_LT, DRC\_CT, DRC\_ET, DRC\_NT, DRC\_SMAX, DRC\_SMIN, can be found in Register 0x59 to Register 0x5D.

Table 23. DRC\_CURVE1 Register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		DRC_LT[6:0]					

Table 24. Bit Description of DRC\_CURVE1 Register

Bit Name	Description	Settings
DRC_LT[6:0]	DRC limiter threshold	0000000: +6 dB 0000001: +5.5 dB –0.5 dB step to 1010000: –35 dB

Table 25. DRC\_CURVE2 Register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		DRC_CT[6:0]					

Table 26. Bit Description of DRC\_CURVE2 Register

Bit Name	Description	Settings
DRC_CT[6:0]	DRC compressor threshold	0000000: +6 dB 0000001: +5.5 dB –0.5 dB step to 1010000: –35 dB

Table 27. DRC\_CURVE3 Register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		DRC_SMAX[6:0]					

Table 28. Bit Description of DRC\_CURVE3 Register

Bit Name	Description	Settings
DRC_SMAX[6:0]	DRC maximum output signal amplitude	0000000: +6 dB 0000001: +5.5 dB –0.5 dB step to 1010000: –35 dB

Table 29. DRC\_CURVE4 Register

D7	D6	D5	D4	D3	D2	D1	D0
DRC_NT[3:0]			DRC_ET[3:0]				

Table 30. Bit Description of DRC\_CURVE4 Register

Bit Name	Description	Settings
DRC_NT[3:0]	DRC noise gating threshold	0000: –51 dB 0001: –54 dB –3 dB step to 1111: –96 dB
DRC_ET[3:0]	DRC expander threshold	0000: –36 dB 0001: –39 dB –3 dB step to 1111: –81 dB

Table 31. DRC\_CURVE5 Register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				DRC_SMIN[3:0]			

Table 32. Bit Description of DRC\_CURVE5 Register

Bit Name	Description	Settings
DRC_SMIN[3:0]	DRC minimum output signal level	0000: –51 dB  0001: –54 dB –3 dB step to 1111: –96 dB

**DRC Gain Smooth**

Before the gain calculated by the static curve function multiplies with the input signal, smooth it to ensure that it does not change rapidly for this can lead to noise.

The gain smooth is affected by its attack and decay time parameters. The attack time can vary from 0 ms to 1.536 sec, while the decay time can vary from 0 ms to 24.576 sec. The corresponding bits are DRC\_ATT and DRC\_DEC and can be found in Register 0x58.

Table 33. DRC\_CTRL3 Register

D7	D6	D5	D4	D3	D2	D1	D0
DRC_ATT[3:0]				DRC_DEC[3:0]			

Table 34. Bit Description of DRC\_CTRL3 Register

Bit Name	Description	Settings
DRC_ATT[3:0]	DRC attack time	0000: 0 ms 0001: 0.1 ms 0010: 0.19 ms 0011: 0.37 ms 0100: 0.75 ms 0101: 1.5 ms 0110: 3 ms 0111: 6 ms ... 1111: 1.536 sec
DRC_DEC[3:0]	DRC decay time	0000: 0 ms 0001: 1.5 ms 0010: 3 ms 0011: 6 ms 0100: 12 ms ... 1111: 24.576 sec

**DRC Hold Time**

Two types of hold time are used in the DRC. One is used in normal mode to prevent the calculated gain from increasing too quickly, and the other is used during DRC transiting from expander mode to noise gating mode to prevent the DRC from entering noise gating too quickly. The DRCHTNOR and DRCHTNG bits in Register 0x5E set which type is used.

**Table 35. DRC\_HOLD\_TIME Register**

D7	D6	D5	D4	D3	D2	D1	D0
DRCHTNG[3:0]				DRCHTNOR[3:0]			

**Table 36. Bit Description of DRC\_HOLD\_TIME Register**

Bit Name	Description	Settings
DRCHTNG[3:0]	DRC hold time for noise gating	0000: 0 ms 0001: 0.67 ms xxxx: double time 0111: 42.67 ms (default) 1111: 43.7 sec
DRCHTNOR[3:0]	DRC hold time for normal operation	0000: 0 ms 0001: 0.67 ms 0010: 1.33 ms 0011: 2.67 ms 0100: 5.33 ms .... 1111: 43.7 sec

**GAIN RIPPLE REMOVE**

Due to the swing of the peak/rms value detected by the level measurement, the gain to apply to the input signal has a little ripple, which leads to the modulation of the output signal. The ripple remove function suppresses this effect. The ripple threshold is defined by the DRCRRH bit in Register 0x5F.

**Table 37. DRC\_RIPPLE\_CTRL Register**

D7	D6	D5	D4	D3	D2	D1	D0
Reserved						DRCRRH[1:0]	

**Table 38. Bit Description of DRC\_RIPPLE\_CTRL Register**

Bit Name	Description	Settings
DRCRRH[1:0]	DRC ripple remove threshold	00: 0 dB 01: 0.28 dB 10: 0.47 dB 11: 0.75 dB (default)

**SPEAKER PROTECTION**

The IC includes a speaker temperature prediction module to protect the loudspeaker. Loudspeakers can be damaged when the voice coil overheats due to operation higher than the rated power. Typically, the thermal time constants of the loudspeakers are long, approximately 1 sec for voice coil and 60 sec for core. They can handle momentary power spikes without overheating; however, they cannot handle sustained high power. The speaker protection method used in the IC can reduce the volume when the temperature of the loudspeaker exceeds the temperature threshold set by the user while preserving the maximum power

of the loudspeaker. The temperature prediction method is based on the general thermal model of the loudspeaker.

In this thermal model, R1, R2, C1, and C2 are temperature coefficients derived by measuring loudspeaker characteristics. They are set by the I<sup>2</sup>C control registers, Register 0x84 to Register 0x8B (SP\_CF1\_H, SP\_CF1\_L, SP\_CF2\_H, SP\_CF2\_L, SP\_CF3\_H, SP\_CF3\_L, SP\_CF4\_H and SP\_CF4\_L).

Other critical parameters needed include ambient temperature, dc resistance of the loudspeaker, and temperature coefficient of the voice coil material. These parameters are set by Register 0x81 to Register 0x83 (TEMP\_AMBIENT, SPKR\_DCR, and SPKR\_TC).

After running the thermal model by setting the speaker protection enable bit (SP\_EN, Register 0x80), the speaker voice coil temperature status and speaker magnet temperature status can be obtained by an I<sup>2</sup>C reading of the SPKR\_TEMP register (Register 0x8C) and the SPKR\_TEMP\_MAG register (Register 0x8D). The user sets the voice coil temperature threshold (maximum speaker voice coil temperature before gain reduction occurs) by using the MAX\_SPKR\_TEMP register (Register 0x8E). If this threshold is crossed, the output volume is reduced according to the speed set by the SP\_AR bits (speaker protection gain reduction attack rate, Register 0x8F, Bits[7:4]) and the SP\_RR bits (speaker protection gain reduction release rate, Register 0x8F, Bits[3:0]).

**POWER SUPPLIES**

The SSM2529 has two internal power supplies that must be provided: SPKVDD and DVDD. The SPKVDD supply powers to the full bridge power stage of the MOSFET and its associated drive, control, and protection circuitry. SPKVDD can operate from 2.5 V to 5.5 V and must be present to obtain audio output. Lowering the SPKVDD supply results in lower output power and correspondingly lower power consumption, and it does not affect audio performance.

DVDD provides power to the digital logic and analog components. DVDD can operate from 1.08 V to 1.98 V, and it must be provided to write to the I<sup>2</sup>C or to obtain audio output. Lowering the supply voltage results in lower power consumption; however, it also results in lower audio performance.

**POWER CONTROL**

The SSM2529 includes various programmable power-down modes that are contained in the first I<sup>2</sup>C register (Register 0x00), power/reset control. By default, the IC is set in software power-down, which is the I<sup>2</sup>C programmable master power-down. Only I<sup>2</sup>C functionality operates when in software power-down mode.

The SSM2529 also contains a smart power-down feature that, when enabled, looks at the incoming digital audio. In addition, if the audio is zero for 1024 consecutive samples, regardless of sample rate, it puts the IC in a smart power-down state. In this state, all circuitry, except the I<sup>2</sup>S and I<sup>2</sup>C ports, are placed in a low power state. After a single nonzero input is received, the SSM2529 leaves this state and resumes normal operation.

## POWER-ON RESET/VOLTAGE SUPERVISOR

The [SSM2529](#) includes an internal power-on reset and voltage supervisor circuit. This circuit provides an internal reset to all circuitry during initial power-up. It also monitors the power supplies to the IC, and it mutes the outputs and issues a reset when the voltages are lower than the minimum operating range. This ensures that no damage due to low voltage operation occurs and that no pops can occur under nearly any power removal conditions.

## STANDALONE MODE

When the SA\_MODE pin is pulled high, the [SSM2529](#) can operate without any I<sup>2</sup>C control. In this mode, the automatic sample rate detection and smart power-down are always enabled. Volume Control A and Volume Control B can be controlled via the SCL and SDA pins.

In standalone mode, the DRC function is disabled. The EQ and HPF are also disabled. When ADDR = 1, the input interface is PDM. Otherwise, I<sup>2</sup>S and TDM serial interface formats can be selected via MCLK. In standalone mode, the working clock is generated by the internal PLL.

**Table 39. Standalone Mode Pin Configuration**

Conventional Operation Pin	SA_MODE = 1
SCL	Volume Control A
SDA	Volume Control B
STDBN	0: shutdown/mute 1: normal operation
ADDR	1: PDM 0: I <sup>2</sup> S/TDM
BCLK	0: 16 BCLK cycles provided by PLL 1: 32 BCLK cycles provided by PLL Clock: 32 BCLK cycles provided off chip
MCLK	0: I <sup>2</sup> S (ADDR = 0) or PDM L channel (ADDR = 1) 1: TDM (ADDR = 0) or PDM R channel (ADDR = 1)

## I<sup>2</sup>C PORT

The [SSM2529](#) supports a 2-wire serial (I<sup>2</sup>C-compatible) micro-processor bus driving multiple peripherals. Two pins, serial data (SDA) and serial clock (SCL), carry information between the [SSM2529](#) and the system I<sup>2</sup>C master controller. The [SSM2529](#) is always a slave on the bus, meaning that it cannot initiate a data transfer. Each slave device is recognized by a unique address. The address byte format is shown in Table 40. The address resides in the first seven bits of the I<sup>2</sup>C write. The LSB of this byte either sets a read or write operation. Logic Level 1 corresponds to a read operation, and Logic Level 0 corresponds to a write operation. The full byte addresses are shown in Figure 41, where the subaddresses are automatically incremented at word boundaries, and can be used for writing large amounts of data to contiguous memory locations. This increment happens automatically after a single-word write unless a stop condition is encountered. A data transfer is always terminated by a stop condition.

Both SDA and SCL must have a 2.2 kΩ pull-up resistor on the lines connected to them. The voltage on these signal lines must not be more than 3.6 V.

**Table 40. I<sup>2</sup>C Address Byte Format**

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	1	1	0	1	0	0	R/W

## Addressing

Initially, each device on the I<sup>2</sup>C bus is in an idle state, monitoring the SDA and SCL lines for a start condition and the proper address. The I<sup>2</sup>C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA, while SCL remains high. This indicates that an address/data stream follows. All devices on the bus respond to the start condition and shift the next eight bits (the 7-bit address plus the R/W bit) MSB first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. The device address for the [SSM2529](#) is 0x34. The ninth bit is known as the acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition.

The R/W bit determines the direction of the data. A Logic 0 on the LSB of the first byte means that the master writes information to the peripheral, whereas a Logic 1 means that the master reads information from the peripheral after writing the subaddress and repeating the start address. A data transfer takes place until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. The timing for the I<sup>2</sup>C port is shown in Figure 3.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, the [SSM2529](#) immediately jumps to the idle condition. During an SCL high period, issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued, the [SSM2529](#) does not issue an acknowledge and returns to the idle condition. If the highest subaddress is exceeded while in auto-increment mode, one of two actions is taken. In read mode, the [SSM2529](#) outputs the highest subaddress register contents until the master device issues a no acknowledge, indicating the end of the read. When the SDA line is not pulled low on the ninth clock pulse of SCL, a no acknowledge occurs. If the highest subaddress location is reached while in write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the [SSM2529](#), and the part returns to the idle condition.

**I<sup>2</sup>C Read and Write Operations**

Table 42 shows the timing of a single-word write operation. Every ninth clock, the SSM2529 issues an acknowledge by pulling SDA low.

Table 43 shows the timing of a burst mode write sequence as an example where the target destination registers are two bytes. The SSM2529 knows to increment its subaddress register every byte because the requested subaddress corresponds to a register or memory area with a byte word length.

The timing of a single-word read operation is shown in Table 44. Note that the first R/W bit is 0, indicating a write operation. This is because the subaddress still needs to be written to set up the internal address. After the SSM2529 acknowledges the receipt of the subaddress, the master must issue a repeated start command

followed by the chip address byte with the R/W bit set to 1 (read). This causes the SSM2529 SDA to reverse and begin driving data back to the master. The master then responds every ninth pulse with an acknowledge pulse to the SSM2529.

Table 42 to Table 45 use the abbreviations shown in Table 41.

**Table 41. Symbols for Table 42 to Table 45**

Symbol	Meaning
S	Start bit
P	Stop bit
A <sub>M</sub>	Acknowledge by master
A <sub>S</sub>	Acknowledge by slave

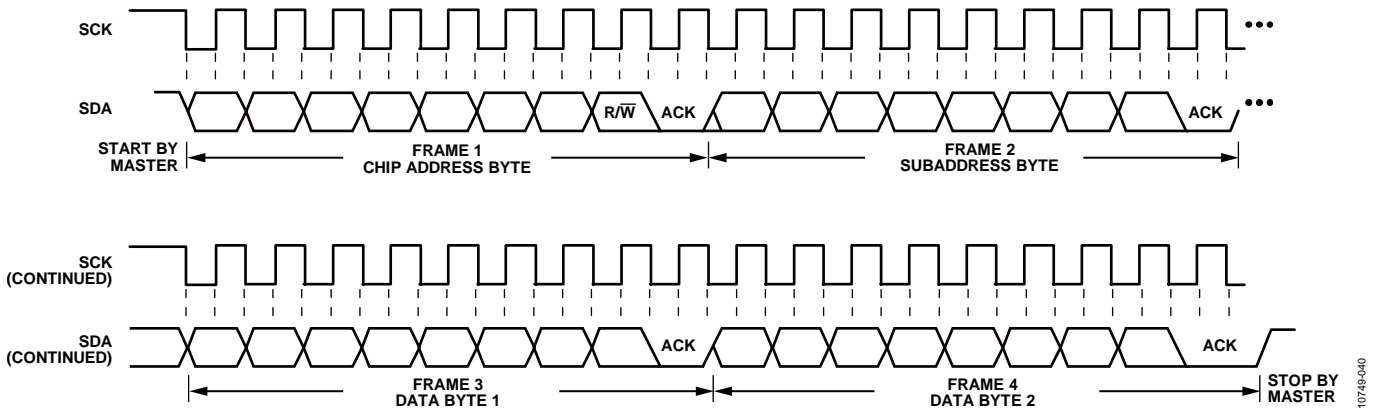


Figure 41. I<sup>2</sup>C Read and Write Timing

**Table 42. Single-Word I<sup>2</sup>C Write Format**

S	IC Address (7 Bits)	R/W = 0	A <sub>S</sub>	Subaddress (8 bits)	A <sub>S</sub>	Data Byte 1 (8 Bits)	P
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**Table 43. Burst Mode I<sup>2</sup>C Write Format**

S	Chip address, R/W = 0	A <sub>S</sub>	Subaddress	A <sub>S</sub>	Data-Word 1	A <sub>S</sub>	Data-Word 2	A <sub>S</sub>	...	P
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**Table 44. Single-Word I<sup>2</sup>C Read Format**

S	Chip address, R/W = 0	A <sub>S</sub>	Subaddress	A <sub>S</sub>	S	Chip address, R/W = 1	A <sub>S</sub>	Data Byte 1	A <sub>M</sub>	Data Byte N	P
---	-----------------------	----------------	------------	----------------	---	-----------------------	----------------	-------------	----------------	-------------	---

**Table 45. Burst Mode I<sup>2</sup>C Read Format**

S	Chip address, R/W = 0	A <sub>S</sub>	Subaddress	A <sub>S</sub>	S	Chip address, R/W = 1	A <sub>S</sub>	Data-Word 1	A <sub>M</sub>	...	P
---	-----------------------	----------------	------------	----------------	---	-----------------------	----------------	-------------	----------------	-----	---



## REGISTER SUMMARY

The SSM2529 contains eighteen 8-bit registers that can be accessed via the I<sup>2</sup>C port. See Table 46 for the control register mapping. The register settings are described in detail in Table 47 through Table 159.

**Table 46.**

Hex	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW	
00	PWR_CTRL	[7:0]	SYS_RST	APWDN_ANA	APWDN_EN	LP_MODE	MCS			SPWDN	0x23	RW	
01	SYS_CTRL	[7:0]	PDM_MODE	PDM_FS	PDB_ADC	BCLK_RATE	BCLK_GEN	EDGE		ASR	0x20	RW	
02	SAI_FMT1	[7:0]	SDATA_FMT		SAI			SR			0x02	RW	
03	SAI_FMT2	[7:0]	LPST	LR_SEL		LRCLK_MODE	LRCLK_POL	SAI_MSB	BCLK_TDMC	BCLK_EDGE	0x00	RW	
04	Channel mapping control	[7:0]	CH_SEL_R				CH_SEL_L				0x10	RW	
05	VOL_BF_FDSP	[7:0]	DIG_VOL									0x40	RW
06	VOL_AF_FDSP	[7:0]	PDP_VOL									0x40	RW
07	Volume and mute control	[7:0]	CLK_LOSS_DET	SR_AUTO			Reserved	PDP_VOL_FORCE	DIG_VOL_FORCE	ANA_GAIN	0x20	RW	
08	DPLL_CTRL	[7:0]	Reserved	DPLL_REF_SEL			DPLL_NDIV				0x00	RW	
09	APLL_CTRL1	[7:0]	M_HI									0x00	RW
0A	APLL_CTRL2	[7:0]	M_LO									0x00	RW
0B	APLL_CTRL3	[7:0]	N_HI									0x00	RW
0C	APLL_CTRL4	[7:0]	N_LO									0x00	RW
0D	APLL_CTRL5	[7:0]	Reserved	R				X		Type	0x00	RW	
0E	APLL_CTRL6	[7:0]	FSYS_DPLL		DPLL_BYPASS	APLL_BYPASS	DPLL_LOCK	APLL_LOCK	PLLEN	COREN	0x30	RW	
0F	FAULT_CTRL1	[7:0]	Reserved			PDB_LINE	PDB_ZC	CLK_LOSS	OC	OT	0x000	RW	
10	FAULT_CTRL2	[7:0]	Reserved	AR_TIME		MRCV	MAX_AR		ARCV		0x4C	RW	
14	DEEMP_CTRL	[7:0]	Reserved				DEEMP_FS		DEEMP_EN		0x00	RW	
15	HPF_CTRL	[7:0]	Reserved		HPFCUT				HPFOR	HPFEN	0x00	RW	
16	EQ1_COEF0_HI	[7:0]	EQ1_COEF0_HI									0x00	RW
17	EQ1_COEF0_LO	[7:0]	EQ1_COEF0_LO									0x00	RW
18	EQ1_COEF1_HI	[7:0]	EQ1_COEF1_HI									0x00	RW
19	EQ1_COEF1_LO	[7:0]	EQ1_COEF1_LO									0x00	RW
1A	EQ1_COEF2_HI	[7:0]	EQ1_COEF2_HI									0x00	RW
1B	EQ1_COEF2_LO	[7:0]	EQ1_COEF2_LO									0x00	RW
1C	EQ1_COEF3_HI	[7:0]	EQ1_COEF3_HI									0x00	RW
1D	EQ1_COEF3_LO	[7:0]	EQ1_COEF3_LO									0x00	RW
1E	EQ1_COEF4_HI	[7:0]	EQ1_COEF4_HI									0x00	RW
1F	EQ1_COEF4_LO	[7:0]	EQ1_COEF4_LO									0x00	RW
20	EQ2_COEF0_HI	[7:0]	EQ2_COEF0_HI									0x00	RW
21	EQ2_COEF0_LO	[7:0]	EQ2_COEF0_LO									0x00	RW
22	EQ2_COEF1_HI	[7:0]	EQ2_COEF1_HI									0x00	RW
23	EQ2_COEF1_LO	[7:0]	EQ2_COEF1_LO									0x00	RW
24	EQ2_COEF2_HI	[7:0]	EQ2_COEF2_HI									0x00	RW
25	EQ2_COEF2_LO	[7:0]	EQ2_COEF2_LO									0x00	RW
26	EQ2_COEF3_HI	[7:0]	EQ2_COEF3_HI									0x00	RW
27	EQ2_COEF3_LO	[7:0]	EQ2_COEF3_LO									0x00	RW
28	EQ2_COEF4_HI	[7:0]	EQ2_COEF4_HI									0x00	RW
29	EQ2_COEF4_LO	[7:0]	EQ2_COEF4_LO									0x00	RW
2A	EQ3_COEF0_HI	[7:0]	EQ3_COEF0_HI									0x00	RW
2B	EQ3_COEF0_LO	[7:0]	EQ3_COEF0_LO									0x00	RW
2C	EQ3_COEF1_HI	[7:0]	EQ3_COEF1_HI									0x00	RW
2D	EQ3_COEF1_LO	[7:0]	EQ3_COEF1_LO									0x00	RW
2E	EQ3_COEF2_HI	[7:0]	EQ3_COEF2_HI									0x00	RW
2F	EQ3_COEF2_LO	[7:0]	EQ3_COEF2_LO									0x00	RW
30	EQ3_COEF3_HI	[7:0]	EQ3_COEF3_HI									0x00	RW
31	EQ3_COEF3_LO	[7:0]	EQ3_COEF3_LO									0x00	RW
32	EQ3_COEF4_HI	[7:0]	EQ3_COEF4_HI									0x00	RW
33	EQ3_COEF4_LO	[7:0]	EQ3_COEF4_LO									0x00	RW
34	EQ4_COEF0_HI	[7:0]	EQ4_COEF0_HI									0x00	RW
35	EQ4_COEF0_LO	[7:0]	EQ4_COEF0_LO									0x00	RW
36	EQ4_COEF1_HI	[7:0]	EQ4_COEF1_HI									0x00	RW



Hex	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW	
37	EQ4_COEF1_LO	[7:0]	EQ4_COEF1_LO								0x00	RW	
38	EQ4_COEF2_HI	[7:0]	EQ4_COEF2_HI								0x00	RW	
39	EQ4_COEF2_LO	[7:0]	EQ4_COEF2_LO								0x00	RW	
3A	EQ4_COEF3_HI	[7:0]	EQ4_COEF3_HI								0x00	RW	
3B	EQ4_COEF3_LO	[7:0]	EQ4_COEF3_LO								0x00	RW	
3C	EQ4_COEF4_HI	[7:0]	EQ4_COEF4_HI								0x00	RW	
3D	EQ4_COEF4_LO	[7:0]	EQ4_COEF4_LO								0x00	RW	
3E	EQ5_COEF0_HI	[7:0]	EQ5_COEF0_HI								0x00	RW	
3F	EQ5_COEF0_LO	[7:0]	EQ5_COEF0_LO								0x00	RW	
40	EQ5_COEF1_HI	[7:0]	EQ5_COEF1_HI								0x00	RW	
41	EQ5_COEF1_LO	[7:0]	EQ5_COEF1_LO								0x00	RW	
42	EQ5_COEF2_HI	[7:0]	EQ5_COEF2_HI								0x00	RW	
43	EQ5_COEF2_LO	[7:0]	EQ5_COEF2_LO								0x00	RW	
44	EQ5_COEF3_HI	[7:0]	EQ5_COEF3_HI								0x00	RW	
45	EQ5_COEF3_LO	[7:0]	EQ5_COEF3_LO								0x00	RW	
46	EQ5_COEF4_HI	[7:0]	EQ5_COEF4_HI								0x00	RW	
47	EQ5_COEF4_LO	[7:0]	EQ5_COEF4_LO								0x00	RW	
48	EQ6_COEF0_HI	[7:0]	EQ6_COEF0_HI								0x00	RW	
49	EQ6_COEF0_LO	[7:0]	EQ6_COEF0_LO								0x00	RW	
4A	EQ6_COEF1_HI	[7:0]	EQ6_COEF1_HI								0x00	RW	
4B	EQ6_COEF1_LO	[7:0]	EQ6_COEF1_LO								0x00	RW	
4C	EQ6_COEF2_HI	[7:0]	EQ6_COEF2_HI								0x00	RW	
4D	EQ6_COEF2_LO	[7:0]	EQ6_COEF2_LO								0x00	RW	
4E	EQ7_COEF0_HI	[7:0]	EQ7_COEF0_HI								0x00	RW	
4F	EQ7_COEF0_LO	[7:0]	EQ7_COEF0_LO								0x00	RW	
50	EQ7_COEF1_HI	[7:0]	EQ7_COEF1_HI								0x00	RW	
51	EQ7_COEF1_LO	[7:0]	EQ7_COEF1_LO								0x00	RW	
52	EQ7_COEF2_HI	[7:0]	EQ7_COEF2_HI								0x00	RW	
53	EQ7_COEF2_LO	[7:0]	EQ7_COEF2_LO								0x00	RW	
54	EQ_CTRL1	[7:0]	EQ_RESERVED				EQ_UPDING	EQ_UPD_CLR	EQ_FORMAT	EQ_UPD	0x00	RW	
55	EQ_CTRL2	[7:0]	EQEN	EQBP7	EQBP6	EQBP5	EQBP4	EQBP3	EQBP2	EQBP1	0x00	RW	
56	DRC_CTRL1	[7:0]	Reserved				DRCLELTAV				0x00	RW	
57	DRC_CTRL2	[7:0]	PEAK_ATT				PEAK_REL				0x00	RW	
58	DRC_CTRL3	[7:0]	DRC_ATT				DRC_DEC				0x00	RW	
59	DRC_CURVE1	[7:0]	Reserved	DRC_LT						0x00	RW		
5A	DRC_CURVE2	[7:0]	Reserved	DRC_CT						0x00	RW		
5B	DRC_CURVE3	[7:0]	Reserved	DRC_SMAX						0x00	RW		
5C	DRC_CURVE4	[7:0]	DRC_NT				DRC_ET				0x88	RW	
5D	DRC_CURVE5	[7:0]	RESERVED				DRC_SMIN				0x00	RW	
5E	DRC_HOLD_TIME	[7:0]	DRCHTNG				DRCHTNOR				0x00	RW	
5F	DRC_RIPPLE_CTRL	[7:0]	Reserved							DRCRRH	0x00	RW	
60	DRC mode control	[7:0]	VBAT_EN	LIM_SRC	LIM_EN	COMP_EN	EXP_EN	NG_EN	DRC_EN		0x3C	RW	
61	FDSP_EN	[7:0]	Reserved								FDSP_EN	0x00	RW
80	SPK_PROT_EN	[7:0]	Reserved								SP_EN	0x00	RW
81	TEMP_AMBIENT	[7:0]	TEMP_AMBIENT									0x19	RW
82	SPKR_DCR	[7:0]	SPKR_DCR									0x40	RW
83	SPKR_TC	[7:0]	SPKR_TC									0x08	RW
84	SP_CF1_H	[7:0]	SP_CF1_H									0x3F	RW
85	SP_CF1_L	[7:0]	SP_CF1_L									0x81	RW
86	SP_CF2_H	[7:0]	SP_CF2_H									0x00	RW
87	SP_CF2_L	[7:0]	SP_CF2_L									0x55	RW
88	SP_CF3_H	[7:0]	SP_CF3_H									0x01	RW
89	SP_CF3_L	[7:0]	SP_CF3_L									0x22	RW
8A	SP_CF4_H	[7:0]	SP_CF4_H									0x02	RW
8B	SP_CF4_L	[7:0]	SP_CF4_L									0x09	RW

Hex	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW	
8C	SPKR_TEMP	[7:0]	SPKR_TEMP									0x00	R
8D	SPKR_TEMP_MAG	[7:0]	SPKR_TEMP_MAG									0x00	R
8E	MAX_SPKR_TEMP	[7:0]	MAX_SPKR_TEMP									0x64	RW
8F	SPK_GAIN	[7:0]	SP_RR				SP_AR				0x44	RW	
FF	SOFT_RST	[7:0]	SOFT_RST									0x00	W

## REGISTER DETAILS

### SOFTWARE RESET AND MASTER SOFTWARE POWER-DOWN CONTROL (PWR\_CTRL) REGISTER

Table 47. Address: 0x00, Reset: 0x23, Name: PWR\_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
7	SYS_RST	0 1	Software reset Normal operation Software reset	0x0	RW
6	APWDN_ANA	0 1	Auto power-down mode Only digital Both analog and digital	0x0	RW
5	APWDN_EN	0 1	Auto power-down enable Auto power-down disabled Auto power-down enabled	0x1	RW
4	LP_MODE	0 1	Low power mode Normal operation Low power operation mode; DAC runs at half speed	0x0	RW
[3:1]	MCS	000 001 010 011 100 101 110 111	Master clock rate selection Refer to Table 48 Refer to Table 48 Refer to Table 48 Refer to Table 48 Refer to Table 48 Refer to Table 48 Not applicable Not applicable	0x1	RW
0	SPWDN	0 1	Master software power-down Normal operation Software master power-down	0x1	RW

Table 48 shows the MCS bit settings available with the possible input sample rates vs. the required master clock frequency, as well as the master clock to bit clock ratio. The b110 thru b111 settings are reserved and not available to the user.

### MCLK RATIO AND FREQUENCY

Table 48. MCS Bit Field Setting—MCLK Ratio and Frequency (N/A = Not Applicable)

Input Sample Frequency, $f_s$ (kHz)		Setting 0 b000	Setting 1 b001	Setting 2 b010	Setting 3 b011	Setting 4 b100	Setting 5 b101	Setting 6 b110 thru b111
8	Ratio MCLK	768 $f_s$ 6.144 MHz	1024 $f_s$ 8.192 MHz	1536 $f_s$ 12.288 MHz	2048 $f_s$ 16.384 MHz	3072 $f_s$ 24.576 MHz	4096 $f_s$ 32.768 MHz	Reserved
11.025	Ratio MCLK	N/A	512 $f_s$ 5.6448 MHz	1024 $f_s$ 11.2896 MHz	1536 $f_s$ 16.9344 MHz	2048 $f_s$ 22.5792 MHz	3072 $f_s$ 33.8688 MHz	Reserved
12	Ratio MCLK	N/A	512 $f_s$ 6.144 MHz	1024 $f_s$ 12.288 MHz	1536 $f_s$ 18.432 MHz	2048 $f_s$ 24.576 MHz	3072 $f_s$ 38.864 MHz	Reserved
16	Ratio MCLK	384 $f_s$ 6.144 MHz	512 $f_s$ 8.192 MHz	768 $f_s$ 12.288 MHz	1024 $f_s$ 16.384 MHz	1536 $f_s$ 24.576 MHz	2048 $f_s$ 32.768 MHz	Reserved
22.05	Ratio MCLK	N/A	256 $f_s$ 5.6448 MHz	512 $f_s$ 11.2896 MHz	768 $f_s$ 16.9344 MHz	1024 $f_s$ 22.5792 MHz	1536 $f_s$ 33.8688 MHz	Reserved
24	Ratio MCLK	N/A	256 $f_s$ 6.144 MHz	512 $f_s$ 12.288 MHz	768 $f_s$ 18.432 MHz	1024 $f_s$ 24.576 MHz	1536 $f_s$ 38.864 MHz	Reserved
32	Ratio MCLK	192 $f_s$ 6.144 MHz	256 $f_s$ 8.192 MHz	384 $f_s$ 12.288 MHz	512 $f_s$ 16.384 MHz	768 $f_s$ 24.576 MHz	1024 $f_s$ 32.768 MHz	Reserved
44.1	Ratio MCLK	N/A	128 $f_s$ 5.6448 MHz	256 $f_s$ 11.2896 MHz	384 $f_s$ 16.9344 MHz	512 $f_s$ 22.5792 MHz	768 $f_s$ 33.8688 MHz	Reserved

Input Sample Frequency, $f_s$ (kHz)		Setting 0 b000	Setting 1 b001	Setting 2 b010	Setting 3 b011	Setting 4 b100	Setting 5 b101	Setting 6 b110 thru b111
48	Ratio MCLK	N/A	128 $f_s$ 6.144 MHz	256 $f_s$ 12.288 MHz	384 $f_s$ 18.432 MHz	512 $f_s$ 24.576 MHz	768 $f_s$ 36.864 MHz	Reserved
88.2	Ratio MCLK	N/A	64 $f_s$ 5.6448 MHz	128 $f_s$ 11.2896 MHz	192 $f_s$ 16.9344 MHz	256 $f_s$ 22.5792 MHz	384 $f_s$ 33.8688 MHz	Reserved
96	Ratio MCLK	N/A	64 $f_s$ 6.144 MHz	128 $f_s$ 12.288 MHz	192 $f_s$ 18.432 MHz	256 $f_s$ 24.576 MHz	384 $f_s$ 36.864 MHz	Reserved

When using MCS = 0/64 $f_s$  mode, the chip automatically operates in low power mode.

### EDGE SPEED AND CLOCKING CONTROL (SYS\_CTRL) REGISTER

Table 49. Address: 0x01, Reset: 0x20, Name: SYS\_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
7	PDM_MODE	0 1	PDM input enable Disable PDM input Enable PDM input	0x0	RW
6	PDM_FS	0 1	PDM input sample rate About 3 MHz sample rate About 6 MHz sample rate	0x0	RW
5	PDB_ADC	0 1	ADC power down Power down Power on	0x1	RW
4	BCLK_RATE	0 1	BCLK cycles per channel frame 32 cycles per channel 16 cycles per channel	0x0	RW
3	BCLK_GEN	0 1	Generate BCLK internally Disabled Enabled	0x0	RW
[2:1]	EDGE	00 01	Edge rate control Normal operation Low EMI mode operation	0x0	RW
0	ASR	0 1	Auto sample rate Sample rate setting determined by MCS register (Register 0x00, Bits[3:1]) Automatic sample rate detection	0x0	RW

### SERIAL AUDIO INTERFACE AND SAMPLE RATE CONTROL (SAI\_FMT1) REGISTER

Table 50. Address: 0x02, Reset: 0x02, Name: SAI\_FMT1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	SDATA_FMT	00 01 10 11	Serial data format I <sup>2</sup> S, BCLK delay by 1 Left justified Right justified, 24-bit data Right justified, 16-bit data	0x0	RW
[5:3]	SAI	000 001 010 011 100 101 110 111	Serial audio interface format Stereo I <sup>2</sup> S, left justified, right justified TDM2 TDM4 TDM8 TDM16 Mono PCM Reserved Reserved	0x0	RW

Bits	Bit Name	Settings	Description	Reset	Access
[2:0]	SR	000 001 010 011 100 101 110 111	Sample rate selection 11.025 kHz, 12 kHz 22.05 kHz, 24 kHz 44.1 kHz, 48 kHz 96 kHz 8 kHz 16 kHz 32 kHz Reserved	0x2	RW

### SERIAL AUDIO INTERFACE CONTROL (SAI\_FMT2) REGISTER

Table 51. Address: 0x03, Reset: 0x00, Name: SAI\_FMT2

Bits	Bit Name	Settings	Description	Reset	Access
7	LPST	0 1	Small power stage enable Disabled Enabled	0x0	RW
[6:5]	LR_SEL	00 01 10 11	L/R channel selector Select left channel Select right channel Select (left + right)/2 Select (left – right)/2	0x0	RW
4	LRCLK_MODE	0 1	LRCLK mode selection for TDM operation 50% duty cycle LRCLK Pulse mode LRCLK	0x0	RW
3	LRCLK_POL	0 1	LRCLK polarity control Normal LRCLK operation Inverted LRCLK operation	0x0	RW
2	SAI_MSB	0 1	SDATA bit stream order MSB first SDATA LSB first SDATA	0x0	RW
1	BCLK_TDMC	0 1	BCLK cycles per frame in TDM modes select 32 BCLK cycles per slot 16 BCLK cycles per slot	0x0	RW
0	BCLK_EDGE	0 1	BCLK active edge select Rising BCLK edge used (if PDM_MODE = 1, L data is registered on the rising edge, and R data is registered on the falling edge) Falling BCLK edge used (if PDM_MODE = 1, R data is registered on the rising edge, and L data is registered on the falling edge)	0x0	RW

**CHANNEL MAPPING CONTROL REGISTER**

Table 52. Address: 0x04, Reset: 0x10, Name: Channel Mapping Control

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	CH_SEL_R	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Right channel mapping select Channel 0 from SAI to right output Channel 1 from SAI to right output Channel 2 from SAI to right output Channel 3 from SAI to right output Channel 4 from SAI to right output Channel 5 from SAI to right output Channel 6 from SAI to right output Channel 7 from SAI to right output Channel 8 from SAI to right output Channel 9 from SAI to right output Channel 10 from SAI to right output Channel 11 from SAI to right output Channel 12 from SAI to right output Channel 13 from SAI to right output Channel 14 from SAI to right output Channel 15 from SAI to right output	0x1	RW
[3:0]	CH_SEL_L	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Left channel mapping select Channel 0 from SAI to left output Channel 1 from SAI to left output Channel 2 from SAI to left output Channel 3 from SAI to left output Channel 4 from SAI to left output Channel 5 from SAI to left output Channel 6 from SAI to left output Channel 7 from SAI to left output Channel 8 from SAI to left output Channel 9 from SAI to left output Channel 10 from SAI to left output Channel 11 from SAI to left output Channel 12 from SAI to left output Channel 13 from SAI to left output Channel 14 from SAI to left output Channel 15 from SAI to left output	0x0	RW

**VOLUME CONTROL BEFORE FDSP (VOL\_BF\_FDSP) REGISTER**

Table 53. Address: 0x05, Reset: 0x40, Name: VOL\_BF\_FDSP

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DIG_VOL		Volume control before FDSP	0x40	RW
		00000000	+24 dB		
		00000001	+23.625 dB		
		00000010	+23.35 dB		
		00000011	+22.875 dB		
		00000100	+22.5 dB		
		00000101	...		
		00111111	+0.375 dB		
		01000000	0 dB		
		01000001	-0.375 dB		
		01000010	...		
		11111101	-70.875 dB		
		11111110	-71.25 dB		
		11111111	Mute		

**VOLUME CONTROL AFTER FDSP (VOL\_AF\_FDSP) REGISTER**

Table 54. Address: 0x06, Reset: 0x40, Name: VOL\_AF\_FDSP

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PDP_VOL		Volume control after FDSP	0x40	RW
		00000000	+24 dB		
		00000001	+23.625 dB		
		00000010	+23.35 dB		
		00000011	+22.875 dB		
		00000100	+22.5 dB		
		00000101	...		
		00111111	+0.375 dB		
		01000000	0 dB		
		01000001	-0.375 dB		
		01000010	...		
		11111101	-70.875 dB		
		11111110	-71.25 dB		
		11111111	Mute		

**VOLUME AND MUTE CONTROL REGISTER**

Table 55. Address: 0x07, Reset: 0x20, Name: Volume and Mute Control

Bits	Bit Name	Settings	Description	Reset	Access
7	CLK_LOSS_DET		Clock loss detect enable	0x0	RW
		0	Clock loss detect disabled		
		1	Clock loss detect enabled		
[6:4]	SR_AUTO		Auto detected sample rate	0x2	R
		000	11.025 kHz/12 kHz		
		001	22.05 kHz/24 kHz		
		010	44.1 kHz/48 kHz		
		011	96 kHz		
		100	8 kHz		
		101	16 kHz		
		110	32 kHz		
		111	Wrong sample rate		
3	Reserved		Reserved	0x0	RW

Bits	Bit Name	Settings	Description	Reset	Access
2	PDP_VOL_FORCE	0 1	PDP volume fade enable Soft (default) Force	0x0	RW
1	DIG_VOL_FORCE	0 1	DIG volume fade enable Soft (default) Force	0x0	RW
0	ANA_GAIN	0 1	Analog gain control 3.6 V gain 5 V gain	0x0	RW

**DPLL\_CTRL REGISTER**

Table 56. Address: 0x08, Reset: 0x00, Name: DPLL\_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
7	Reserved		Reserved	0x0	RW
[6:4]	DPLL_REF_SEL	000 001 010	DPLL source clock selection Select MCLK as DPLL reference clock Select BCLK as DPLL reference clock Select LRCLK as DPLL reference clock	0x0	RW
[3:0]	DPLL_NDIV	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010	DPLL output clock frequency Reference clock frequency × 1 Reference clock frequency × 1024 Reference clock frequency × 512 Reference clock frequency × 256 Reference clock frequency × 128 Reference clock frequency × 64 Reference clock frequency × 32 Reference clock frequency × 16 Reference clock frequency × 8 Reference clock frequency × 4 Reference clock frequency × 2	0x0	RW

**APLL\_CTRL1 REGISTER**

Table 57. Address: 0x09, Reset: 0x00, Name: APLL\_CTRL1

Bits	Bit Name	Description	Reset	Access
[7:0]	M_HI	Denominator (M) of the fractional APLL upper byte	0x00	RW

**APLL\_CTRL2 REGISTER**

Table 58. Address: 0x0A, Reset: 0x00, Name: APLL\_CTRL2

Bits	Bit Name	Description	Reset	Access
[7:0]	M_LO	Denominator (M) of the fractional APLL lower byte	0x00	RW

**APLL\_CTRL3 REGISTER**

Table 59. Address: 0x0B, Reset: 0x00, Name: APLL\_CTRL3

Bits	Bit Name	Description	Reset	Access
[7:0]	N_HI	Numerator (N) of the fractional APLL upper byte	0x00	RW

**APLL\_CTRL4 REGISTER**

Table 60. Address: 0x0C, Reset: 0x00, Name: APLL\_CTRL4

Bits	Bit Name	Description	Reset	Access
[7:0]	N_LO	Numerator (N) of the fractional APLL lower byte	0x00	RW



**APLL\_CTRL5 REGISTER****Table 61. Address: 0x0D, Reset: 0x00, Name: APLL\_CTRL5**

Bits	Bit Name	Settings	Description	Reset	Access
7	Reserved		Reserved	0x0	RW
[6:3]	R	0010 0011 0100 0101 0110 0111 1000	Integer part of APLL R = 2 R = 3 R = 4 R = 5 R = 6 R = 7 R = 8	0x0	RW
[2:1]	X	00 01 10 11	APLL input clock divider X = 1 X = 2 X = 3 X = 4	0x0	RW
0	Type	0 1	APLL operation mode Integer Fractional	0x0	RW

**APLL\_CTRL6 REGISTER****Table 62. Address: 0x0E, Reset: 0x30, Name: APLL\_CTRL6**

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	FSYS_DPLL	00 01 10 11	Analog OSC Clock Rate 1 Analog OSC Clock Rate 2 Analog OSC Clock Rate 3 Analog OSC Clock Rate 4	0x0	RW
5	DPLL_BYPASS	0 1	Enable DPLL Bypass DPLL (default)	0x1	RW
4	APLL_BYPASS	0 1	Enable APLL Bypass APLL (default)	0x1	RW
3	DPLL_LOCK	0 1	DPLL not locked DPLL locked	0x0	R
2	APLL_LOCK	0 1	APLL not locked APLL locked	0x0	R
1	PLLEN	0 1	Disable internal PLL (default) Enable internal PLL	0x0	RW
0	COREN	0 1	Core clock enable Core clock disable (default) Core clock enable	0x0	RW

**FAULT\_CTRL1 REGISTER**

Table 63. Address: 0x0F, Reset: 0x00, Name: FAULT\_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	Reserved			0x0	RW
4	PDB_LINE	0 1	Single end lineout enable Disabled Enabled	0x0	RW
3	PDB_ZC	0 1	Lineout calibration enable Disabled Enabled	0x0	RW
2	CLK_LOSS	0 1	Clock for DAC and Class-D lost Normal operation Loss of clock signal	0x0	R
1	OC	0 1	Right channel overcurrent fault Normal operation Right channel overcurrent fault	0x0	R
0	OT	0 1	Overtemperature fault status Normal operation Overtemperature fault	0x0	R

**FAULT\_CTRL2 REGISTER**

Table 64. Address: 0x10, Reset: 0x4C, Name: FAULT\_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
7	Reserved			0x0	RW
[6:5]	AR_TIME	00 01 10 11	Auto recovery time 10 ms auto fault recovery delay 20 ms auto fault recovery delay 40 ms auto fault recovery delay 80 ms auto fault recovery delay	0x2	RW
4	MRCV	1	Manual fault recovery Writing of 1 causes a manual fault recovery attempt when ARCV = 11	0x0	RW
[3:2]	MAX_AR	00 01 10 11	Maximum fault recovery attempts 1 auto recovery attempt 3 auto recovery attempts 7 auto recovery attempts Unlimited auto recovery attempts	0x3	RW
[1:0]	ARCV	00 01 10 11	Auto fault recovery control Auto fault recovery for overtemperature and overcurrent faults Auto fault recovery for overtemperature fault only Auto fault recovery for overcurrent fault only No auto fault recovery	0x0	RW

**DEEMP\_CTRL REGISTER**

Table 65. Address: 0x14, Reset: 0x00, Name: DEEMP\_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	Reserved			0x00	RW
[2:1]	DEEMP_FS	00 01 10 11	De-emphasis sample rate selection Set coefficients to all zero 48 kHz 44.1 kHz 32 kHz	0x0	RW
0	DEEMP_EN	1 0	De-emphasis enable De-emphasis filter enable De-emphasis filter disable	0x0	RW

**HPF\_CTRL REGISTER**

Table 66. Address: 0x15, Reset: 0x00, Name: HPF\_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	Reserved			0x0	RW
[5:2]	HPFCUT	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	High-pass filter 3 dB cutoff frequency 3.7 Hz (default) 50 Hz 100 Hz 150 Hz 200 Hz 250 Hz 300 Hz 350 Hz 400 Hz 450 Hz 500 Hz 550 Hz 600 Hz 650 Hz 700 Hz 750 Hz	0x00	RW
1	HPFOR	0 1	Store/clear high-pass filter dc value when HPF disabled Clear dc value Store dc value	0x0	RW
0	HPFEN	0 1	High-pass filter enabled HPF disabled (default) HPF enabled	0x0	RW

**EQ1\_COEF0\_HI REGISTER**

Table 67. Address: 0x16, Reset: 0x00, Name: EQ1\_COEF0\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ1_COEF0_HI	EQ coefficient	0x00	RW

**EQ1\_COEF0\_LO REGISTER**

Table 68. Address: 0x17, Reset: 0x00, Name: EQ1\_COEF0\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ1_COEF0_LO	EQ coefficient	0x00	RW

**EQ1\_COEF1\_HI REGISTER**

Table 69. Address: 0x18, Reset: 0x00, Name: EQ1\_COEF1\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ1_COEF1_HI	EQ coefficient	0x00	RW

**EQ1\_COEF1\_LO REGISTER**

Table 70. Address: 0x19, Reset: 0x00, Name: EQ1\_COEF1\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ1_COEF1_LO	EQ coefficient	0x00	RW

**EQ1\_COEF2\_HI REGISTER**

Table 71. Address: 0x1A, Reset: 0x00, Name: EQ1\_COEF2\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ1_COEF2_HI	EQ coefficient	0x00	RW

**EQ1\_COEF2\_LO REGISTER**

Table 72. Address: 0x1B, Reset: 0x00, Name: EQ1\_COEF2\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ1_COEF2_LO	EQ coefficient	0x00	RW

**EQ1\_COEF3\_HI REGISTER**

Table 73. Address: 0x1C, Reset: 0x00, Name: EQ1\_COEF3\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ1_COEF3_HI	EQ coefficient	0x00	RW

**EQ1\_COEF3\_LO REGISTER**

Table 74. Address: 0x1D, Reset: 0x00, Name: EQ1\_COEF3\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ1_COEF3_LO	EQ coefficient	0x00	RW

**EQ1\_COEF4\_HI REGISTER**

Table 75. Address: 0x1E, Reset: 0x00, Name: EQ1\_COEF4\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ1_COEF4_HI	EQ coefficient	0x00	RW

**EQ1\_COEF4\_LO REGISTER**

Table 76. Address: 0x1F, Reset: 0x00, Name: EQ1\_COEF4\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ1_COEF4_LO	EQ coefficient	0x00	RW

**EQ2\_COEF0\_HI REGISTER**

Table 77. Address: 0x20, Reset: 0x00, Name: EQ2\_COEF0\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ2_COEF0_HI	EQ coefficient	0x00	RW

**EQ2\_COEF0\_LO REGISTER**

Table 78. Address: 0x21, Reset: 0x00, Name: EQ2\_COEF0\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ2_COEF0_LO	EQ coefficient	0x00	RW

**EQ2\_COEF1\_HI REGISTER**

Table 79. Address: 0x22, Reset: 0x00, Name: EQ2\_COEF1\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ2_COEF1_HI	EQ coefficient	0x00	RW

**EQ2\_COEF1\_LO REGISTER**

Table 80. Address: 0x23, Reset: 0x00, Name: EQ2\_COEF1\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ2_COEF1_LO	EQ coefficient	0x00	RW

**EQ2\_COEF2\_HI REGISTER**

Table 81. Address: 0x24, Reset: 0x00, Name: EQ2\_COEF2\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ2_COEF2_HI	EQ coefficient	0x00	RW

**EQ2\_COEF2\_LO REGISTER**

Table 82. Address: 0x25, Reset: 0x00, Name: EQ2\_COEF2\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ2_COEF2_LO	EQ coefficient	0x00	RW

**EQ2\_COEF3\_HI REGISTER**

Table 83. Address: 0x26, Reset: 0x00, Name: EQ2\_COEF3\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ2_COEF3_HI	EQ coefficient	0x00	RW

**EQ2\_COEF3\_LO REGISTER**

Table 84. Address: 0x27, Reset: 0x00, Name: EQ2\_COEF3\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ2_COEF3_LO	EQ coefficient	0x00	RW

**EQ2\_COEF4\_HI REGISTER**

Table 85. Address: 0x28, Reset: 0x00, Name: EQ2\_COEF4\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ2_COEF4_HI	EQ coefficient	0x00	RW

**EQ2\_COEF4\_LO REGISTER**

Table 86. Address: 0x29, Reset: 0x00, Name: EQ2\_COEF4\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ2_COEF4_LO	EQ coefficient	0x00	RW

**EQ3\_COEF0\_HI REGISTER**

Table 87. Address: 0x2A, Reset: 0x00, Name: EQ3\_COEF0\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ3_COEF0_HI	EQ coefficient	0x00	RW

**EQ3\_COEF0\_LO REGISTER**

Table 88. Address: 0x2B, Reset: 0x00, Name: EQ3\_COEF0\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ3_COEF0_LO	EQ coefficient	0x00	RW

**EQ3\_COEF1\_HI REGISTER**

Table 89. Address: 0x2C, Reset: 0x00, Name: EQ3\_COEF1\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ3_COEF1_HI	EQ coefficient	0x00	RW

**EQ3\_COEF1\_LO REGISTER**

Table 90. Address: 0x2D, Reset: 0x00, Name: EQ3\_COEF1\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ3_COEF1_LO	EQ coefficient	0x00	RW

**EQ3\_COEF2\_HI REGISTER**

Table 91. Address: 0x2E, Reset: 0x00, Name: EQ3\_COEF2\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ3_COEF2_HI	EQ coefficient	0x00	RW

**EQ3\_COEF2\_LO REGISTER**

Table 92. Address: 0x2F, Reset: 0x00, Name: EQ3\_COEF2\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ3_COEF2_LO	EQ coefficient	0x00	RW

**EQ3\_COEF3\_HI REGISTER**

Table 93. Address: 0x30, Reset: 0x00, Name: EQ3\_COEF3\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ3_COEF3_HI	EQ coefficient	0x00	RW

**EQ3\_COEF3\_LO REGISTER**

Table 94. Address: 0x31, Reset: 0x00, Name: EQ3\_COEF3\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ3_COEF3_LO	EQ coefficient	0x00	RW

**EQ3\_COEF4\_HI REGISTER**

Table 95. Address: 0x32, Reset: 0x00, Name: EQ3\_COEF4\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ3_COEF4_HI	EQ coefficient	0x00	RW

**EQ3\_COEF4\_LO REGISTER**

Table 96. Address: 0x33, Reset: 0x00, Name: EQ3\_COEF4\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ3_COEF4_LO	EQ coefficient	0x00	RW

**EQ4\_COEF0\_HI REGISTER**

Table 97. Address: 0x34, Reset: 0x00, Name: EQ4\_COEF0\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ4_COEF0_HI	EQ coefficient	0x00	RW

**EQ4\_COEF0\_LO REGISTER**

Table 98. Address: 0x35, Reset: 0x00, Name: EQ4\_COEF0\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ4_COEF0_LO	EQ coefficient	0x00	RW

**EQ4\_COEF1\_HI REGISTER**

Table 99. Address: 0x36, Reset: 0x00, Name: EQ4\_COEF1\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ4_COEF1_HI	EQ coefficient	0x00	RW

**EQ4\_COEF1\_LO REGISTER**

Table 100. Address: 0x37, Reset: 0x00, Name: EQ4\_COEF1\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ4_COEF1_LO	EQ coefficient	0x00	RW

**EQ4\_COEF2\_HI REGISTER**

Table 101. Address: 0x38, Reset: 0x00, Name: EQ4\_COEF2\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ4_COEF2_HI	EQ coefficient	0x00	RW

**EQ4\_COEF2\_LO REGISTER**

Table 102. Address: 0x39, Reset: 0x00, Name: EQ4\_COEF2\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ4_COEF2_LO	EQ coefficient	0x00	RW

**EQ4\_COEF3\_HI REGISTER**

Table 103. Address: 0x3A, Reset: 0x00, Name: EQ4\_COEF3\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ4_COEF3_HI	EQ coefficient	0x00	RW

**EQ4\_COEF3\_LO REGISTER**

Table 104. Address: 0x3B, Reset: 0x00, Name: EQ4\_COEF3\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ4_COEF3_LO	EQ coefficient	0x00	RW

**EQ4\_COEF4\_HI REGISTER**

Table 105. Address: 0x3C, Reset: 0x00, Name: EQ4\_COEF4\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ4_COEF4_HI	EQ coefficient	0x00	RW

**EQ4\_COEF4\_LO REGISTER**

Table 106. Address: 0x3D, Reset: 0x00, Name: EQ4\_COEF4\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ4_COEF4_LO	EQ coefficient	0x00	RW

**EQ5\_COEF0\_HI REGISTER**

Table 107. Address: 0x3E, Reset: 0x00, Name: EQ5\_COEF0\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ5_COEF0_HI	EQ coefficient	0x00	RW

**EQ5\_COEF0\_LO REGISTER**

Table 108. Address: 0x3F, Reset: 0x00, Name: EQ5\_COEF0\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ5_COEF0_LO	EQ coefficient	0x00	RW

**EQ5\_COEF1\_HI REGISTER**

Table 109. Address: 0x40, Reset: 0x00, Name: EQ5\_COEF1\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ5_COEF1_HI	EQ coefficient	0x00	RW

**EQ5\_COEF1\_LO REGISTER**

Table 110. Address: 0x41, Reset: 0x00, Name: EQ5\_COEF1\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ5_COEF1_LO	EQ coefficient	0x00	RW

**EQ5\_COEF2\_HI REGISTER**

Table 111. Address: 0x42, Reset: 0x00, Name: EQ5\_COEF2\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ5_COEF2_HI	EQ coefficient	0x00	RW

**EQ5\_COEF2\_LO REGISTER**

Table 112. Address: 0x43, Reset: 0x00, Name: EQ5\_COEF2\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ5_COEF2_LO	EQ coefficient	0x00	RW

**EQ5\_COEF3\_HI REGISTER**

Table 113. Address: 0x44, Reset: 0x00, Name: EQ5\_COEF3\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ5_COEF3_HI	EQ coefficient	0x00	RW

**EQ5\_COEF3\_LO REGISTER**

Table 114. Address: 0x45, Reset: 0x00, Name: EQ5\_COEF3\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ5_COEF3_LO	EQ coefficient	0x00	RW

**EQ5\_COEF4\_HI REGISTER**

Table 115. Address: 0x46, Reset: 0x00, Name: EQ5\_COEF4\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ5_COEF4_HI	EQ coefficient	0x00	RW

**EQ5\_COEF4\_LO REGISTER**

Table 116. Address: 0x47, Reset: 0x00, Name: EQ5\_COEF4\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ5_COEF4_LO	EQ coefficient	0x00	RW

**EQ6\_COEF0\_HI REGISTER**

Table 117. Address: 0x48, Reset: 0x00, Name: EQ6\_COEF0\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ6_COEF0_HI	EQ coefficient	0x00	RW

**EQ6\_COEF0\_LO REGISTER**

Table 118. Address: 0x49, Reset: 0x00, Name: EQ6\_COEF0\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ6_COEF0_LO	EQ coefficient	0x00	RW

**EQ6\_COEF1\_HI REGISTER**

Table 119. Address: 0x4A, Reset: 0x00, Name: EQ6\_COEF1\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ6_COEF1_HI	EQ coefficient	0x00	RW

**EQ6\_COEF1\_LO REGISTER**

Table 120. Address: 0x4B, Reset: 0x00, Name: EQ6\_COEF1\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ6_COEF1_LO	EQ coefficient	0x00	RW



**EQ6\_COEF2\_HI REGISTER**

Table 121. Address: 0x4C, Reset: 0x00, Name: EQ6\_COEF2\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ6_COEF2_HI	EQ coefficient	0x00	RW

**EQ6\_COEF2\_LO REGISTER**

Table 122. Address: 0x4D, Reset: 0x00, Name: EQ6\_COEF2\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ6_COEF2_LO	EQ coefficient	0x00	RW

**EQ7\_COEF0\_HI REGISTER**

Table 123. Address: 0x4E, Reset: 0x00, Name: EQ7\_COEF0\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ7_COEF0_HI	EQ coefficient	0x00	RW

**EQ7\_COEF0\_LO REGISTER**

Table 124. Address: 0x4F, Reset: 0x00, Name: EQ7\_COEF0\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ7_COEF0_LO	EQ coefficient	0x00	RW

**EQ7\_COEF1\_HI REGISTER**

Table 125. Address: 0x50, Reset: 0x00, Name: EQ7\_COEF1\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ7_COEF1_HI	EQ coefficient	0x00	RW

**EQ7\_COEF1\_LO REGISTER**

Table 126. Address: 0x51, Reset: 0x00, Name: EQ7\_COEF1\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ7_COEF1_LO	EQ coefficient	0x00	RW

**EQ7\_COEF2\_HI REGISTER**

Table 127. Address: 0x52, Reset: 0x00, Name: EQ7\_COEF2\_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ7_COEF2_HI	EQ coefficient	0x00	RW

**EQ7\_COEF2\_LO REGISTER**

Table 128. Address: 0x53, Reset: 0x00, Name: EQ7\_COEF2\_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	EQ7_COEF2_LO	EQ coefficient	0x00	RW

**EQ\_CTRL1 REGISTER**

Table 129. Address: 0x54, Reset: 0x00, Name: EQ\_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	EQ_RESERVED		Reserved	0x0	RW
3	EQ_UPDING	0 1	EQ coefficient updating flag None EQ coefficients updating	0x0	R
2	EQ_UPD_CLR	0 1	EQ coefficient update clear Normal operation Interrupt coefficient update	0x0	W
1	EQ_FORMAT	0 1	EQ coefficient format selection Normal Large gain	0x0	RW
0	EQ_UPD	1 0	EQ coefficient registers update flag Update None	0x0	R

**EQ\_CTRL2 REGISTER**

Table 130. Address: 0x55, Reset: 0x00, Name: EQ\_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
7	EQEN	0 1	EQ enable EQ disable EQ enable	0x0	RW
6	EQBP7	0 1	EQ Band 7 bypass when EQ enabled No bypass Bypass EQ Band 7	0x0	RW
5	EQBP6	0 1	EQ Band 6 bypass when EQ enabled No bypass Bypass EQ Band 6	0x0	RW
4	EQBP5	0 1	EQ Band 5 bypass when EQ enabled No bypass Bypass EQ Band 5	0x0	RW
3	EQBP4	0 1	EQ Band 4 bypass when EQ enabled No bypass Bypass EQ Band 4	0x0	RW
2	EQBP3	0 1	EQ Band 3 bypass when EQ enabled No bypass Bypass EQ Band 3	0x0	RW
1	EQBP2	0 1	EQ Band 2 bypass when EQ enabled No bypass Bypass EQ Band 2	0x0	RW
0	EQBP1	0 1	EQ Band 1 bypass when EQ enabled No bypass Bypass EQ Band 1	0x0	RW

**DRC\_CTRL1 REGISTER**

Table 131. Address: 0x56, Reset: 0x00, Name: DRC\_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	Reserved			0x0	RW
[3:0]	DRCLELTAV	0000 0001 0011 1111	DRC rms detector average time 0 ms(default) 0.075 ms 0.30 ms 24.576 sec	0x0	RW

**DRC\_CTRL2 REGISTER**

Table 132. Address: 0x57, Reset: 0x00, Name: DRC\_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	PEAK_ATT	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	DRC peak detector attack time setting; 16 possible values 0 ms 0.09 ms 0.19 ms 0.37 ms 0.75 ms 1.5 ms 3 ms 6 ms 12 ms 24 ms 48 ms 96 ms 192 ms 384 ms 768 ms 1.536 sec	0x0	RW
[3:0]	PEAK_REL	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	DRC peak detector decay time setting; 16 possible values 0 ms 1.5 ms 3 ms 6 ms 12 ms 24 ms 48 ms 96 ms 192 ms 384 ms 768 ms 1.536 sec 3.072 sec 6.144 sec 12.288 sec 24.576 sec	0x0	RW

**DRC\_CTRL3 REGISTER**

Table 133. Address: 0x58, Reset: 0x00, Name: DRC\_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRC_ATT	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	DRC attack time setting; 16 possible settings 0 ms 0.1 ms 0.19 ms 0.37 ms 0.75 ms 1.5 ms 3 ms 6 ms 12 ms 24 ms 48 ms 96 ms 192 ms 384 ms 768 ms 1.536 sec	0x0	RW
[3:0]	DRC_DEC	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	DRC decay time setting; 16 possible settings 0 ms 1.5 ms 3 ms 6 ms 12 ms 24 ms 48 ms 96 ms 192 ms 384 ms 768 ms 1.536 sec 3.072 sec 6.144 sec 12.288 sec 24.576 sec	0x0	RW

**DRC\_CURVE1 REGISTER**

Table 134. Address: 0x59, Reset: 0x00, Name: DRC\_CURVE1

Bits	Bit Name	Settings	Description	Reset	Access
7	Reserved			0x0	RW
[6:0]	DRC_LT	0000000 0000001 xxxxxxx 1010000	DRC limiter threshold setting, relative to input, in 0.5 dB steps +6 dB +5.5 dB -0.5 dB step -35 dB	0x00	RW

**DRC\_CURVE2 REGISTER**

Table 135. Address: 0x5A, Reset: 0x00, Name: DRC\_CURVE2

Bits	Bit Name	Settings	Description	Reset	Access
7	Reserved			0x0	RW
[6:0]	DRC_CT	0000000 0000001 xxxxxxx 1010000	DRC compressor threshold setting, relative to input in 0.5 dB steps +6 dB +5.5 dB -0.5 dB step -35 dB	0x00	RW

**DRC\_CURVE3 REGISTER**

Table 136. Address: 0x5B, Reset: 0x00, Name: DRC\_CURVE3

Bits	Bit Name	Settings	Description	Reset	Access
7	Reserved			0x0	RW
[6:0]	DRC_SMAX	0000000 0000001 xxxxxxx 1010000	This is the DRC maximum output signal amplitude setting. This is the maximum output level produced by the DRC and is used to indicate the upper compressor threshold. The possible settings are in 0.5 dB steps. +6 dB +5.5 dB -0.5 dB step -35 dB	0x00	RW

**DRC\_CURVE4 REGISTER**

Table 137. Address: 0x5C, Reset: 0x88, Name: DRC\_CURVE4

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRC_NT	0000 0001 xxxx 1111	DRC noise gating threshold setting, relative to input; 16 possible values in 3 dB steps -51 dB -54 dB -3 dB step -96 dB	0x8	RW
[3:0]	DRC_ET	0000 0001 xxxx 1111	DRC expander threshold setting, relative to input; 16 possible values in 3 dB steps -36 dB -39 dB -3 dB step -81 dB	0x8	RW

**DRC\_CURVE5 REGISTER**

Table 138. Address: 0x5D, Reset: 0x00, Name: DRC\_CURVE5

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	Reserved			0x0	RW
[3:0]	DRC_SMIN	0000 0001 xxxx 1011 1111	DRC minimum output signal level -51 dB(default) -54 dB -3 dB step -84 dB -96 dB	0x0	RW

**DRC\_HOLD\_TIME REGISTER**

Table 139. Address: 0x5E, Reset: 0x00, Name: DRC\_HOLD\_TIME

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DRCHTNG	0000 0001 xxxx 0111 1111	DRC hold time for noise gating 0 ms(default) 0.67 ms Double time 42.67 ms 43.7 sec	0x0	RW
[3:0]	DRCHTNOR	0000 0001 xxxx 0111 1111	DRC hold time for normal operation 0 ms(default) 0.67 ms Double time 42.67 ms 43.7 sec	0x0	RW

**DRC\_RIPPLE\_CTRL REGISTER**

Table 140. Address: 0x5F, Reset: 0x00, Name: DRC\_RIPPLE\_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	Reserved			0x0	RW
[1:0]	DRCRRH	00 01 10 11	DRC ripple remove threshold 0 dB (default) 0.28 dB 0.47 dB 0.75 dB	0x0	RW

**DRC MODE CONTROL REGISTER**

Table 141. Address: 0x60, Reset: 0x3C, Name: DRC Mode Control

Bits	Bit Name	Settings	Description	Reset	Access
7	VBAT_EN	0 1	VBAT tracking enable VBAT tracking disable VBAT tracking enable	0x0	RW
6	LIM_SRC	0 1	Limiter source selection RMS Peak	0x0	RW
5	LIM_EN	0 1	Limiter enable Limiter function disabled Limiter function enabled	0x1	RW
4	COMP_EN	0 1	Compressor enable Compressor function disabled Compressor function enabled	0x1	RW
3	EXP_EN	0 1	Expander enable Expander function disabled Expander function enabled	0x1	RW
2	NG_EN	0 1	Noise gate enable Noise gate function disabled Noise gate function enabled	0x1	RW
[1:0]	DRC_EN	0 1	DRC enable DRC disabled DRC enabled	0x0	RW

**FDSP\_EN REGISTER**

Table 142. Address: 0x61, Reset: 0x00, Name: FDSP\_EN

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	Reserved			0x00	RW
0	FDSP_EN	0 1	FDSP enable Disable FDSP Enable FDSP	0x0	RW

**SPK\_PROT\_EN REGISTER**

Table 143. Address: 0x80, Reset: 0x00, Name: SPK\_PROT\_EN

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	Reserved			0x00	RW
0	SP_EN	0 1	Speaker protection enable Speaker protection disabled (default) Speaker protection enabled	0x0	RW

**TEMP\_AMBIENT REGISTER**

Table 144. Address: 0x81, Reset: 0x19, Name: TEMP\_AMBIENT

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	TEMP_AMBIENT	0x19 0x20	Ambient temperature in degrees Celsius (8.0 integer format) 25°C (default) 32°C	0x19	RW

**SPKR\_DCR REGISTER**

Table 145. Address: 0x82, Reset: 0x40, Name: SPKR\_DCR

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SPKR_DCR	0x34 0x40	Nominal speaker dc resistance in ohms (5.3 unsigned format) 6.5 $\Omega$ 8 $\Omega$ (default)	0x40	RW

**SPKR\_TC REGISTER**

Table 146. Address: 0x83, Reset: 0x08, Name: SPKR\_TC

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SPKR_TC	0x08 0x0A	Nominal speaker temperature coefficient, rise in ohms per degrees Celsius (0.8 fractional format). 0.033 $\Omega/^\circ\text{C}$ (default) 0.04 $\Omega/^\circ\text{C}$	0x08	RW

**SP\_CF1\_H REGISTER**

Table 147. Address: 0x84, Reset: 0x3F, Name: SP\_CF1\_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SP_CF1_H	Default	Speaker Temperature Model Coefficient 1, Bits[15:8] in 0.8 fractional format	0x3F	RW

**SP\_CF1\_L REGISTER**

Table 148. Address: 0x85, Reset: 0x81, Name: SP\_CF1\_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SP_CF1_L	Default	Speaker Temperature Model Coefficient 1, Bits[7:0] in 0.8 fractional format	0x81	RW

**SP\_CF2\_H REGISTER**

Table 149. Address: 0x86, Reset: 0x00, Name: SP\_CF2\_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SP_CF2_H	Default	Speaker Temperature Model Coefficient 2, Bits[15:8] in 0.8 fractional format	0x00	RW

**SP\_CF2\_L REGISTER**

Table 150. Address: 0x87, Reset: 0x55, Name: SP\_CF2\_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SP_CF2_L	Default	Speaker Temperature Model Coefficient 2, Bits[7:0] in 0.8 fractional format	0x55	RW

**SP\_CF3\_H REGISTER**

Table 151. Address: 0x88, Reset: 0x01, Name: SP\_CF3\_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SP_CF3_H	Default	Speaker Temperature Model Coefficient 3, Bits[15:8] in 0.8 fractional format	0x01	RW

**SP\_CF3\_L REGISTER**

Table 152. Address: 0x89, Reset: 0x22, Name: SP\_CF3\_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SP_CF3_L	Default	Speaker Temperature Model Coefficient 3, Bits[7:0] in 0.8 fractional format	0x22	RW

**SP\_CF4\_H REGISTER**

Table 153. Address: 0x8A, Reset: 0x02, Name: SP\_CF4\_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SP_CF4_H	Default	Speaker Temperature Model Coefficient 4, Bits[15:8] in 0.8 fractional format	0x02	RW

**SP\_CF4\_L REGISTER**

Table 154. Address: 0x8B, Reset: 0x09, Name: SP\_CF4\_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SP_CF4_L	Default	Speaker Temperature Model Coefficient 4, Bits[7:0] in 0.8 fractional format	0x09	RW

**SPKR\_TEMP REGISTER**

Table 155. Address: 0x8C, Reset: 0x00, Name: SPCR\_TEMP

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SPKR_TEMP	0x20	Speaker voice coil temperature status (8.0 integer format) 32°C	0x00	R

**SPKR\_TEMP\_MAG REGISTER**

Table 156. Address: 0x8D, Reset: 0x00, Name: SPCR\_TEMP\_MAG

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SPKR_TEMP_MAG	0x20	Speaker magnet temperature status (8.0 integer format) 32°C	0x00	R

**MAX\_SPKR\_TEMP REGISTER**

Table 157. Address: 0x8E, Reset: 0x64, Name: MAX\_SPKR\_TEMP

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	MAX_SPKR_TEMP	0x64	Maximum speaker voice coil temperature before gain reduction occurs, 8.0 integer format 100°C	0x64	RW



**SPK\_GAIN REGISTER**

Table 158. Address: 0x8F, Reset: 0x44, Name: SPK\_GAIN

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	SP_RR	0000 0001 0010 0011 0100 0101 0110 0111	Speaker protection gain reduction release rate 0.549 dB/s 0.275 dB/s 0.137 dB/s 0.092 dB/s 0.069 dB/s (default) 0.034 dB/s 0.017 dB/s 0.008 dB/s	0x4	RW
[3:0]	SP_AR	0000 0001 0010 0011 0100 0101 0110 0111	Speaker protection gain reduction attack rate 0.070 dB/ms 0.035 dB/ms 0.017 dB/ms 0.012 dB/ms 0.009 dB/ms (default) 0.006 dB/ms 0.004 dB/ms 0.003 dB/ms	0x4	RW

**SOFT\_RST REGISTER**

Table 159. Address: 0xFF, Reset: 0x00, Name: SOFT\_RST

Bits	Bit Name	Description	Reset	Access
[7:0]	SOFT_RST	Write 0x00 to reset all registers	0x00	W

APPLICATIONS INFORMATION

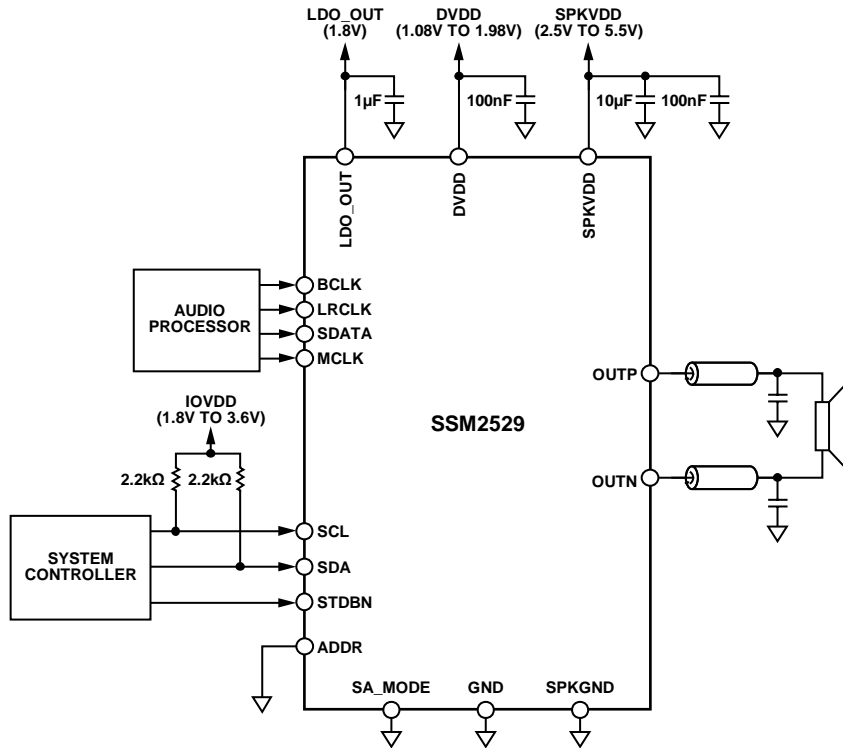


Figure 42. Software Mode (with I<sup>2</sup>C Interface)

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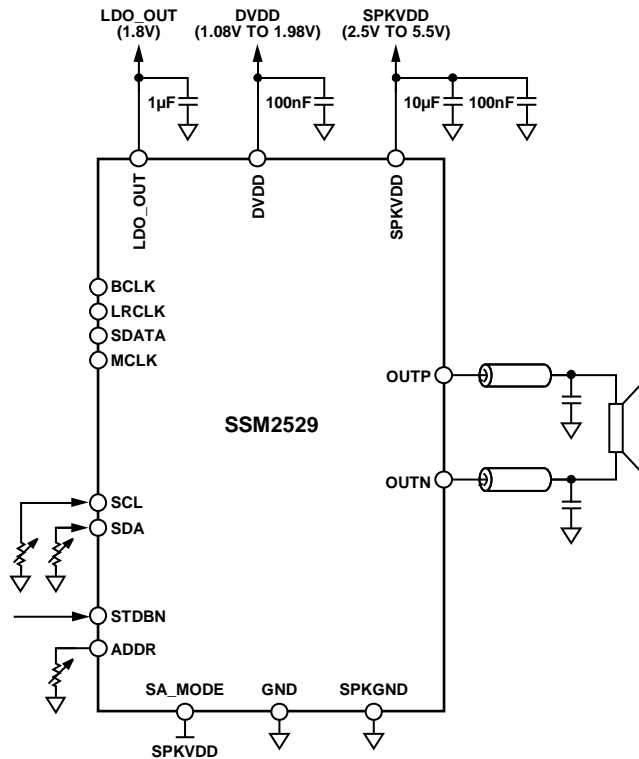
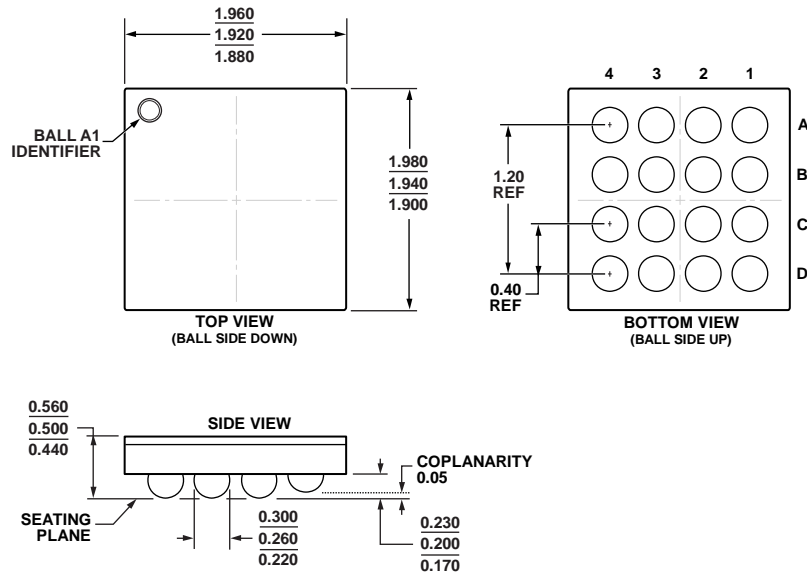


Figure 43. Hardware Standalone Mode

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### OUTLINE DIMENSIONS



02-03-2012-A

Figure 44. 16-Ball Wafer Level Chip Scale Package [WLCSP] (CB-16-12)  
Dimensions shown in millimeters

### ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding
SSM2529ACBZ-RL	-40°C to +85°C	16-Ball Wafer Level Chip Scale Package [WLCSP]	CB-16-12	Y4D
SSM2529ACBZ-R7	-40°C to +85°C	16-Ball Wafer Level Chip Scale Package [WLCSP]	CB-16-12	Y4D
EVAL-SSM2529Z		Evaluation Board		

<sup>1</sup>Z = RoHS Compliant Part.

**NOTES**

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).