TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

SSM3J15FU

High Speed Switching Applications
Analog Switch Applications

Unit: mm

•	Small	package

• Low ON resistance : $R_{on} = 12 \Omega \text{ (max) } (@V_{GS} = -4 \text{ V})$

: $R_{on} = 32 \Omega \text{ (max) } (@V_{GS} = -2.5 \text{ V})$

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V_{DS}	-30	V	
Gate-Source voltage		V_{GSS}	±20	V	
Drain current	DC	ΙD	-100	mA	
Dialii cuitent	Pulse	I _{DP}	-200	ША	
Drain power dissipation (Ta = 25°C)		P _D (Note 1)	150	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55~150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling

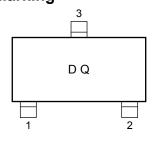
Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Total rating, mounted on FR4 board (25.4 mm \times 25.4 mm \times 1.6 t, Cu Pad: 0.6 mm 2 \times 3)

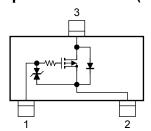
2.1±0.1 1.25±0.1 1.25±0.1 1.0+80 200-510 200-510 1 : GATE 2 : SOURCE 3 : DRAIN JEDEC — JEITA SC-70 TOSHIBA 2-2E1E

Weight: 0.006g(typ.)

Marking



Equivalent Circuit (top view)



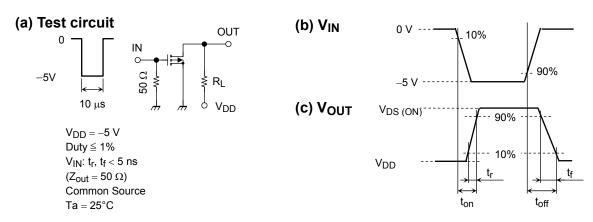
Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	MIN.	TYP.	MAX.	UNIT
Gate leakage current		I _{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$	_	_	±1	μА
Drain-Source breakdown voltage		V (BR) DSS	$I_D = -0.1 \text{ mA}, V_{GS} = 0$	-30			V
Drain cut-off current		I _{DSS}	$V_{DS} = -30 \text{ V}, V_{GS} = 0$			-1	μΑ
Gate threshold voltage		V_{th}	$V_{DS} = -3 \text{ V}, I_D = -0.1 \text{ mA}$	-1.1		-1.7	>
Forward transfer admittance		Y _{fs}	$V_{DS} = -3 \text{ V}, I_D = -10 \text{ mA}$	20			mS
Drain-Source ON resistance		R _{DS} (ON)	$I_D = -10 \text{ mA}, V_{GS} = -4 \text{ V}$		8	12	Ω
			$I_D = -1 \text{ mA}, V_{GS} = -2.5 \text{ V}$		14	32	
Input capacitance		C _{iss}	$V_{DS} = -3 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		9.1		pF
Reverse transfer capacitance		C _{rss}		_	3.5		pF
Output capacitance		Coss		_	8.6	_	pF
Switching time	Turn-on time	t _{on}	$V_{DD} = -5 \text{ V}, I_D = -10 \text{ mA}, $ $V_{GS} = 0 \sim -5 \text{ V}$		65		ns
	Turn-off time	t _{off}		_	175	_	

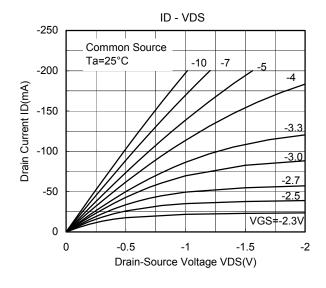
Switching Time Test Circuit

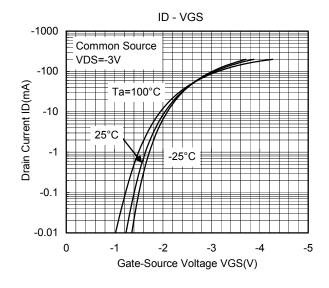


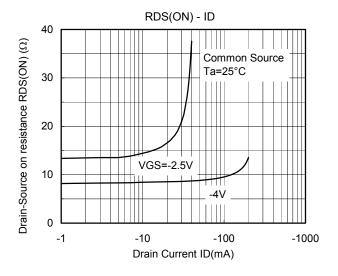
Precaution

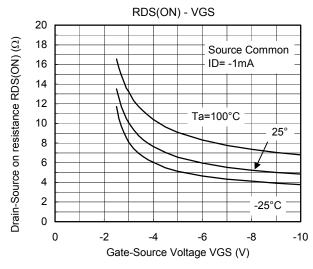
 V_{th} can be expressed as voltage between gate and source when low operating current value is $I_D=-100~\mu A$ for this product. For normal switching operation, $V_{GS~(on)}$ requires higher voltage than V_{th} and $V_{GS~(off)}$ requires lower ${\rm voltage}$ than V_{th} . (Relationship can be established as follows: $V_{GS~(off)} < V_{th} < V_{GS~(on)}$)

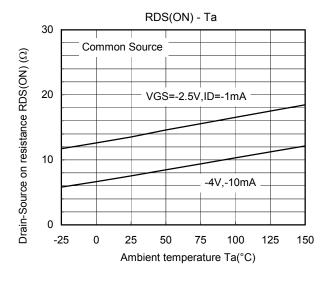
Please take this into consideration for using the device.

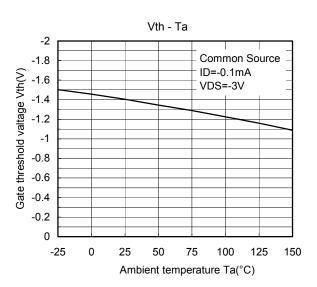


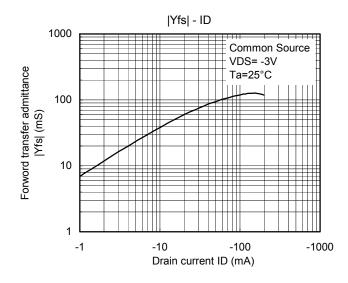


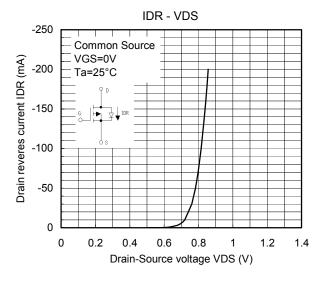


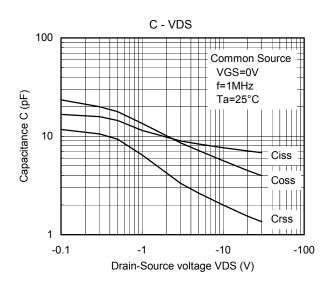


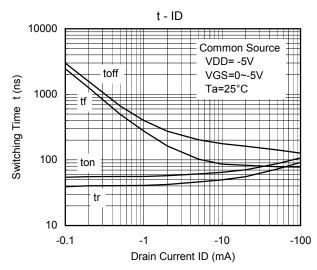


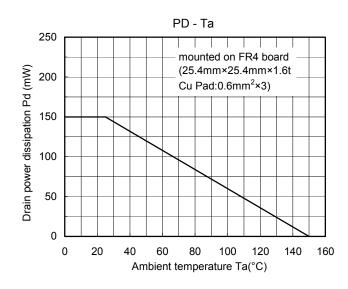












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20070701-EN GENERAL

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