

512 Kbit / 1 Mbit / 2 Mbit / 4 Mbit (x8) Many-Time Programmable Flash

SST37VF512 / SST37VF010 / SST37VF020 / SST37VF040



Data Sheet

FEATURES:

- **Organized as 64K x8 / 128K x8 / 256K x8 / 512K x8**
- **2.7-3.6V Read Operation**
- **Superior Reliability**
 - Endurance: At least 1000 Cycles
 - Greater than 100 years Data Retention
- **Low Power Consumption:**
 - Active Current: 10 mA (typical)
 - Standby Current: 2 μ A (typical)
- **Fast Read Access Time:**
 - 70 ns
- **Latched Address and Data**
- **Fast Byte-Program Operation:**
 - Byte-Program Time: 15 μ s (typical)
 - Chip Program Time:
 - 1 seconds (typical) for SST37VF512
 - 2 seconds (typical) for SST37VF010
 - 4 seconds (typical) for SST37VF020
 - 8 seconds (typical) for SST37VF040
- **Electrical Erase Using Programmer**
 - Does not require UV source
 - Chip-Erase Time: 100 ms (typical)
- **CMOS I/O Compatibility**
- **JEDEC Standard Byte-wide Flash EEPROM Pinouts**
- **Packages Available**
 - 32-lead PLCC
 - 32-lead TSOP (8mm x 14mm)
 - 32-pin PDIP
 - Non-Pb (lead-free) packages available

PRODUCT DESCRIPTION

The SST37VF512/010/020/040 devices are 64K x8 / 128K x8 / 256K x8 / 512K x8 CMOS, Many-Time Programmable (MTP), low cost flash, manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST37VF512/010/020/040 can be electrically erased and programmed at least 1000 times using an external programmer, e.g., to change the contents of devices in inventory. The SST37VF512/010/020/040 have to be erased prior to programming. These devices conform to JEDEC standard pinouts for byte-wide flash memories.

Featuring high performance Byte-Program, the SST37VF512/010/020/040 provide a typical Byte-Program time of 15 μ s. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with an endurance of at least 1000 cycles. Data retention is rated at greater than 100 years.

The SST37VF512/010/020/040 are suited for applications that require infrequent writes and low power nonvolatile storage. These devices will improve flexibility, efficiency, and performance while matching the low cost in nonvolatile applications that currently use UV-EPROMs, OTPs, and mask ROMs.

To meet surface mount and conventional through hole requirements, the SST37VF512/010/020/040 are offered in 32-lead PLCC, 32-lead TSOP, and 32-pin PDIP packages. See Figures 2, 3, and 4 for pin assignments.

Device Operation

The SST37VF512/010/020/040 devices are nonvolatile memory solutions that can be used instead of standard flash devices if in-system programmability is not required. It is functionally (Read) and pin compatible with industry standard flash products. The device supports electrical Erase operation via an external programmer.

Read

The Read operation of the SST37VF512/010/020/040 is controlled by CE# and OE#. Both CE# and OE# have to be low for the system to obtain data from the outputs. Once the address is stable, the address access time is equal to the delay from CE# to output (T_{CE}). Data is available at the output after a delay of TOE from the falling edge of OE#, assuming the CE# pin has been low and the addresses have been stable for at least $T_{CE}-T_{OE}$. When the CE# pin is high, the chip is deselected and a standby current of only 2 μ A (typical) is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is V_{IH} . Refer to Figure 5 for the timing diagram.



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Byte-Program Operation

The SST37VF512/010/020/040 are programmed by using an external programmer. The programming mode is activated by asserting 11.4-12V on OE# pin and V_{IL} on CE# pin. The device is programmed using a single pulse (WE# pin low) of 15 μs per byte. Using the MTP programming algorithm, the Byte-Program process continues byte-by-byte until the entire chip has been programmed. Refer to Figure 11 for the flowchart and Figure 7 for the timing diagram.

Chip-Erase Operation

The only way to change a data from a “0” to “1” is by electrical erase that changes every bit in the device to “1”. The SST37VF512/010/020/040 use an electrical Chip-Erase operation. The entire chip can be erased in 100 ms (WE# pin low). In order to activate erase mode, the 11.4-12V is applied to OE# and A₉ pins while CE# is low. All other address and data pins are “don’t care”. The falling edge of WE# will start the Chip-Erase operation. Once the chip has been erased, all bytes must be verified for FFH. Refer to Figure 10 for the flowchart and Figure 6 for the timing diagram.

Product Identification Mode

The Product Identification mode identifies the devices as SST37VF512, SST37VF010, SST37VF020, and SST37VF040 and manufacturer as SST. This mode may be accessed by the hardware method. To activate this mode, the programming equipment must force V_H (11.4-12V) on address A₉. Two identifier bytes may then be sequenced from the device outputs by toggling address line A₀. For details, see Table 3 for hardware operation.

TABLE 1: Product Identification

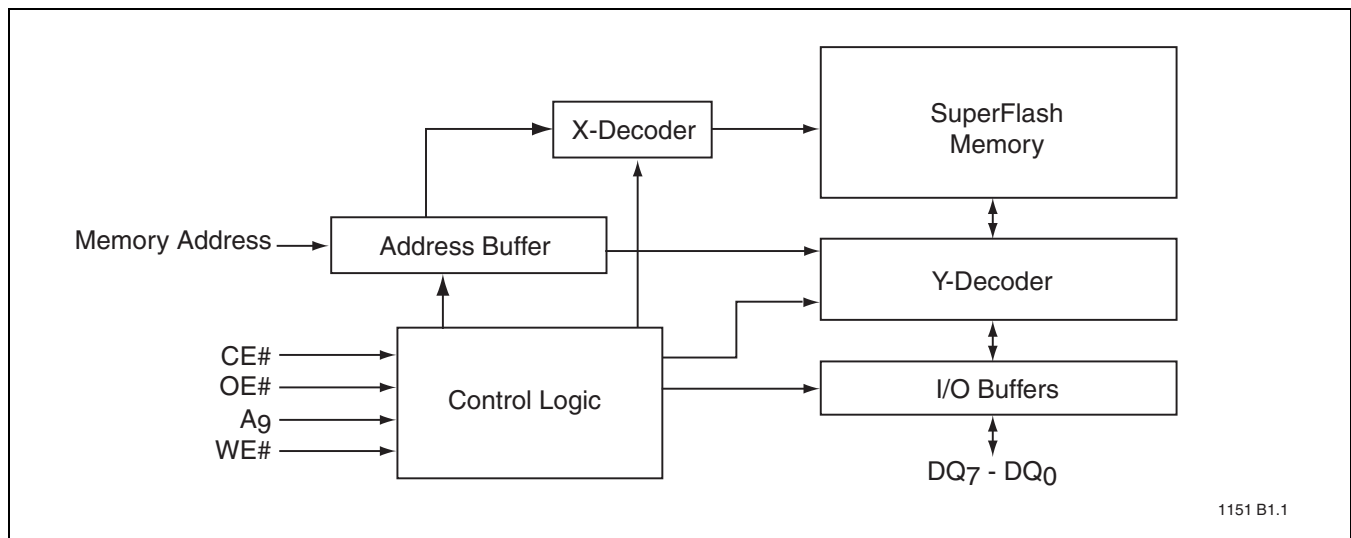
| | Address | Data |
|-------------------|---------|------|
| Manufacturer's ID | 0000H | BFH |
| Device ID | | |
| SST37VF512 | 0001H | C4H |
| SST37VF010 | 0001H | C5H |
| SST37VF020 | 0001H | C6H |
| SST37VF040 | 0001H | C2H |

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Design Considerations

The SST37VF512/010/020/040 should have a 0.1 μF ceramic high frequency, low inductance capacitor connected between V_{DD} and GND. This capacitor should be placed as close to the package terminals as possible.

OE# and A₉ must remain stable at V_H for the entire duration of an Erase operation. OE# must remain stable at V_H for the entire duration of the Program operation.



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FIGURE 1: Functional Block Diagram

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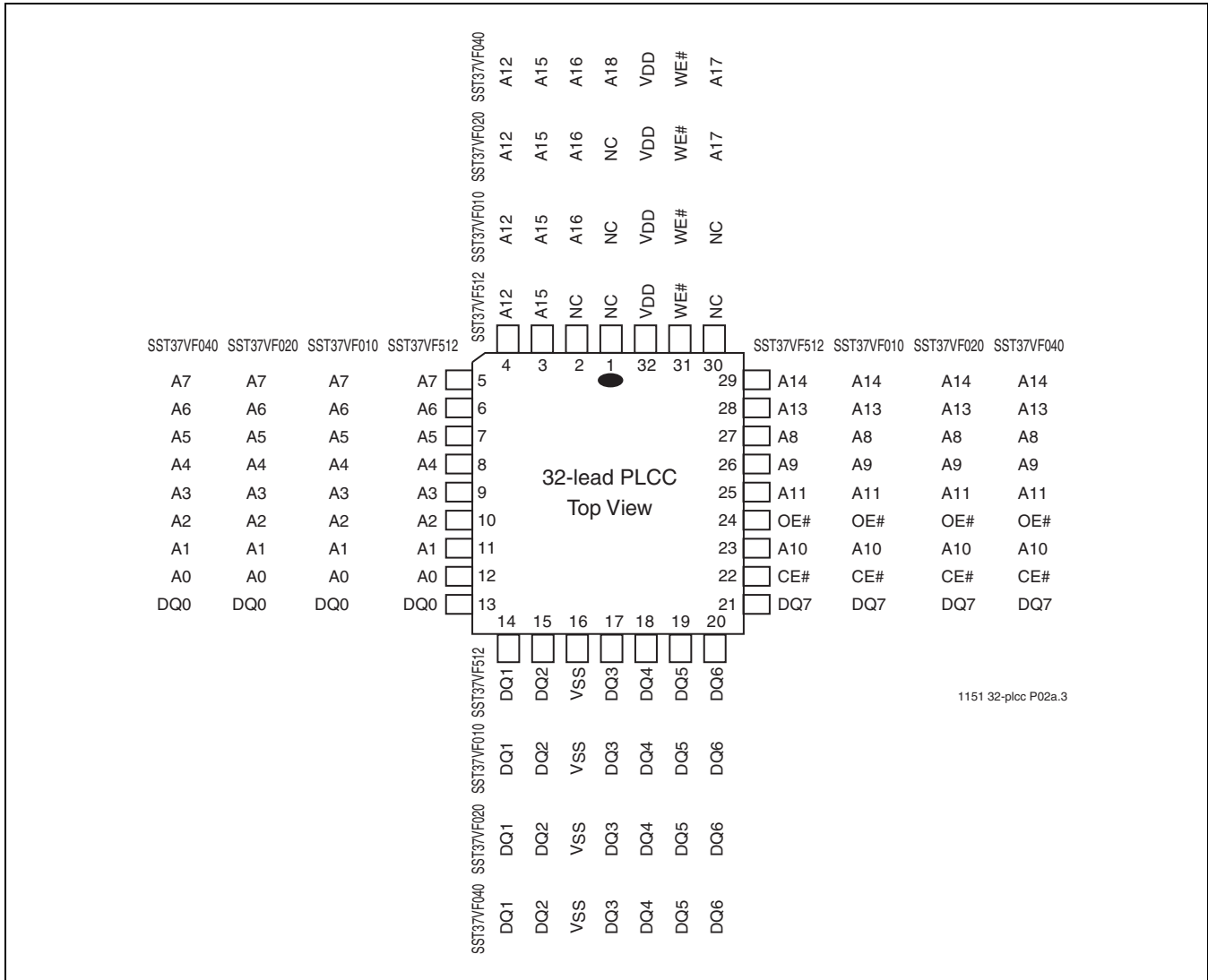


FIGURE 2: Pin Assignments for 32-lead PLCC

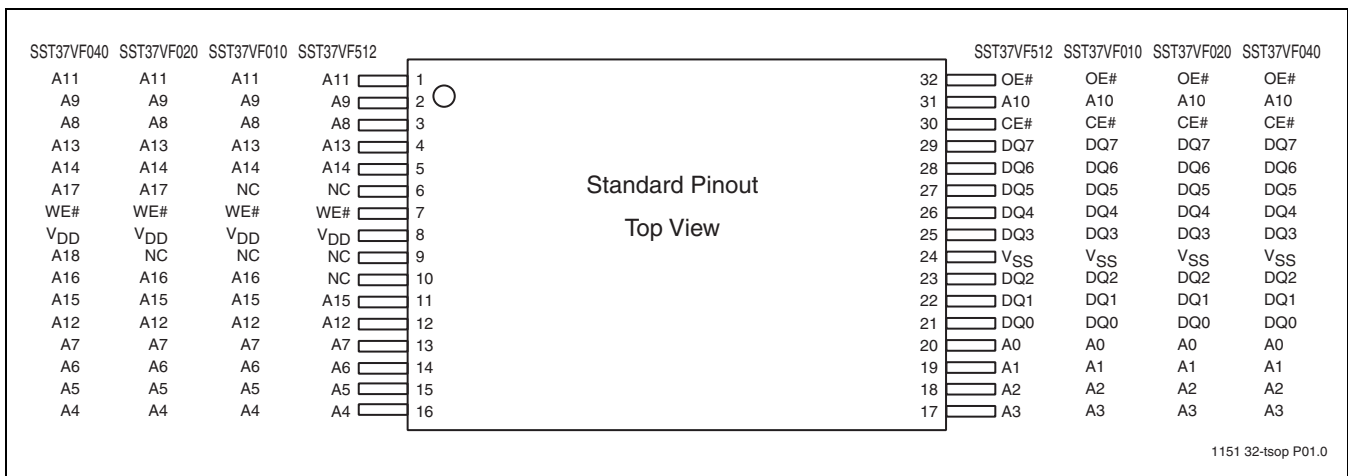


FIGURE 3: Pin Assignments for 32-lead TSOP (8mm x 14mm)



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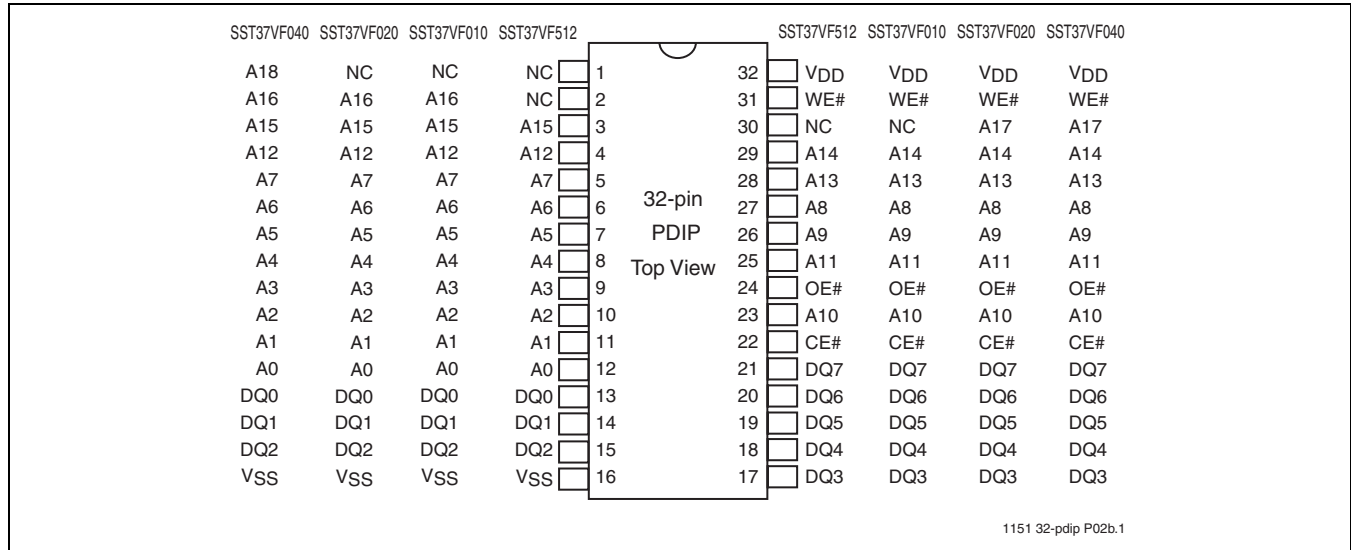


FIGURE 4: Pin Assignments for 32-pin PDIP

TABLE 2: Pin Description

| Symbol | Pin Name | Functions |
|----------------|-------------------|---|
| $A_{MS}^1-A_0$ | Address Inputs | To provide memory addresses. |
| DQ_7-DQ_0 | Data Input/output | To output data during Read cycles and receive input data during Program cycles. The outputs are in tri-state when OE# or CE# is high. |
| CE# | Chip Enable | To activate the device when CE# is low. |
| WE# | Write Enable | To program or erase (WE# = V_{IL} pulse during Program or Erase) |
| OE# | Output Enable | To gate the data output buffers during Read operation when low |
| V_{DD} | Power Supply | To provide 3.0V supply (2.7-3.6V) |
| V_{SS} | Ground | |
| NC | No Connection | Unconnected pins. |

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- A_{MS} = Most significant address
 $A_{MS} = A_{15}$ for SST37VF512, A_{16} for SST37VF010, A_{17} for SST37VF020, and A_{18} for SST37VF040

TABLE 3: Operation Modes Selection

| Mode | CE# | WE# | A_9 | OE# | DQ | Address |
|------------------------|----------|----------|----------|----------------------|---|--|
| Read | V_{IL} | V_{IH} | A_{IN} | V_{IL} | D_{OUT} | A_{IN} |
| Output Disable | V_{IL} | X | X | V_{IH} | High Z | A_{IN} |
| Standby | V_{IH} | X | X | X | High Z | X |
| Chip-Erase | V_{IL} | V_{IL} | V_H | V_H | High Z | X |
| Byte-Program | V_{IL} | V_{IL} | A_{IN} | V_H | D_{IN} | A_{IN} |
| Program/Erase Inhibit | X | V_{IH} | X | X | High Z | X |
| | X | X | X | V_{IL} or V_{IH} | High Z/ D_{OUT} | X |
| Product Identification | V_{IL} | V_{IH} | V_H | V_{IL} | Manufacturer's ID (BFH) Device ID ¹ | $A_{MS}^2 - A_1 = V_{IL}, A_0 = V_{IL}$ $A_{MS}^2 - A_1 = V_{IL}, A_0 = V_{IH}$ |

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- Device ID = C4H for SST37VF512, C5H for SST37VF020, C6H for SST37VF020, and C2H for SST37VF040
- A_{MS} = Most significant address
 $A_{MS} = A_{15}$ for SST37VF512, A_{16} for SST37VF010, A_{17} for SST37VF020, and A_{18} for SST37VF040

Note: X = V_{IL} or V_{IH} (or V_H in case of OE# and A_9)
 $V_H = 11.4-12V$



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Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

| | |
|--|--|
| Temperature Under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| D. C. Voltage on Any Pin to Ground Potential | -0.5V to V _{DD} +0.5V |
| Transient Voltage (<20 ns) on Any Pin to Ground Potential | -2.0V to V _{DD} +2.0V |
| Voltage on A ₉ Pin to Ground Potential | -0.5V to 13.2V |
| Package Power Dissipation Capability (T _A = 25°C) | 1.0W |
| Through Hole Lead Soldering Temperature (10 Seconds) | 300°C |
| Surface Mount Solder Reflow Temperature: | “with-Pb” units ¹ : 240°C for 3 seconds |
| | “non-Pb” units: 260°C for 3 seconds |
| Output Short Circuit Current ² | 50 mA |

1. Certain “with-Pb” package types are capable of 260°C for 3 seconds; please consult the factory for the latest information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

| Range | Ambient Temp | V _{DD} |
|------------|--------------|-----------------|
| Commercial | 0°C to +70°C | 2.7-3.6V |

AC CONDITIONS OF TEST

| | |
|----------------------------|-------------------------|
| Input Rise/Fall Time | 5 ns |
| Output Load | C _L = 100 pF |
| See Figures 8 and 9 | |

TABLE 4: Read Mode DC Operating Characteristics V_{DD}=2.7-3.6V (T_A = 0°C to +70°C (Commercial))

| Symbol | Parameter | Limits | | | Test Conditions |
|------------------|---|----------------------|-----|-------|---|
| | | Min | Max | Units | |
| I _{DD} | V _{DD} Read Current | | 12 | mA | Address input=V _{ILT} /V _{IHT} , at f=1/T _{RC} Min V _{DD} =V _{DD} Max CE#=V _{IL} , OE#=V _{IHT} , all I/Os open |
| I _{SB} | Standby V _{DD} Current | | 15 | μA | CE#=V _{IHC} , V _{DD} =V _{DD} Max |
| I _{LI} | Input Leakage Current | | 1 | μA | V _{IN} =GND to V _{DD} , V _{DD} =V _{DD} Max |
| I _{LO} | Output Leakage Current | | 10 | μA | V _{OUT} =GND to V _{DD} , V _{DD} =V _{DD} Max |
| V _{IL} | Input Low Voltage | | 0.8 | V | V _{DD} =V _{DD} Min |
| V _{IH} | Input High Voltage | 0.7 V _{DD} | | V | V _{DD} =V _{DD} Max |
| V _{IHC} | Input High Voltage (CMOS) | V _{DD} -0.3 | | V | V _{DD} =V _{DD} Max |
| V _{OL} | Output Low Voltage | | 0.2 | V | I _{OL} =100 μA, V _{DD} =V _{DD} Min |
| V _{OH} | Output High Voltage | V _{DD} -0.3 | | V | I _{OH} =-100 μA, V _{DD} =V _{DD} Min |
| I _H | Supervoltage Current for A ₉ | | 200 | μA | CE#=OE#=V _{IL} , A ₉ =V _H Max |

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TABLE 5: Program/Erase DC Operating Characteristics $V_{DD}=2.7-3.6V$ ($T_A = 25^\circ C \pm 5^\circ C$)

| Symbol | Parameter | Limits | | | Test Conditions |
|-------------|-----------------------------------|--------|-----|---------|---|
| | | Min | Max | Units | |
| I_{DD} | V_{DD} Erase or Program Current | | 20 | mA | $CE\#=V_{IL}$, $OE\#=V_H$, $V_{DD}=V_{DD} \text{ Max}$, $WE\#=V_{IL}$ |
| I_{LI} | Input Leakage Current | | 1 | μA | $V_{IN}=GND$ to V_{DD} , $V_{DD}=V_{DD} \text{ Max}$ |
| I_{LO} | Output Leakage Current | | 10 | μA | $V_{OUT}=GND$ to V_{DD} , $V_{DD}=V_{DD} \text{ Max}$ |
| V_H | Supervoltage for A_9 and $OE\#$ | 11.4 | 12 | V | $OE\#=V_H \text{ Max}$, $A_9=V_H \text{ Max}$, $V_{DD}=V_{DD} \text{ Max}$, $CE\#=V_{IL}$ $CE\#=V_{IL}$, $OE\#=11.4-12V$, $V_{DD}=V_{DD} \text{ Max}$, $WE\#=V_{IL}$ |
| I_{HA9} | Supervoltage Current for A_9 | | 200 | μA | |
| $I_{HOE\#}$ | Supervoltage Current for $OE\#$ | | 3 | mA | |

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TABLE 6: Recommended System Power-up Timings

| Symbol | Parameter | Minimum | Units |
|------------------|-----------------------------|---------|---------|
| $T_{PU-READ}^1$ | Power-up to Read Operation | 100 | μs |
| $T_{PU-WRITE}^1$ | Power-up to Write Operation | 100 | μs |

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7: Capacitance ($T_A = 25^\circ C$, $f=1 \text{ Mhz}$, other pins open)

| Parameter | Description | Test Condition | Maximum |
|-------------|---------------------|----------------|---------|
| $C_{I/O}^1$ | I/O Pin Capacitance | $V_{I/O} = 0V$ | 12 pF |
| C_{IN}^1 | Input Capacitance | $V_{IN} = 0V$ | 6 pF |

T7.0 1151

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: Reliability Characteristics

| Symbol | Parameter | Minimum Specification | Units | Test Method |
|-------------|----------------|-----------------------|--------|---------------------|
| N_{END}^1 | Endurance | 10,000 | Cycles | JEDEC Standard A117 |
| T_{DR}^1 | Data Retention | 100 | Years | JEDEC Standard A103 |
| I_{LTH}^1 | Latch Up | $100 + I_{DD}$ | mA | JEDEC Standard 78 |

T8.3 1151

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



AC CHARACTERISTICS

TABLE 9: Read Cycle Timing Parameters $V_{DD} = 2.7-3.6V$ ($T_A = 0^\circ C$ to $+70^\circ C$ (Commercial))

| Symbol | Parameter | SST37VF512-70 SST37VF010-70 SST37VF020-70 SST37VF040-70 | | Units |
|-------------|---------------------------------|--|-----|-------|
| | | Min | Max | |
| T_{RC} | Read Cycle Time | 70 | | ns |
| T_{CE} | Chip Enable Access Time | | 70 | ns |
| T_{AA} | Address Access Time | | 70 | ns |
| T_{OE} | Output Enable Access Time | | 35 | ns |
| T_{CLZ}^1 | CE# Low to Active Output | 0 | | ns |
| T_{OLZ}^1 | OE# Low to Active Output | 0 | | ns |
| T_{CHZ}^1 | CE# High to High-Z Output | | 25 | ns |
| T_{OHZ}^1 | OE# High to High-Z Output | | 25 | ns |
| T_{OH}^1 | Output Hold from Address Change | 0 | | ns |

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10: Program/Erase Cycle Timing Parameters $V_{DD} = 2.7-3.6V$ ($T_A = 25^\circ C \pm 5^\circ C$)

| Symbol | Parameter | Min | Max | Units |
|-----------|--|-----|-----|---------|
| T_{BP} | Byte-Program Time | | 20 | μs |
| T_{CES} | CE# Setup Time | 1 | | μs |
| T_{CEH} | CE# Hold Time | 1 | | μs |
| T_{AS} | Address Setup Time | 1 | | μs |
| T_{AH} | Address Hold Time | 1 | | μs |
| T_{DS} | Data Setup Time | 1 | | μs |
| T_{DH} | Data Hold Time | 1 | | μs |
| T_{PRT} | OE# Rise Time for Program and Erase | 50 | | ns |
| T_{VPS} | OE# Setup Time for Program and Erase | 1 | | μs |
| T_{VPH} | OE# Hold Time for Program and Erase | 1 | | μs |
| T_{PW} | WE# Program Pulse Width | 15 | 25 | μs |
| T_{EW} | WE# Erase Pulse Width | 100 | 200 | ms |
| T_{VR} | OE#/A ₉ Recovery Time for Erase | 1 | | μs |
| T_{ART} | A ₉ Rise Time to 12V during Erase | 50 | | ns |
| T_{A9S} | A ₉ Setup Time during Erase | 1 | | μs |
| T_{A9H} | A ₉ Hold Time during Erase | 1 | | μs |

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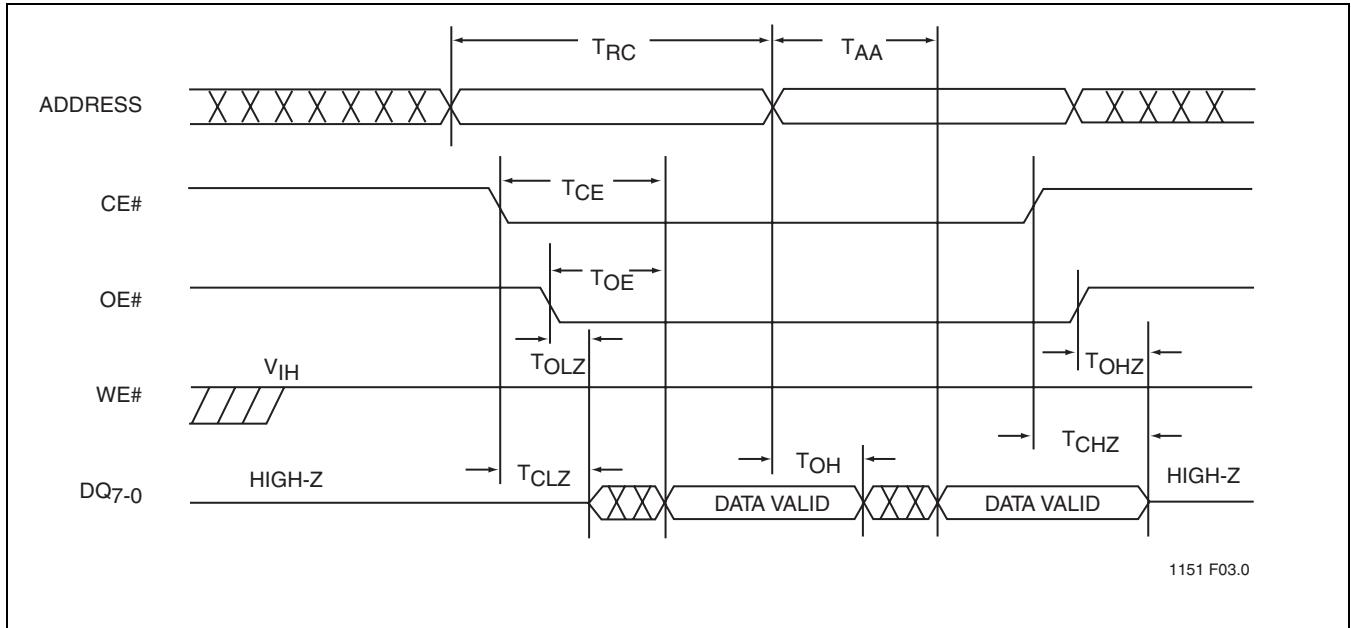


FIGURE 5: Read Cycle Timing Diagram

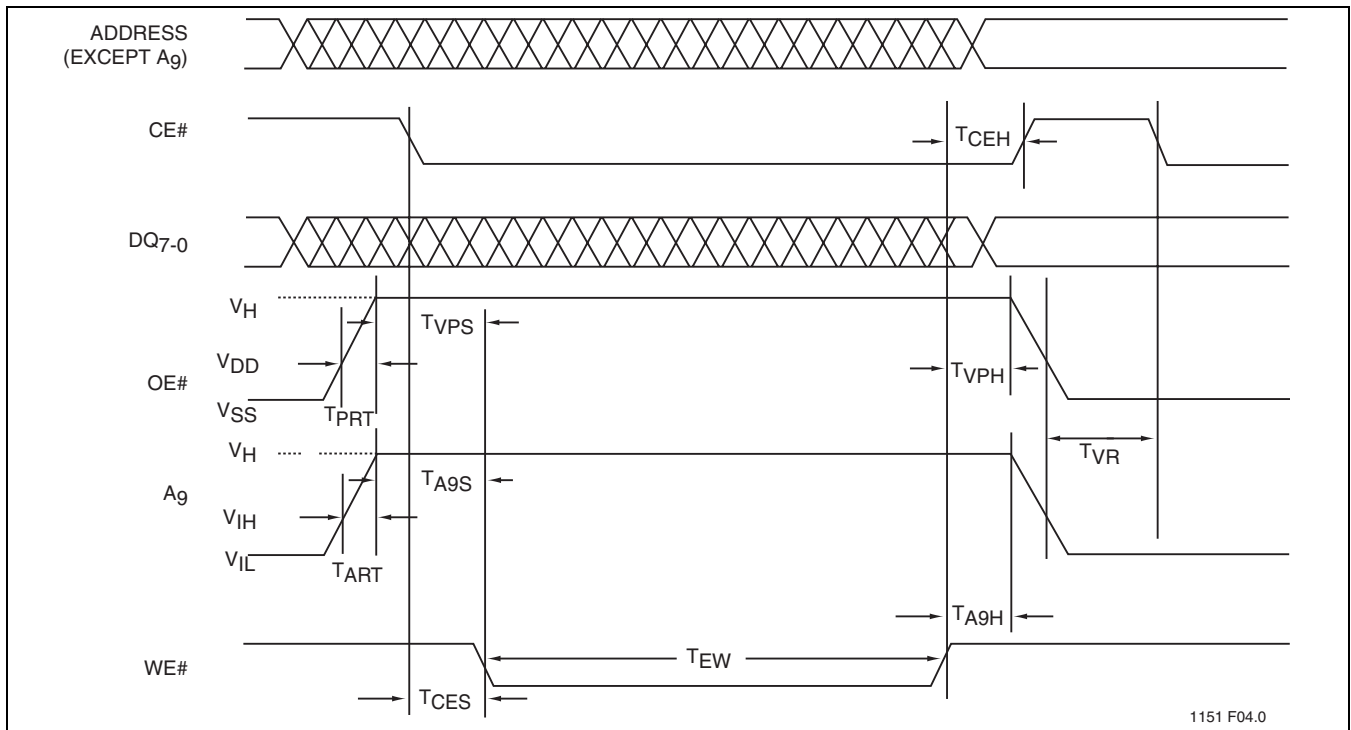


FIGURE 6: Chip-Erase Timing Diagram

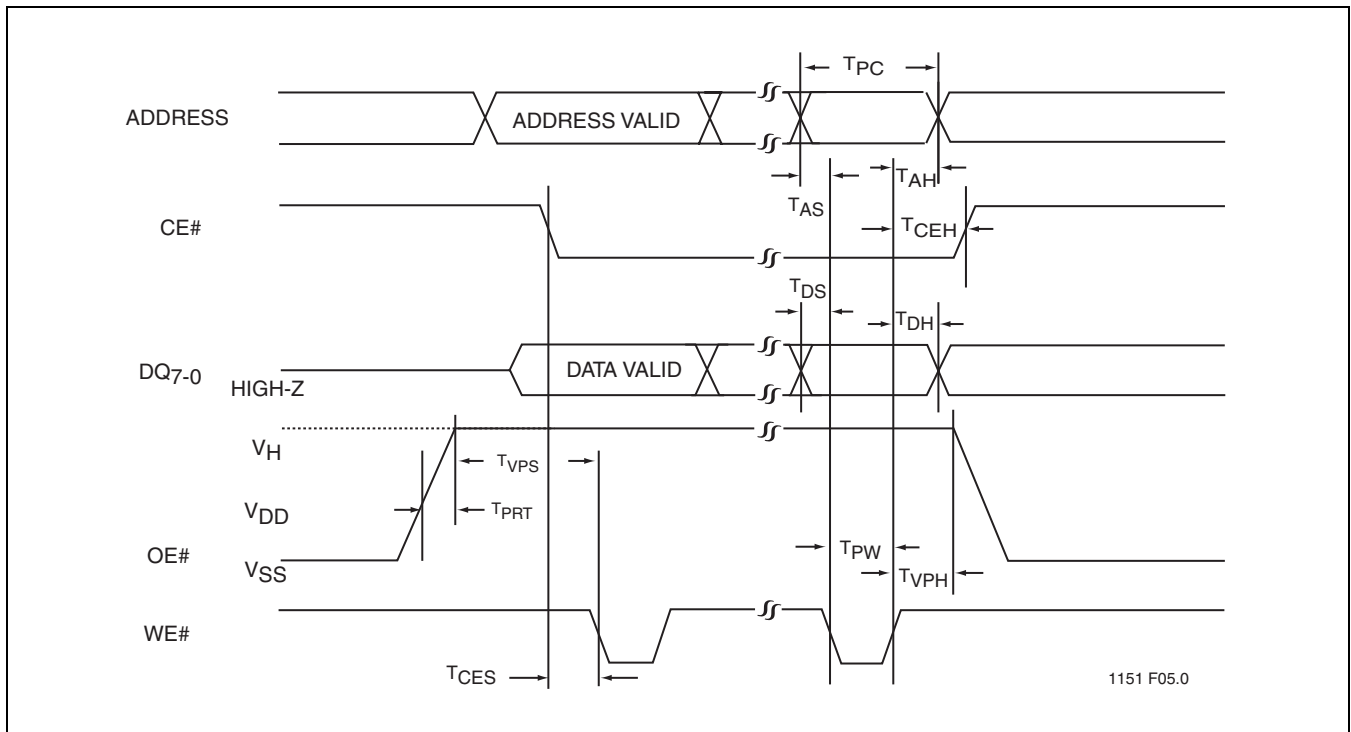
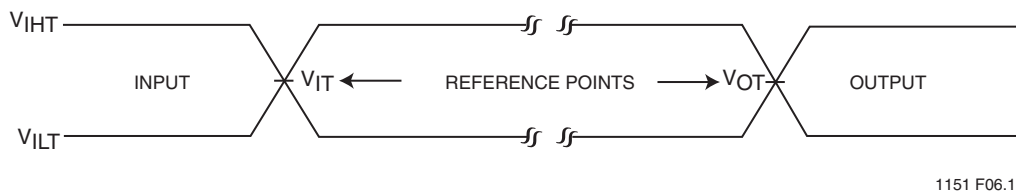


FIGURE 7: Byte-Program Timing Diagram



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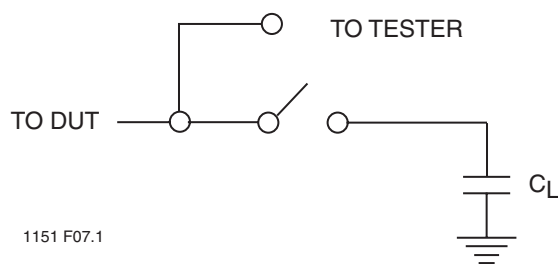


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AC test inputs are driven at V_{IHT} ($0.9 V_{DD}$) for a logic "1" and V_{ILT} ($0.1 V_{DD}$) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} ($0.5 V$) and V_{OT} ($0.5 V_{DD}$). Input rise and fall times ($10\% \leftrightarrow 90\%$) are $<5 ns$.

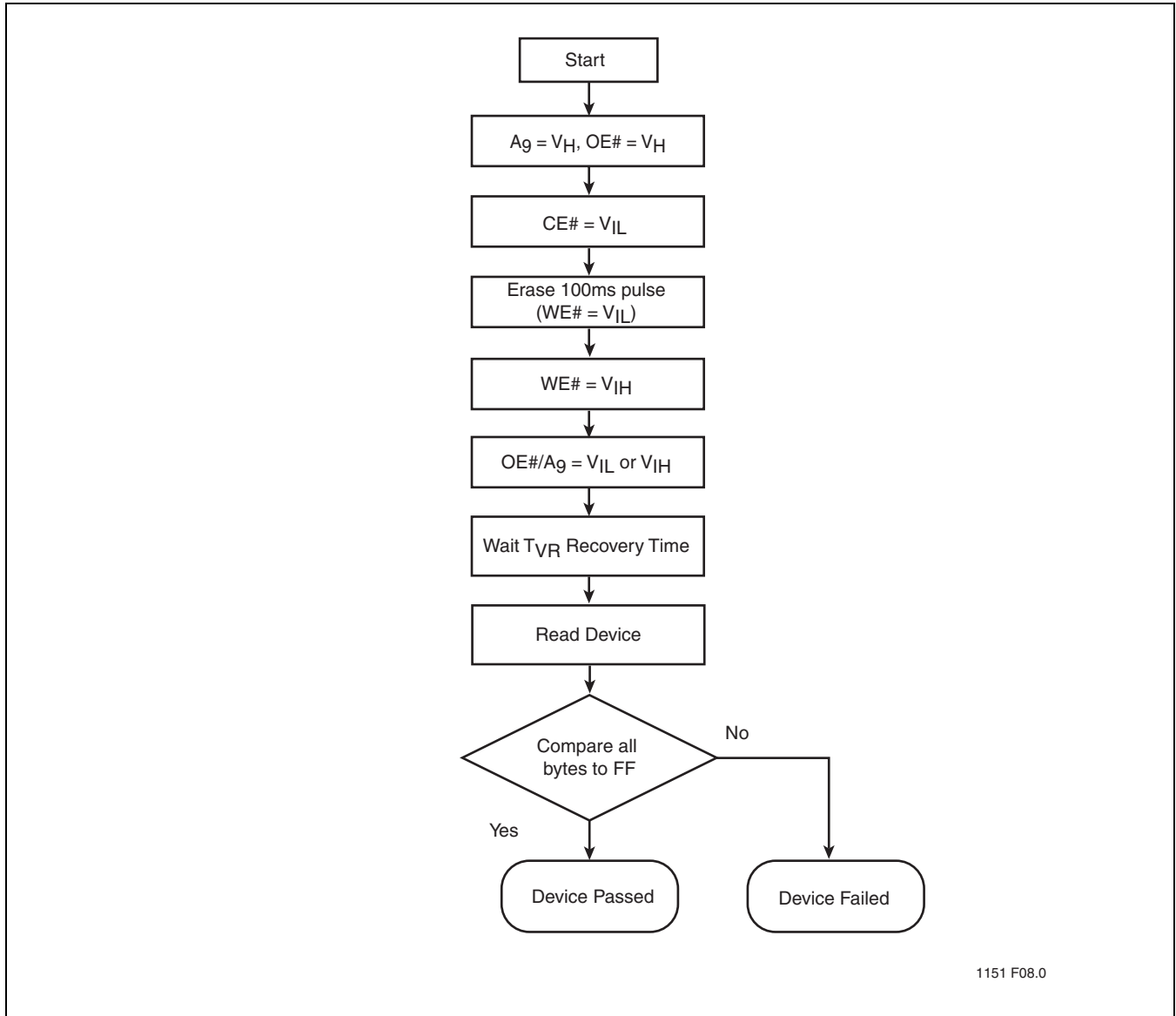
Note: V_{IT} - V_{INPUT} Test
 V_{OT} - V_{OUTPUT} Test
 V_{IHT} - V_{INPUT} HIGH Test
 V_{ILT} - V_{INPUT} LOW Test

FIGURE 8: AC Input/Output Reference Waveforms



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FIGURE 9: A Test Load Example



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FIGURE 10: Chip-Erase Algorithm



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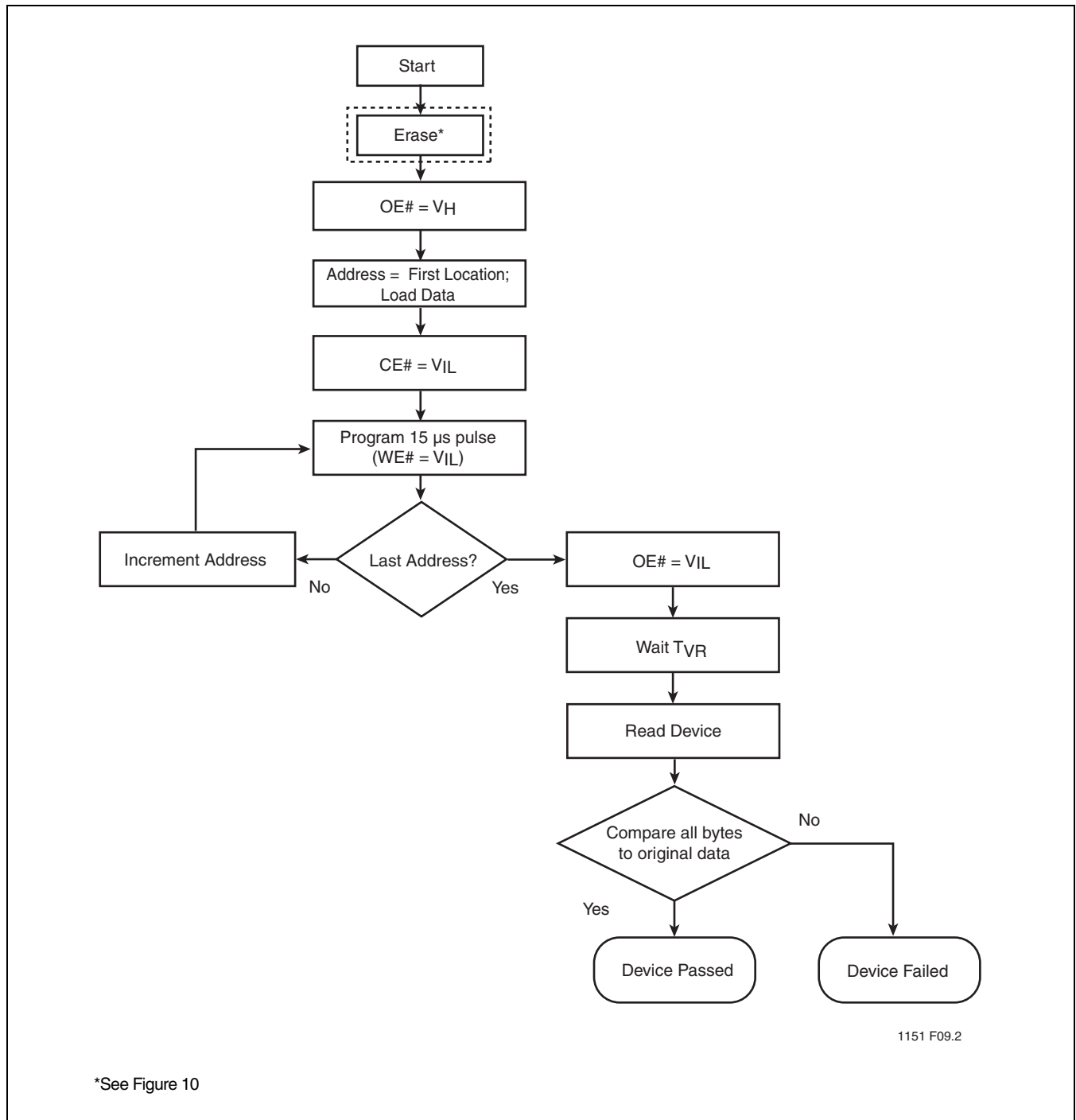


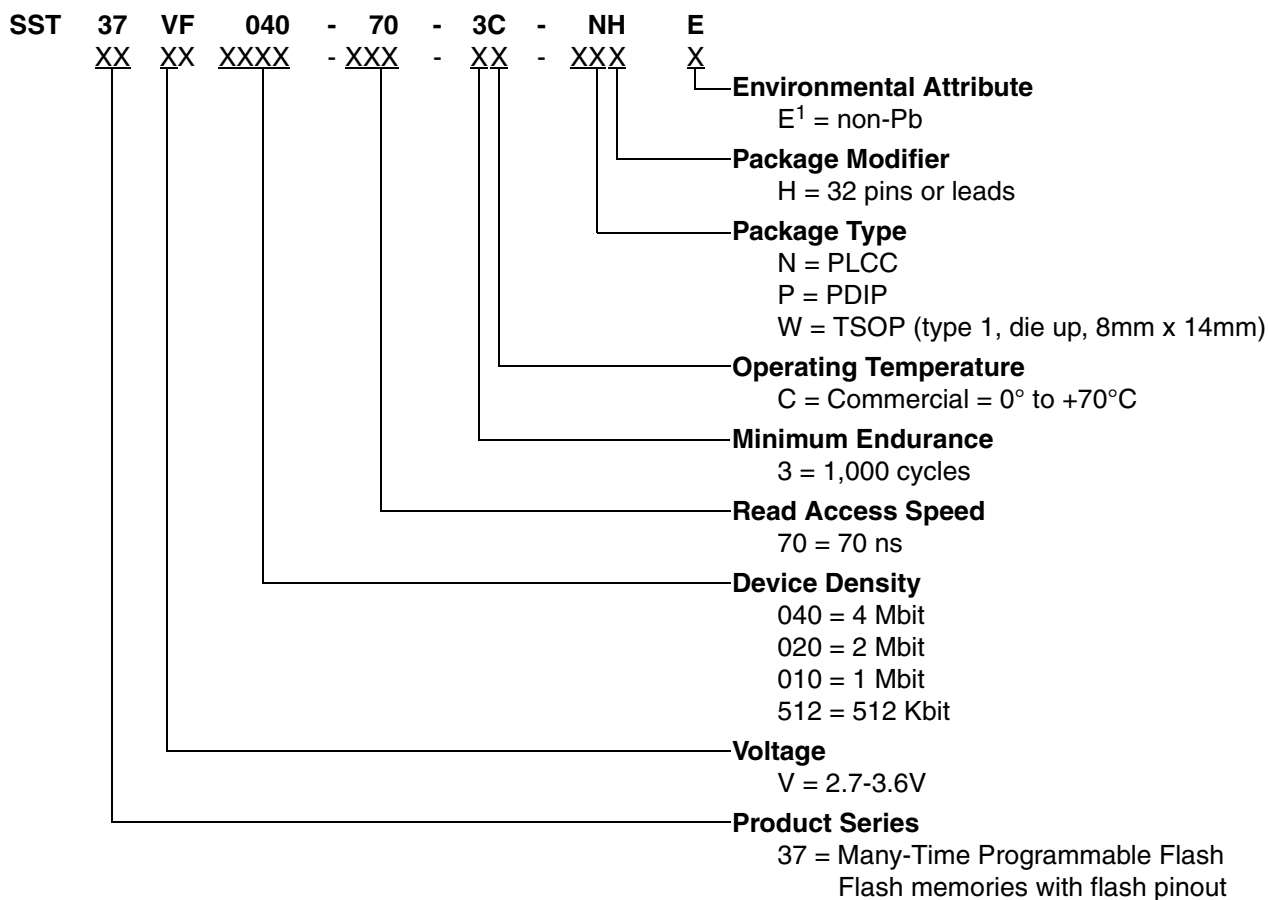
FIGURE 11: Byte-Program Algorithm

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PRODUCT ORDERING INFORMATION



1. Environmental suffix "E" denotes non-Pb solder.
 SST non-Pb solder devices are "RoHS Compliant".



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Valid combinations for SST37VF512

SST37VF512-70-3C-NH* SST37VF512-70-3C-WH* SST37VF512-70-3C-PH*
SST37VF512-70-3C-NHE* SST37VF512-70-3C-WHE*

Valid combinations for SST37VF010

SST37VF010-70-3C-NH SST37VF010-70-3C-WH SST37VF010-70-3C-PH
SST37VF010-70-3C-NHE SST37VF010-70-3C-WHE SST37VF010-70-3C-PHE

Valid combinations for SST37VF020

SST37VF020-70-3C-NH SST37VF020-70-3C-WH SST37VF020-70-3C-PH
SST37VF020-70-3C-NHE SST37VF020-70-3C-WHE SST37VF020-70-3C-PHE

Valid combinations for SST37VF040

SST37VF040-70-3C-NH SST37VF040-70-3C-WH SST37VF040-70-3C-PH
SST37VF040-70-3C-NHE SST37VF040-70-3C-WHE SST37VF040-70-3C-PHE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

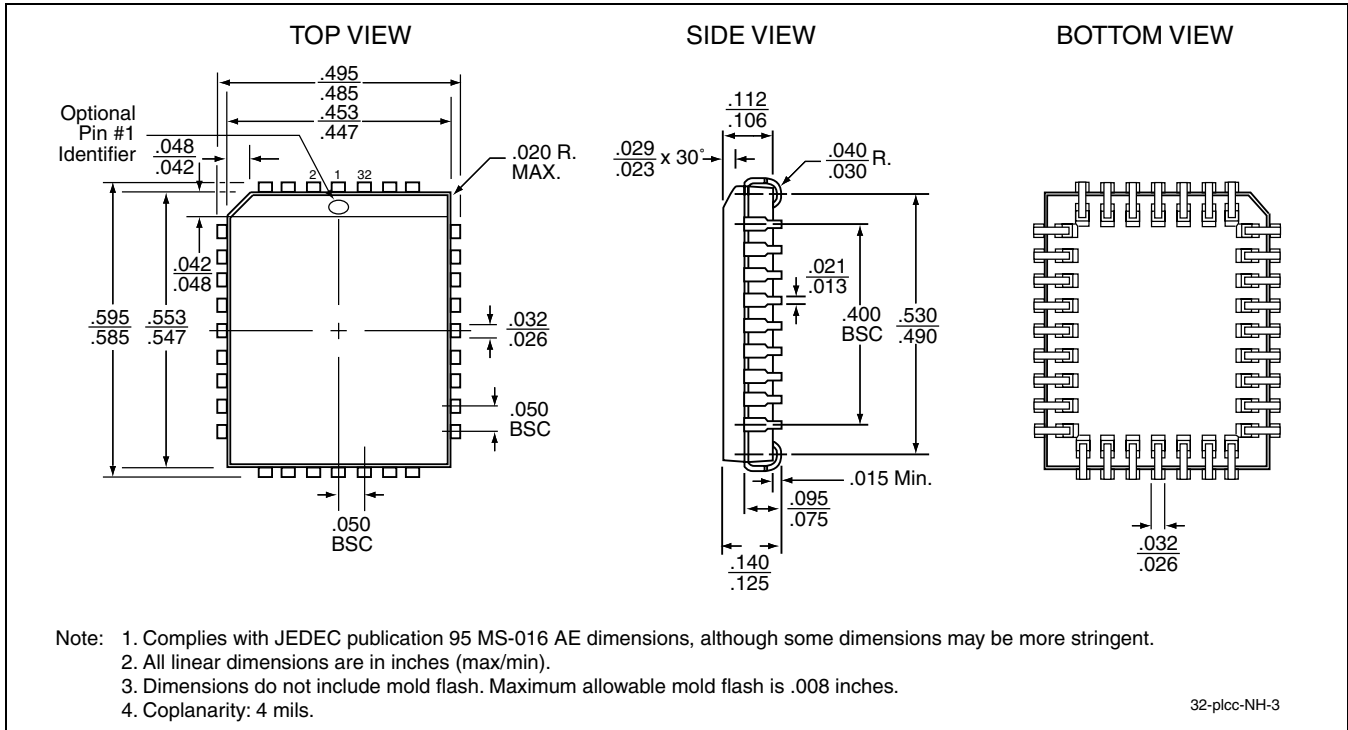
* Not recommended for new designs.

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PACKAGING DIAGRAMS

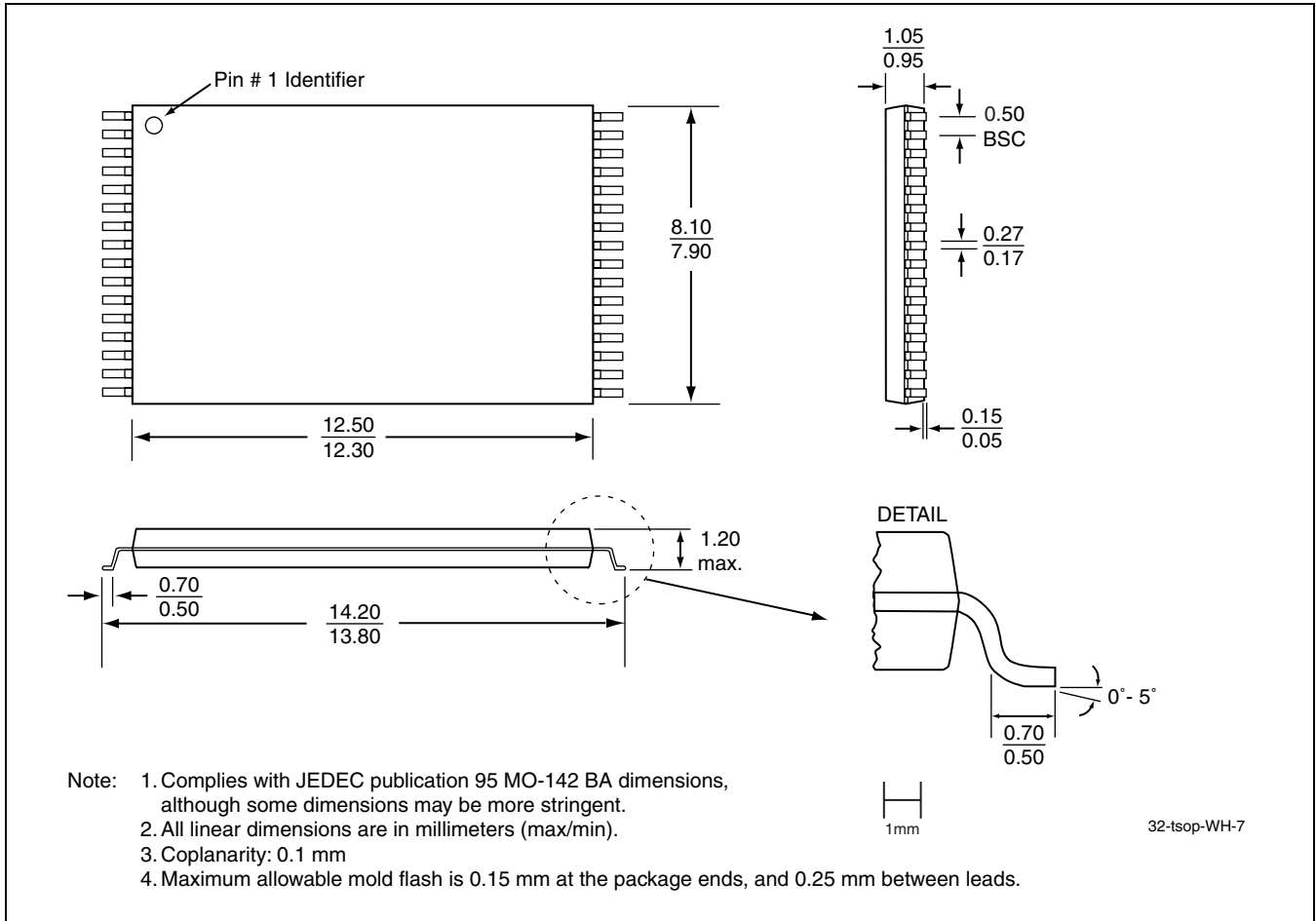


32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NH



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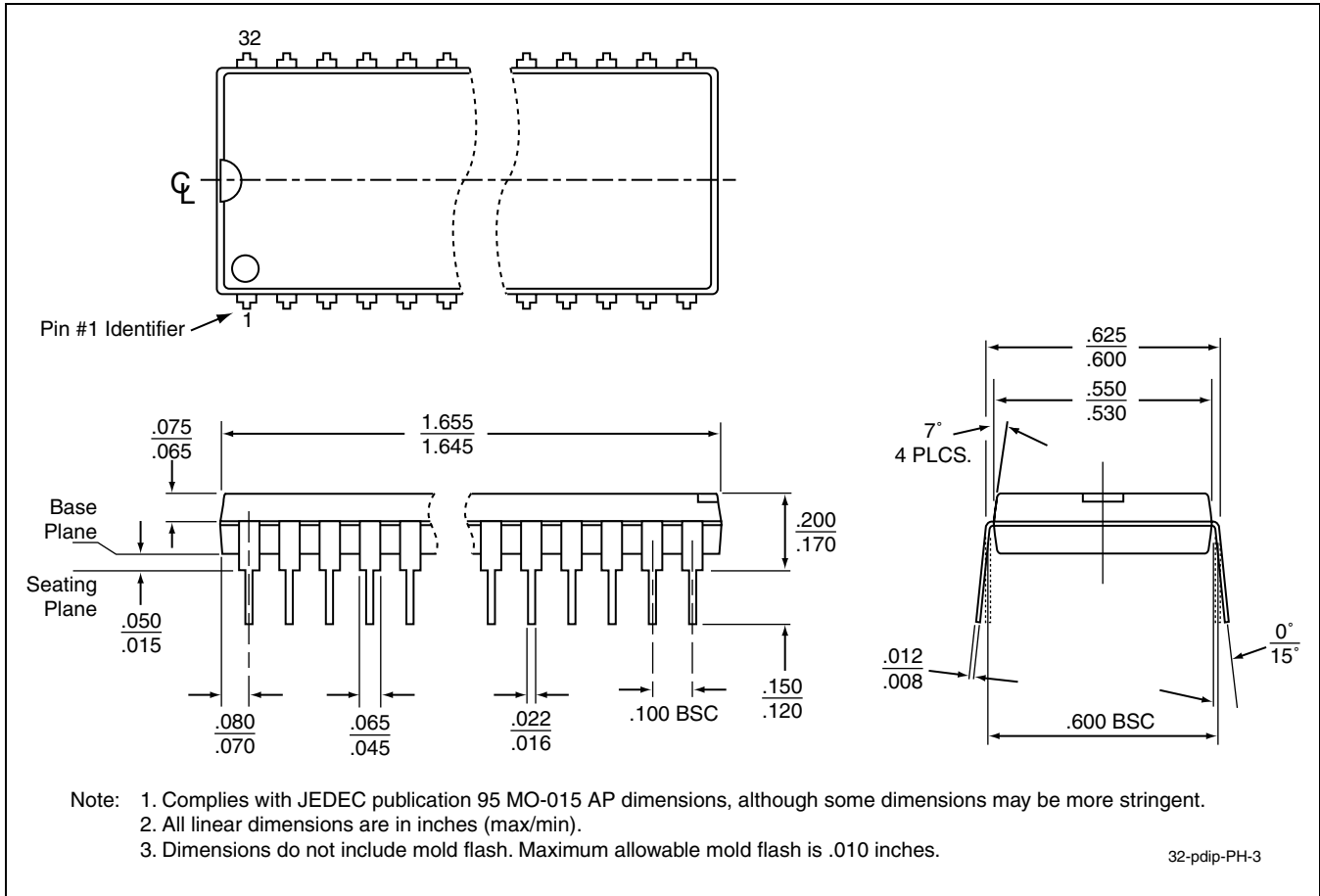


32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM
SST PACKAGE CODE: WH

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32-PIN PLASTIC DUAL IN-LINE PINS (PDIP)
SST PACKAGE CODE: PH



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TABLE 11: Revision History

| Number | Description | Date |
|--------|---|----------|
| 02 | <ul style="list-style-type: none">• 2002 Data Book | Feb 2002 |
| 03 | <ul style="list-style-type: none">• Part number changes - see page 14 for additional information• Clarified the Test Conditions for V_{DD} Read Current parameter in Table 4 on page 5<ul style="list-style-type: none">– Address input = V_{ILT}/V_{IHT}– $CE\#=OE\#=V_{ILT}$ | Mar 2003 |
| 04 | <ul style="list-style-type: none">• 2004 Data Book• Added non-Pb MPNs and removed footnote (See page 14) | Nov 2003 |
| 05 | <ul style="list-style-type: none">• Removed 90 ns parts, related footnote, and MPNs (See page 14)• Added 70 ns parts and MPNs for the PH package• Changed Byte-Program time from 10 μs to 15 μs• Updated chip program times• Separated Supervoltage Current for A_9 and $OE\#$ in Table 5 on page 6 | May 2004 |
| 06 | <ul style="list-style-type: none">• Added non-Pb 32-PDIP MPNs for 1, 2, and 4 Mbit devices• Clarified the solder temperature profile under “Absolute Maximum Stress Ratings” on page 5 | Dec 2004 |
| 07 | <ul style="list-style-type: none">• Changed program voltage from 12.6V to 12V globally | Aug 2006 |