

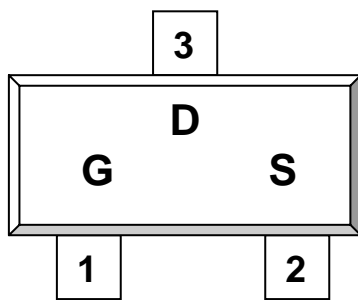
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DESCRIPTION

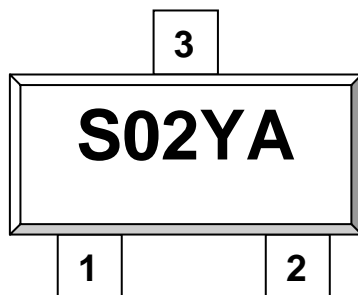
The ST2302 is the N-Channel logic enhancement mode power field effect transistor are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other batter powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

**PIN CONFIGURATION
SOT-23-3L**

1.Gate 2.Source 3.Drain



S: Subcontractor Y: Year Code A: Process Code

FEATURE

- 20V/3.6A, $R_{DS(ON)} = 80\text{m-ohm}$
@VGS = 4.5V
- 20V/2.4A, $R_{DS(ON)} = 95\text{m-ohm}$
@VGS = 2.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design

**STANSON TECHNOLOGY**

120 Bentley Square, Mountain View, Ca 94040 USA
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N Channel Enhancement Mode MOSFET ST2302

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ABSOLUTE MAXIMUM RATINGS (Ta = 25 Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	20	V
Gate-Source Voltage	V _{GSS}	+/-12	V
Continuous Drain Current (T _J =150)	I _D	T _A =25	A
		T _A =70	2.2
Pulsed Drain Current	I _{DM}	10	A
Continuous Source Current (Diode Conduction)	I _S	1.6	A
Power Dissipation	P _D	T _A =25	W
		T _A =70	0.8
Operation Junction Temperature	T _J	150	
Storage Temperature Range	T _{STG}	-55/150	
Thermal Resistance-Junction to Ambient	R _{JA}	100	/W

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ELECTRICAL CHARACTERISTICS (Ta = 25 Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=10\mu A$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=50\mu A$	0.45		1.2	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=8V$			100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$			1	uA
		$V_{DS}=20V, V_{GS}=0V$ $T_J=55$			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} = 5V, V_{GS}=4.5V$	6			A
		$V_{DS} = 5V, V_{GS}=2.5V$	4			
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=3.6A$		0.05	0.08	
		$V_{GS}=2.5V, I_D=3.1A$		0.07	0.095	
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=3.6V$		10		S
Diode Forward Voltage	V_{SD}	$I_S=-1.6A, V_{GS}=0V$		0.85	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=10V, V_{GS}=4.5V$ $I_D = -3.6A$		5.4	10	nC
Gate-Source Charge	Q_{gs}			0.65		
Gate-Drain Charge	Q_{gd}			1.4		
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V$ $F=1MHz$		340		pF
Output Capacitance	C_{oss}			115		
Reverse Transfer Capacitance	C_{rss}			33		
Turn-On Time	$t_{d(on)}$	$V_{DD}=10V, R_L=5.5$ $I_D=3.6A, V_{GEN}=4.5V$ $R_G=6$		12	25	nS
	t_r			36	60	
Turn-Off Time	$t_{d(off)}$			34	60	
	t_f			10	25	



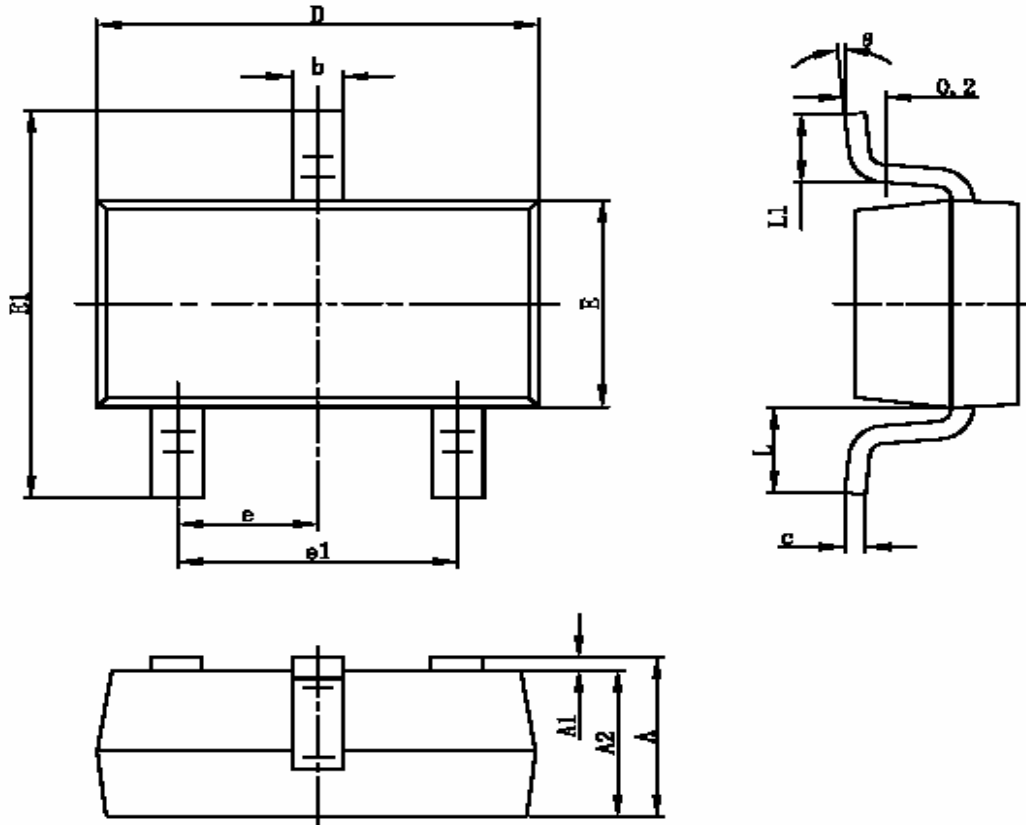
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SOT-23-3L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
theta	0°	8°	0°	8°



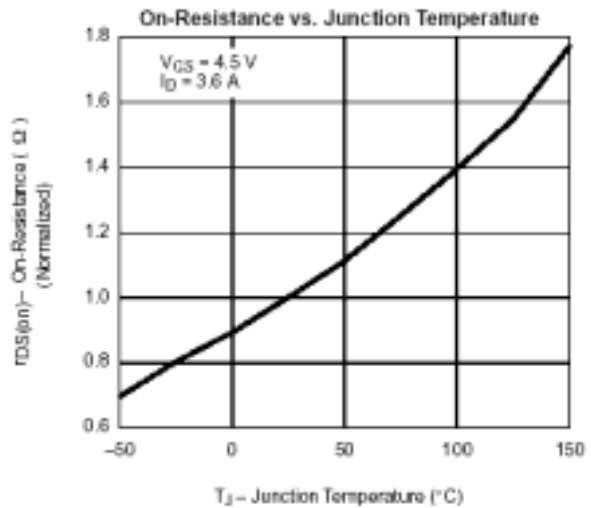
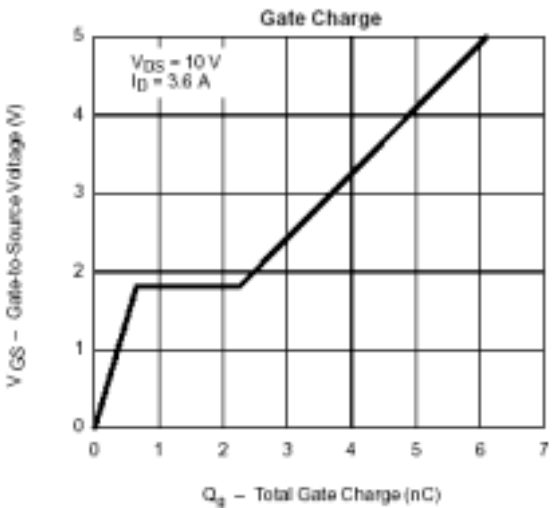
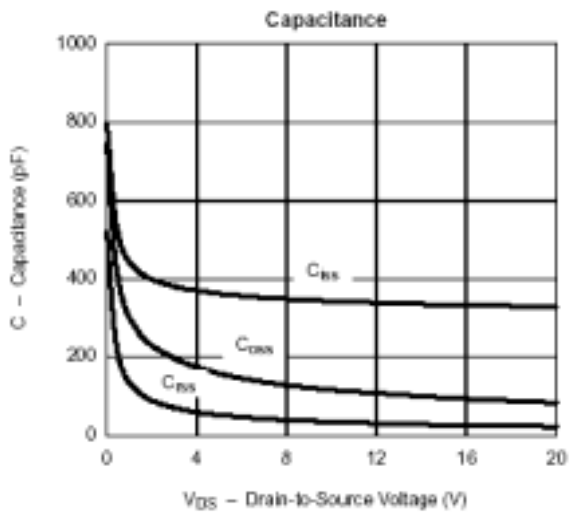
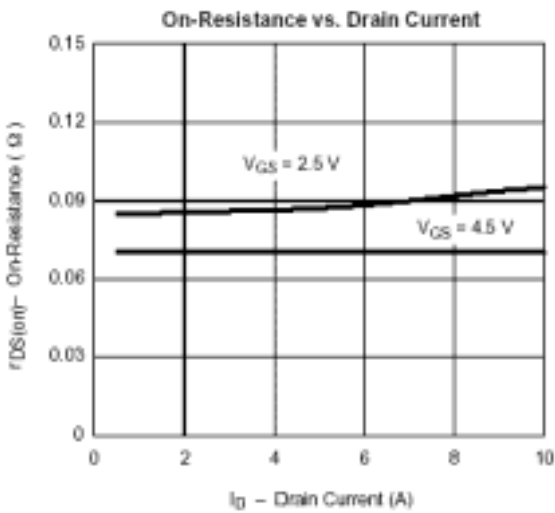
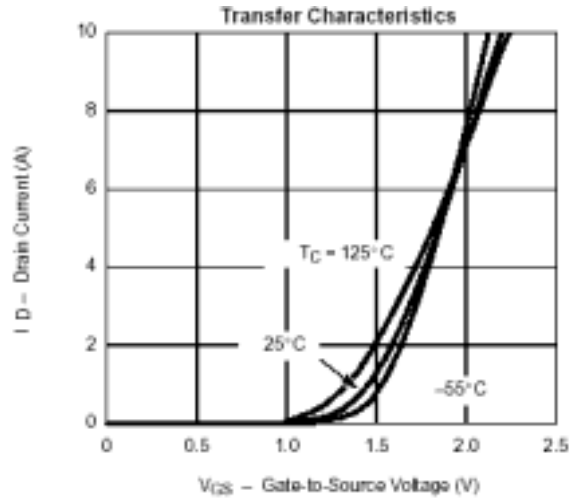
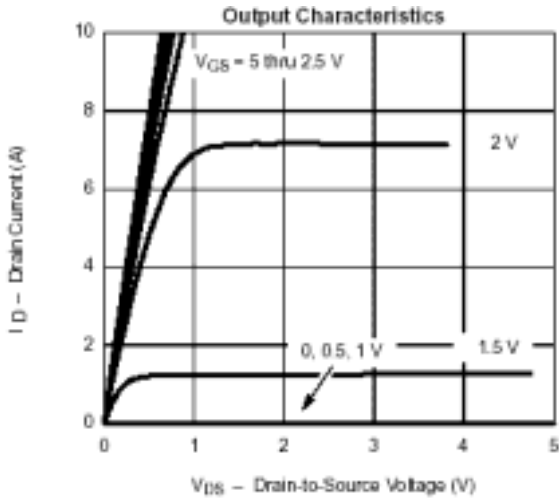
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TYPICAL CHARACTERISTICS



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