

Sitronix

ST7065C

40CH Segment/Common Driver for Dot Matrix LCD

■ Functions:

- Dot matrix LCD driver with two 20 channel outputs
- Selectable function to use common/segment drivers simultaneously
- Bias voltage (V1 ~ V6)
- Input/output signals
 - Input : Serial display data and control pulse from controller IC
 - Output : 20 X 2 channels waveform for LCD driving

■ Features:

- Display driving bias : static to 1/5
- Power supply for logic : 2.7V ~ 5.5V
- Power supply for LCD voltage ($V_{DD} \sim V_{EE}$) : 3V ~ 11V
- 64 Pin QFP package and bare chip available

■ Description:

ST7065C is a segment/common driver for dot matrix type LCD display. It features 40 channels with 20 X 2 bits bi-directional shift registers, data latches, LCD drivers and logic control circuits. It is fabricated by high voltage CMOS process with low current consumption.

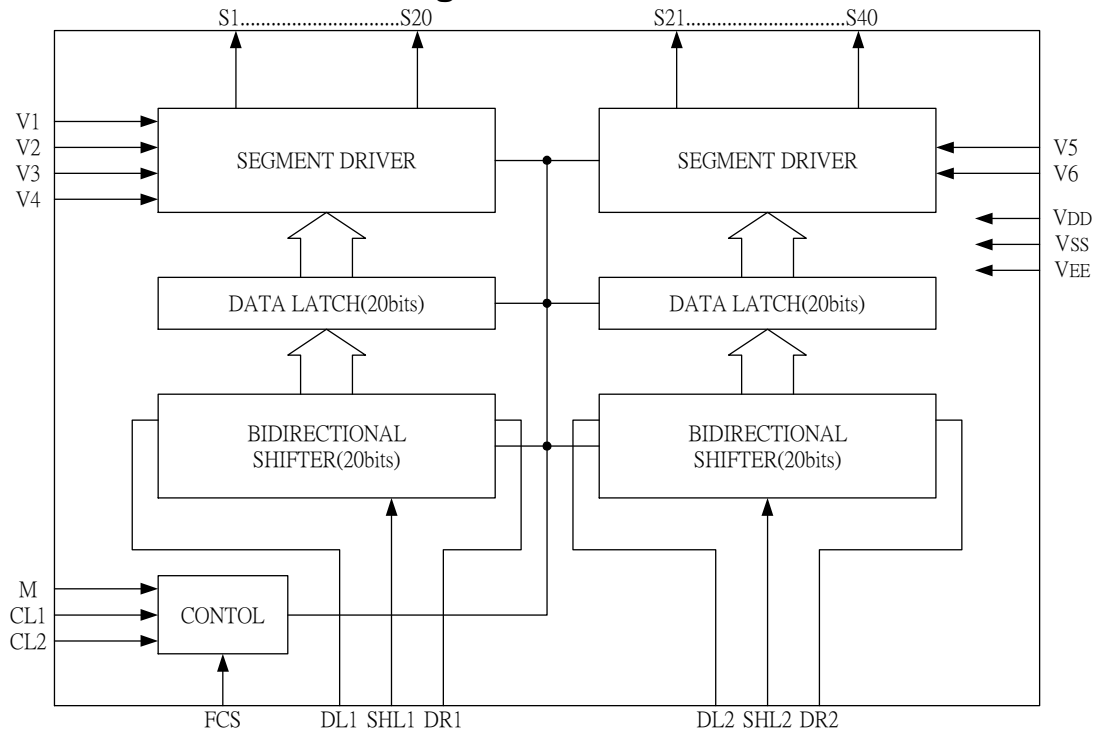
The **ST7065C** can convert serial data received from a LCD controller, such as **ST7066U**, into

parallel data and send out LCD driving waveforms to the LCD panel. The **ST7065C** is designed for general-purpose LCD drivers. It can drive both static and dynamic drive LCD. The LSI can be used as segment/common driver.

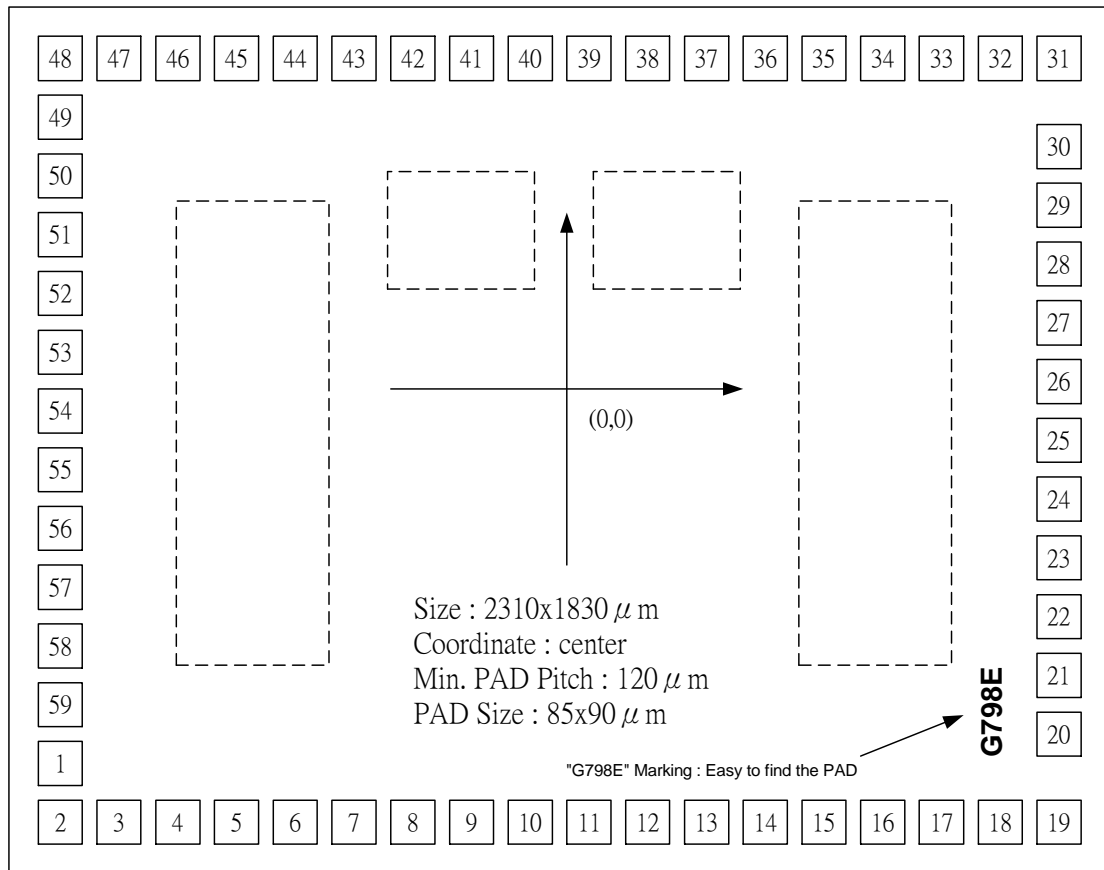
The **ST7065C** has pin function compatibility with the KS0065B that allows the user easily to replace it with a **ST7065C**.

ST7065C Specification Revision History		
Version	Date	Description
1.1	2000/07/31	First Edition
1.2	2000/11/14	Added QFP Pad Configuration(Page 4)
1.3	2001/04/18	Moved QFP Package Dimensions(Page 13) to Page 4 Change Shift Register Table(Page 8)
1.4	2001/05/04	ST7065 Transition to ST7065C
1.4a	2001/08/29	Added “Substrate connect to VDD”(Page 3)
1.4b	2007/08/17	Modify Temperature Range
1.4c	2009/08/21	Added COM/SEG Application Circuit(Page11)

■ Functional Block Diagram



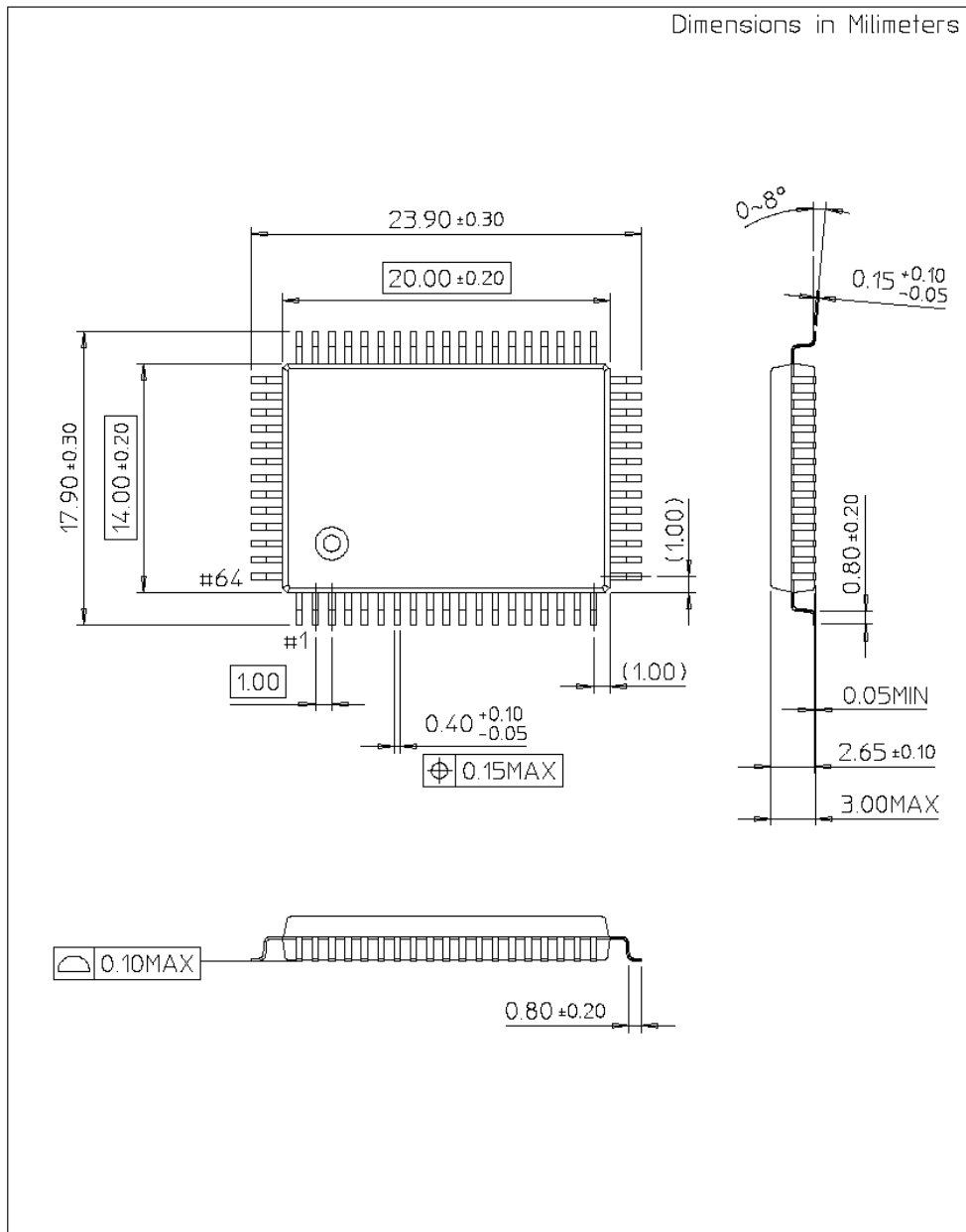
■ Pad Arrangement



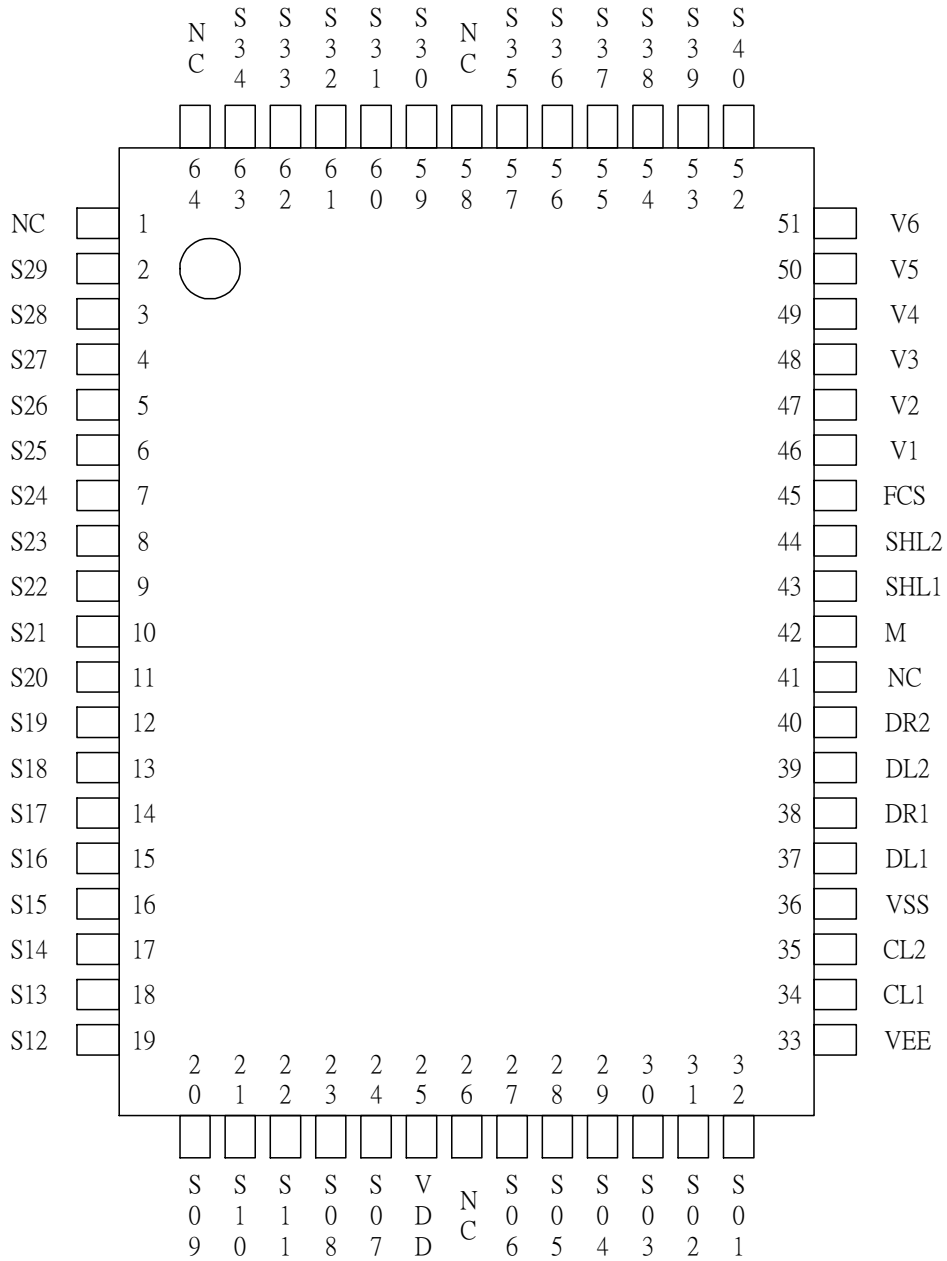
Substrate connect to VDD.

■ Package Dimensions

64-QFP-1420F



■ Pad Configuration(QFP 64)



■ Pad Name and Coordinates

Pad No.	Pad Name	X	Y
1	VEE	-1045	-670
2	CL1	-1040	-805
3	CL2	-910	-805
4	VSS	-780	-805
5	DL1	-660	-805
6	DR1	-540	-805
7	DL2	-420	-805
8	DR2	-300	-805
9	M	-180	-805
10	SHL1	-60	-805
11	SHL2	60	-805
12	FCS	180	-805
13	V1	300	-805
14	V2	420	-805
15	V3	540	-805
16	V4	660	-805
17	V5	780	-805
18	V6	910	-805
19	S[40]	1040	-800
20	S[39]	1045	-623
21	S[38]	1045	-488
22	S[37]	1045	-358
23	S[36]	1045	-233
24	S[35]	1045	-108
25	S[30]	1045	20
26	S[31]	1045	145
27	S[32]	1045	270
28	S[33]	1045	395
29	S[34]	1045	525
30	S[29]	1045	655

Pad No.	Pad Name	X	Y
31	S[28]	1040	800
32	S[27]	910	805
33	S[26]	780	805
34	S[25]	660	805
35	S[24]	540	805
36	S[23]	420	805
37	S[22]	300	805
38	S[21]	180	805
39	S[20]	60	805
40	S[19]	-60	805
41	S[18]	-180	805
42	S[17]	-300	805
43	S[16]	-420	805
44	S[15]	-540	805
45	S[14]	-660	805
46	S[13]	-780	805
47	S[12]	-910	805
48	S[9]	-1040	800
49	S[10]	-1045	670
50	S[11]	-1045	540
51	S[8]	-1045	420
52	S[7]	-1045	300
53	VDD	-1045	180
54	S[6]	-1045	60
55	S[5]	-1045	-60
56	S[4]	-1045	-180
57	S[3]	-1045	-300
58	S[2]	-1045	-420
59	S[1]	-1045	-540

■ Pin Description:

Pin Name	Purpose	Description	I/O
VDD	POWER	for logic	N/A
VSS	GROUND	for logic	N/A
VEE	LCD GND	for LCD driving voltage	N/A
V1 V2	LCD output	used as select voltage level	I
V3 V4	LCD output	Used as non select voltage level for Part I	I
V5 V6	LCD output	Used as non select voltage level for Part II	I
S[1]-S[20]	segment	LCD driver output for part 1	O
SHL1	direction	direction control for part 1 segments	I
DL1, DR1	data in /out	If SHL1 = 1 then DL1=out, DR1=in If SHL1 = 0 then DL1=in, DR1=out	I/O
S[21]-S[40]	segment	LCD driver output for part 2	O
SHL2	direction	direction control for part 2 segments	I
DL2, DR2	data in/out	If SHL2 = 1 then DL2=out, DR2=in If SHL2 = 0 then DL2=in, DR2=out	I/O
M	alternation	Alternate the LCD driving waveform	I
CL1	latch clock	latch the data after shift is completed	I
CL2	shift clock	shift the data into the segments	I
FCS	mode selection	mode select signal for Part II	I

■ **Functional Description:**

Shift Registers and Data I/O

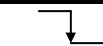
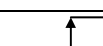
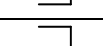
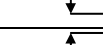
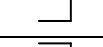
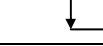
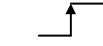
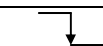
The **ST7065C** supplies two sets of shift register, which controls the shift direction by SHL1 & SHL2. The DL1, DR1, DL2 and DR2 are data input or output option function.

Shift Direction of Channel 1				Shift Direction of Channel 2			
SHL1	Shift Direction	DL1	DR1	SHL2	Shift Direction	DL2	DR2
0	S[1] → S[20]	IN	OUT	0	S[21] → S[40]	IN	OUT
1	S[20] → S[1]	OUT	IN	1	S[40] → S[21]	OUT	IN

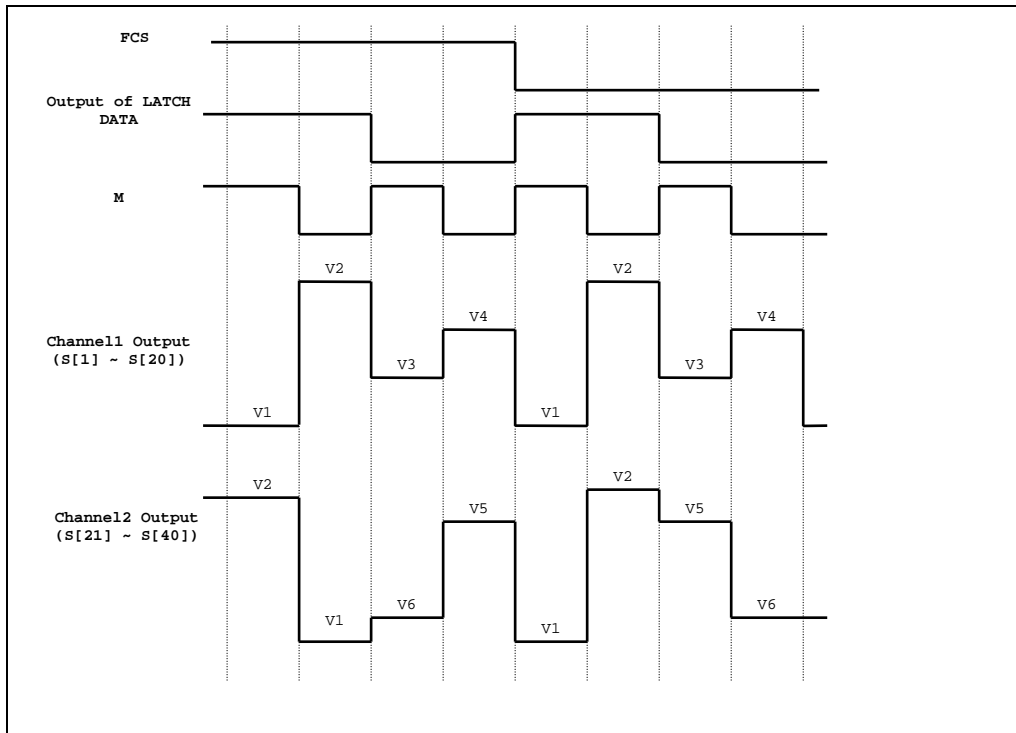
Clock and Mode Selection

In channel 1 part, the CL1 is the clock to latch data on the falling edge. It latches the data input from the bi-directional shift register at the falling edge of CL1 and transfers its outputs to the LCD driver circuit. The CL2 is the clock to shift data on the falling edge. It shifts the serial data at the falling of CL2 and transfers the output of each bit of the register to the latch circuit.

In channel 2 part, the CL1 and CL2 is the clock to latch or shift data on the falling or rising edge which is depend on FCS value. When FCS is low, the channel 2 function is the same as channel 1 as a segment driver. When FCS is high, the channel 2 function will become a common driver. Detail functions are show in the following table:

FCS		Clock Edge	Channel 1	Channel 2
0	CL1		Latch data	Latch Data
			----	----
	CL2		Shift data	Shift data
			----	----
1	CL1		Latch data	----
			----	Shift data
	CL2		Shift data	----
			----	Latch data

■ LCD Output Waveform



The output levels of channel1 and channel2 are decided by the combination of FCS, M, and latched data. Refer to the following table:

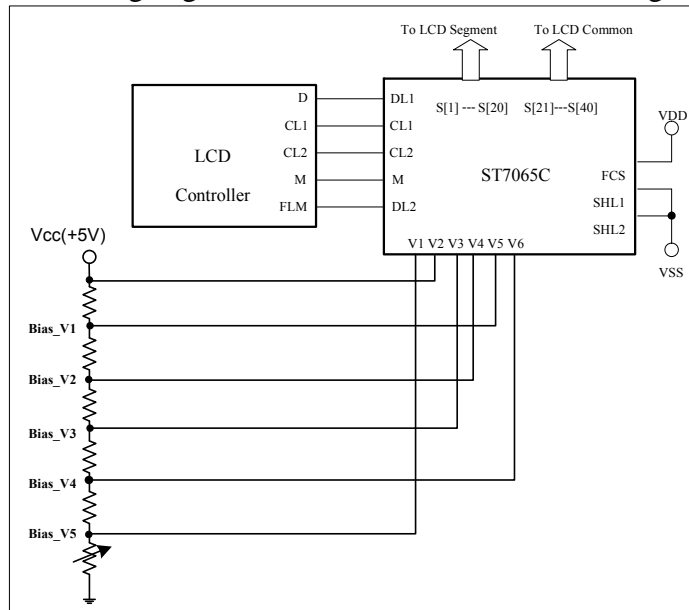
FCS	Latched Data	M	Channel 1	Channel 2
1	1	1	V1	V2
		0	V2	V1
	0	1	V3	V6
		0	V4	V5
0	1	1	V1	V1
		0	V2	V2
	0	1	V3	V5
		0	V4	V6

Note:

To use the same function of channel 1 and channel 2 as a segment driver, V3 and V5, V4 and V6 need to short respectively.

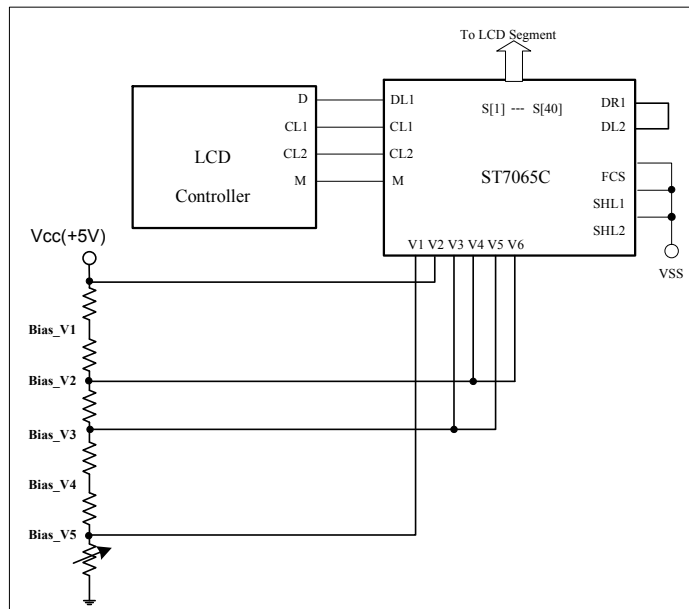
Channel 1 used as a segment driver and channel 2 as a common driver (FCS=1)

When channel 2 is used as a common driver, FCS is connected to VDD. Channel 2 will shift data on the rising edge of CL1 and latch data on the rising edge of CL2.



Both Channels 1 and 2 used as segment drivers (FCS=0)

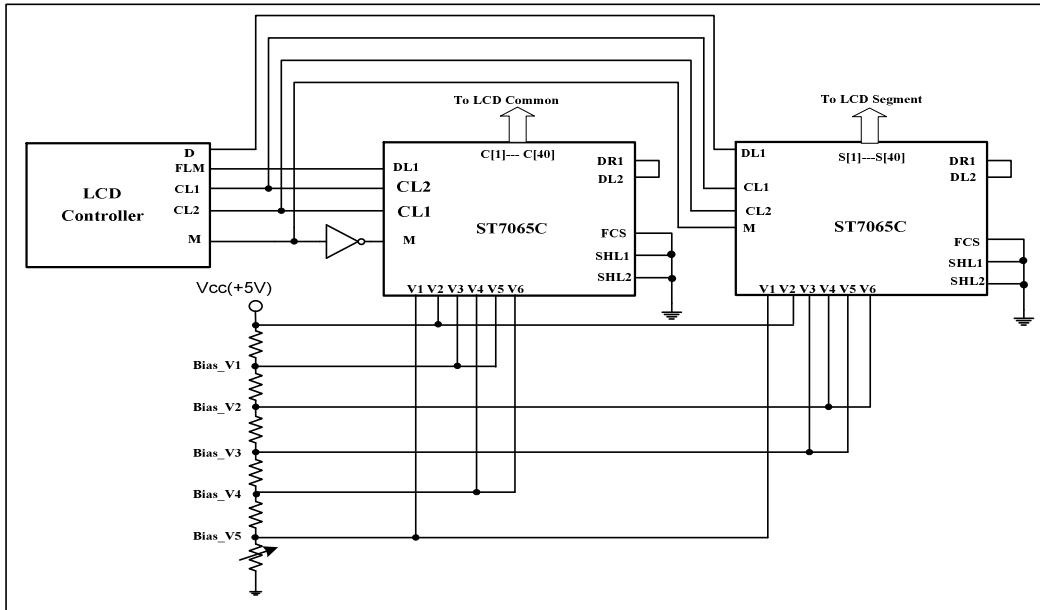
When both channels 1 and 2 of the **ST7065C** are used as segment drivers, they will shift data on the falling edge of CL2 and latch data on the falling edge of CL1. V3&V5, V4&V6 are shorted in the application circuit as shown in the following figure.



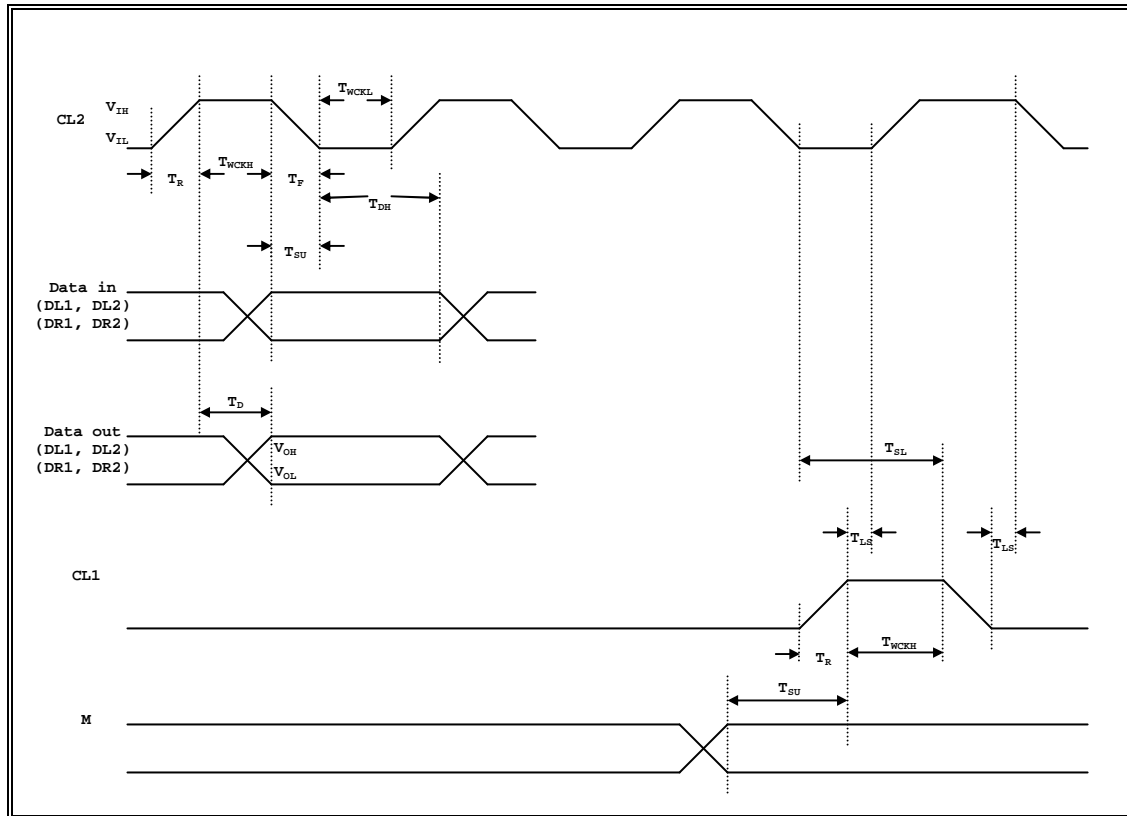
One ST7065C used as a common driver and the other ST7065C as a segment driver (FCS=0)

The **ST7065C** are used as common drivers, the FCS is set low and the signals (CL1, CL2, M) from the controller are connected. V3&V5, V4&V6 are shorted in the application circuit as shown in the following figure.

The other **ST7065C** are used as segment drivers, they will shift data on the falling edge of CL2 and latch data on the falling edge of CL1. V3&V5, V4&V6 are shorted in the application circuit as shown in the following figure.



■ Timing Characteristics



■ D.C Characteristics:

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Applicable pin
VDD	Operating Voltage	-	2.7	-	5.5	V	-
VLCD	Driver Supply Voltage	VDD-VEE	3	-	11	V	-
VIH	Input High Voltage	-	0.7 VDD	-	VDD	V	CL1,CL2,M,SHL1,S HL2 DL1,DL2,DR1,DR2
VIL	Input Low Voltage	-	0	-	0.3 VDD	V	
ILKG	Input Leakage Current	VIN = 0 ~ VDD	-5	-	5	uA	
VOH	Output High Voltage	IOH = -0.4mA	VDD -0.4	-	-	V	DL1,DL2,DR1,DR2 V1~V6, S[1]~S[40]
VOL	Output Low Voltage	IOL = +0.4mA	-	-	0.4	V	
IDD	Operating Current	FCL2 = 400KHZ	-	100	300	uA	VDD,VEE
IV	Leakage Current	VIN = VDD ~ VEE	-10	-	10	uA	V1 ~ V6

■ A.C Characteristics:

Symbol	Parameter	Test Condition	Min.	Max.	Unit	Applicable pin
FCL	Data Shift Frequency	-	-	400	KHZ	CL2
TWCKH	Clock High Level Width	-	800	-	ns	CL1,CL2
TWCKL	Clock Low Level Width	-	800	-	ns	CL2
TSL	Clock Set-up Time	CL2 → CL1	500	-	ns	CL1,CL2
TLS	Clock Set-up Time	CL1 → CL2	500	-	ns	CL1,CL2
TR/TF	Clock Rise/Fall Time	-	-	200	ns	CL1,CL2
TSU	Data Set-up Time	-	300	-	ns	DL1,DL2,DR1,DR2
TDH	Data Hold Time	-	300	-	ns	DL1,DL2,DR1,DR2
TD	Data Delay Time	CL = 15 PF	-	500	ns	DL1,DL2,DR1,DR2

■ Maximum Absolute Ratings:

Symbol	Parameters	Min.	Max.	Unit
VDD	Supply Voltage	-0.3	7	V
TOPR	Operating Temperature	-20	85	°C
TSTG	Storage Temperature	-55	125	°C

■ Application Circuit: (2Line x 24Word)

