# STA333ML

## Sound Terminal™
## 2 channel microless high efficiency digital audio system

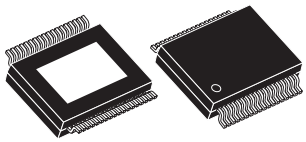
**Target Specification**

## Features

- Wide supply voltage range (4.5-18 V)
- 2 x 20 W @ 8 Ω, Vcc = 18 V
- 3 power output configurations; 2 channels of ternary PWM
- PowerSSO-36 exposed pad package
- 2 channels of 24-Bit DDX®
- 100 dB SNR and dynamic range
- 32 kHz to 48 kHz input sample rates
- Soft volume update
- Automatic zero-detect mute
- Automatic invalid input detect mute
- 2-channel $I^2S$ input data interface
- Selectable clock input ratio (256 / 364 Fs)
- Max power correction for lower full power
- 96 kHz internal processing sample rate, 24-bit precision
- Thermal overload and short-circuit protection embedded

## Applications

- LCD
- DVD
- Cradle
- Digital speaker
- Wireless speaker cradle



PowerSSO36 slug down

## Description

STA333ML is a single die embedding digital audio processing and high efficiency power amplification, capable of operating without the aid of an external micro controller.

The STA333ML is part of the Sound Terminal™ family that provides full digital audio streaming to the speaker offering cost effectiveness, low energy dissipation and sound enrichment.

The STA333ML combines a unique 24-bit DDX® digital Class-D ternary modulator together with an extremely low RDSON stereo power Dmos stage. The latter is capable of a total output power of 2 x 20 W with outstanding performances in terms of efficiency (>90 %), THD, SNR and EMI.

The microless feature allows the use in low cost applications (cradle, digital speakers, audio terminals) where no micro controller is needed.

The serial audio data interface accepts the world wide used $I^2S$ format; basic features (for example, oversampling clock, gain, $I^2S$ format) can be set using a minimal number of selection pins.

STA333ML is self-protected against thermal overload, overcurrent, short circuit and overvoltage conditions.

The fault condition is also exported to an external pin (INT-LINE) for specific requirements.

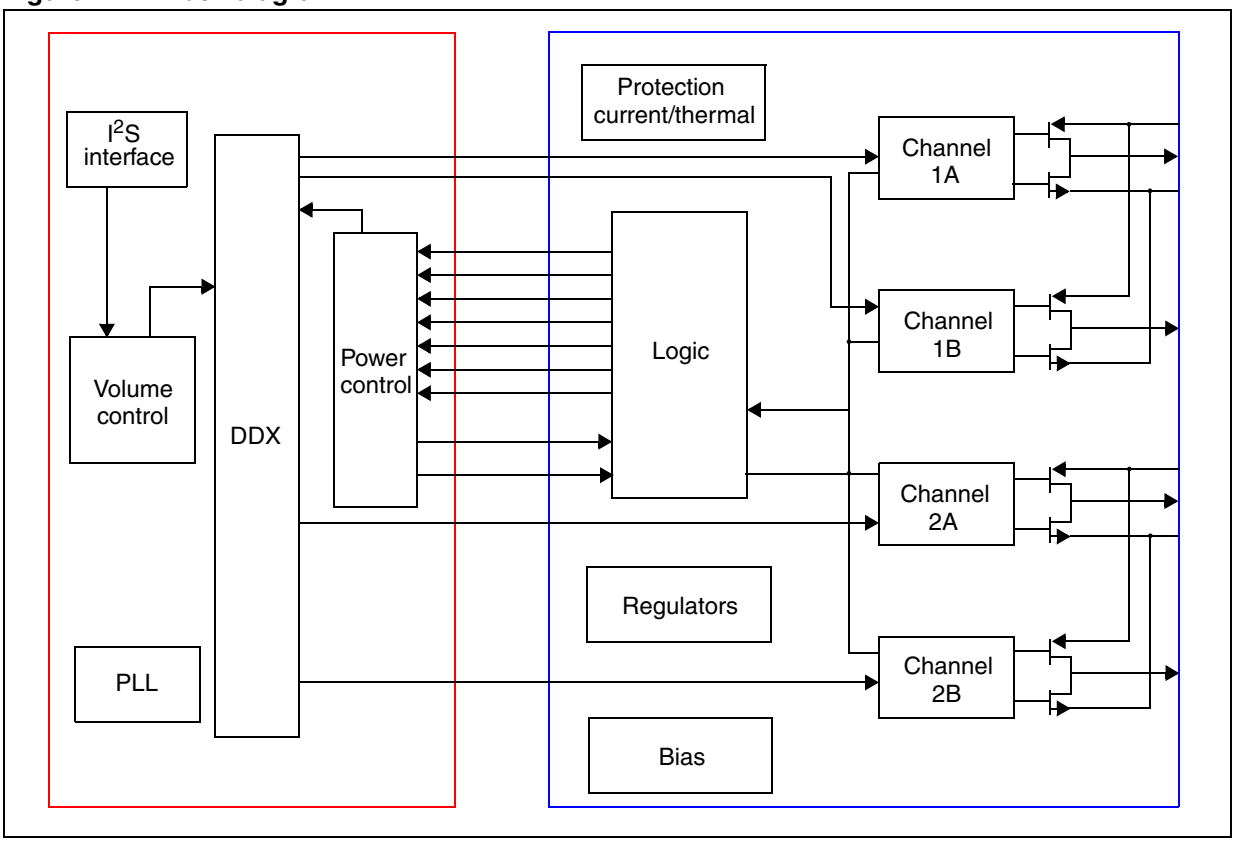
## Order codes

| Part number | Package | Packing |
|---|---|---|
| STA333ML | PowerSSO36 (slug down) | Tube |
| STA333ML13TR | PowerSSO36 (slug down) | Tape and reel |

# Contents

# 1 Block diagram

**Figure 1. Block diagram**



# 2 Pin description

**Figure 2. Pin connection (Top view)**

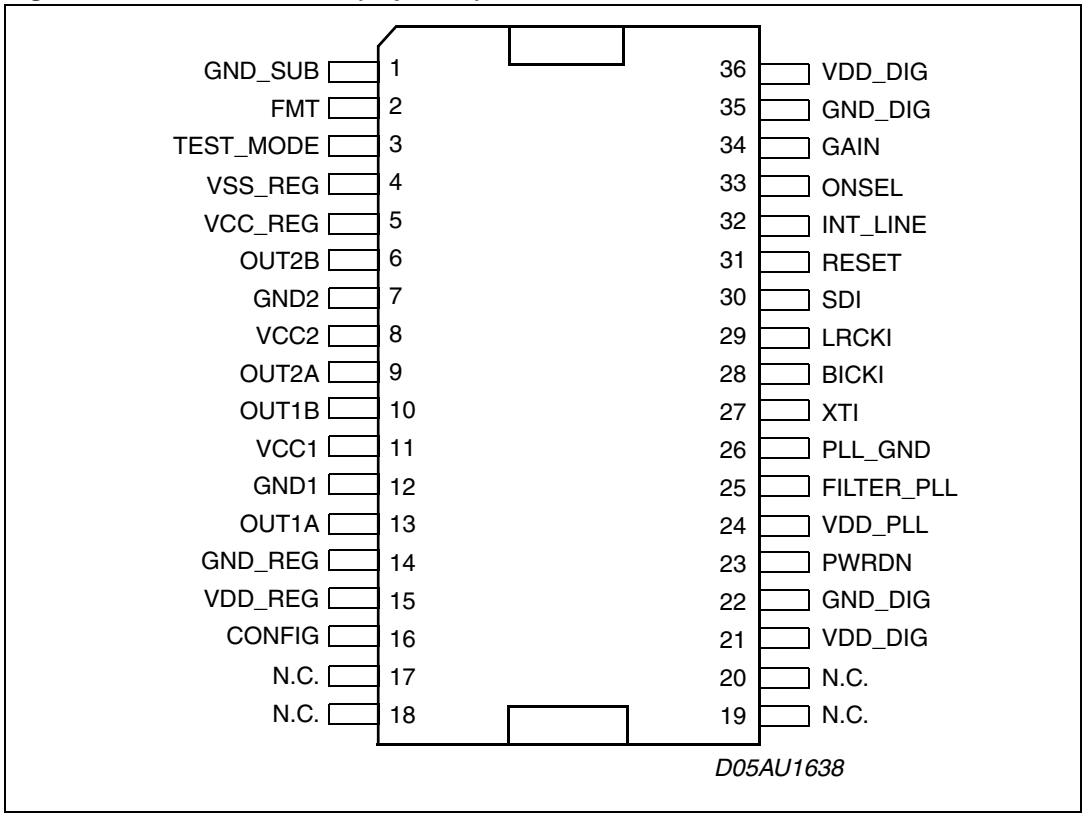



**Table 1. Pin description**

| Pin | Type | Name | Description |
|---|---|---|---|
| 1 | Gnd | GND_SUB | Substrate ground |
| 2 | I | FMT | 0: $I^2S$ format<br>1: left justified |
| 3 | I | TEST_MODE | This pin must be connected to GROUND |
| 4 | I/O | VSS | Internal reference at Vcc-3.3 V |
| 5 | I/O | VSS_REG | Internal Vcc reference |
| 6 | O | OUT2B | Output half bridge 2B |
| 7 | Gnd | GND2 | Power negative supply |
| 8 | Power | VCC2 | Power positive supply |
| 9 | O | OUT2A | Output half bridge 2A |
| 10 | O | OUT1B | Output half bridge 1B |
| 11 | Power | VCC1 | Power positive supply |
| 12 | Gnd | GND1 | Power negative supply |

Table 1. Pin description (continued)

| Pin | Type | Name | Description |
|---|---|---|---|
| 13 | I/O | OUT1A | Output half bridge 1A |
| 14 | GND | GND_REG | Internal ground reference |
| 15 | Power | VDD_REG | Internal 3.3 V reference voltage |
| 16 | I | CONFIG | Paralleled mode command |
| 17 | | N.C. | Not connected |
| 18 | | N.C. | Not connected |
| 19 | | N.C. | Not connected |
| 20 | | N.C. | Not connected |
| 21 | Power | VDD_DIG | Positive supply digital |
| 22 | GND | GND_DIG | Digital ground |
| 23 | I | PWDN | Power down |
| 24 | Power | VDD_PLL | Positive supply for PLL |
| 25 | I | FILTER_PLL | Connection to PLL filter |
| 26 | GND | GND_PLL | Negative supply for PLL |
| 27 | I | XTI | PLL input clock, 256 Fs, or 384 Fs |
| 28 | I | BICKI | $I^2S$ serial clock |
| 29 | I | LRCKI | $I^2S$ left/right clock |
| 30 | I | SDI | $I^2S$ serial data channel |
| 31 | I | RESET | Reset |
| 32 | O | INT_LINE | Fault interrupt |
| 33 | I | ONSEL | Onersampling selector<br>0: 256 Fs<br>1: 384 Fs |
| 34 | I | GAIN | Gain selector<br>0: 0 dBFs<br>1: 24 dBFs |
| 35 | GND | GND_DIG | Digital ground |
| 36 | Power | VDD_DIG | Digital supply |

# 3 Electrical specifications

## 3.1 Thermal data

**Table 2. Thermal data**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $R_{Th(j\text{-}case)}$ | Thermal resistance junction to case (thermal pad) | | 1.5 | 2 | °C/W |
| $T_{sd}$ | Thermal shut-down junction temperature | | 150 | | °C |
| $T_w$ | Thermal warning temperature | | 130 | | °C |
| $T_{hsd}$ | Thermal shut-down hysteresis | | 20 | | °C |

## 3.2 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VCC | Power supply voltage (VCCxA,VCCxB) | | | 20 | V |
| $V_L$ | Logic input interface | -0.3 | | 4 | V |
| VDD_DIG | Positive supply digital | | | 4 | V |
| $T_{op}$ | Operating junction temperature | 0 | | 150 | °C |
| $T_{stg}$ | Storage temperature | -40 | | 150 | °C |

## 3.3 Recommended operating condition

**Table 4. Recommended operating condition**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_S$ | Power supply voltage (VCCxA,VCCxB) | 4.5 | | 18.0 | V |
| $V_L$ | Logic Input Interface | 2.7 | 3.3 | 3.6 | V |
| VDD_DIG | Positive supply digital | 2.7 | 3.3 | 3.6 | V |
| $T_{amb}$ | Ambient temperature | 0 | | 70 | °C |

## 3.4 Electrical characteristics

**Table 5. Electrical characteristics**

($V_{CC}$ = 18 V,VDD_DIG=3.3 V $f_{sw}$ = 384 kHz, $T_{amb}$ = 25 °C, $R_L$ = 8 Ω unless otherwise specified)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Po | Output power BTL | THD = 1 % | | 16 | | W |
| | | THD = 10% | | 20 | | |
| $R_{dsON}$ | Power Pchannel/Nchannel MOSFET (Total Bridge) | Id=1A | | 180 | 250 | mΩ |
| $I_{dss}$ | Power Pchannel/Nchannel leakage | $V_{cc}$ = 18V | | | 10 | µA |
| gP | Power Pchannel RdsON Matching | Id=1A | 95 | | | % |
| gN | Power Nchannel RdsON Matching | Id=1A | 95 | | | % |
| $I_{LDT}$ | Low current dead time (static) | Resistive load *Figure 3*. | | 5 | 10 | ns |
| $I_{HDT}$ | High current dead time (dynamic) | @Iload = 1.5 A (*Figure 5*) | | 10 | 20 | ns |
| $t_r$ | Rise time | Resistive load *Figure 3*. | | 8 | 10 | ns |
| $t_f$ | Fall time | Resistive load *Figure 3*. | | 8 | 10 | ns |
| VCC | Supply voltage operating voltage | | 4.5 | | 18 | V |
| $I_{cc}$ | Supply current from Vcc in power down | PWRDN = 0 | | 0.1 | | mA |
| | Supply current from Vcc in operation | PCM Input signal = -60 dBFS.<br>Switching frequency = 384KHz<br>No LC filters | | 30 | | mA |
| | Supply current DDX processing (reference only) | Internal clock = 49.152 MHz | | 80 | | mA |
| $I_{lim}$ | Overcurrent limit | Nonlinear output | 2.2 | 3.5 | 4.3 | A |
| $I_{sc}$ | short circuit protection | Hi-Z output | 2.7 | 3.8 | 5.0 | A |
| UVL | Under voltage protection threshold | | | 3.5 | 4.3 | V |
| tmin | Output minimum pulse width | No load | 20 | 30 | 60 | ns |
| DR | Dynamic range | | | 100 | | dB |
| SNR | Signal to noise ratio | A - weighted | | 94 | | dB |
| THD+N | Total harmonic distortion + noise | Po = 1 W, f = 1 kHz | | 0.05 | 0.2 | % |
| PSRR | Power supply rejection ratio | DDX stereo, <5 kHz<br>Vripple = 1 $V_{RMS}$<br>Audio input = dither only | | 80 | | dB |

**Table 5. Electrical characteristics** (continued)
($V_{CC}$ = 18 V,VDD_DIG=3.3 V $f_{sw}$ = 384 kHz, $T_{amb}$ = 25 °C, $R_L$ = 8 Ω unless otherwise specified)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $X_{TALK}$ | Crosstalk | DDX stereo, <5 kHz<br>One CH driven @ 1 W<br>other channel measured | | 80 | | dB |
| η | Peak efficiency, DDX mode | Po = 2 x 20 W, 8 Ω | | 90 | | % |

**Table 6. Functional pin status**

| Pin name | Pin number | Logic value | IC status |
|---|---|---|---|
| PWRDN | 23 | 0 | Low absorption |
| PWRDN | 23 | 1 | Normal operation |

# 4 Testing

**Figure 3. Resistive load**

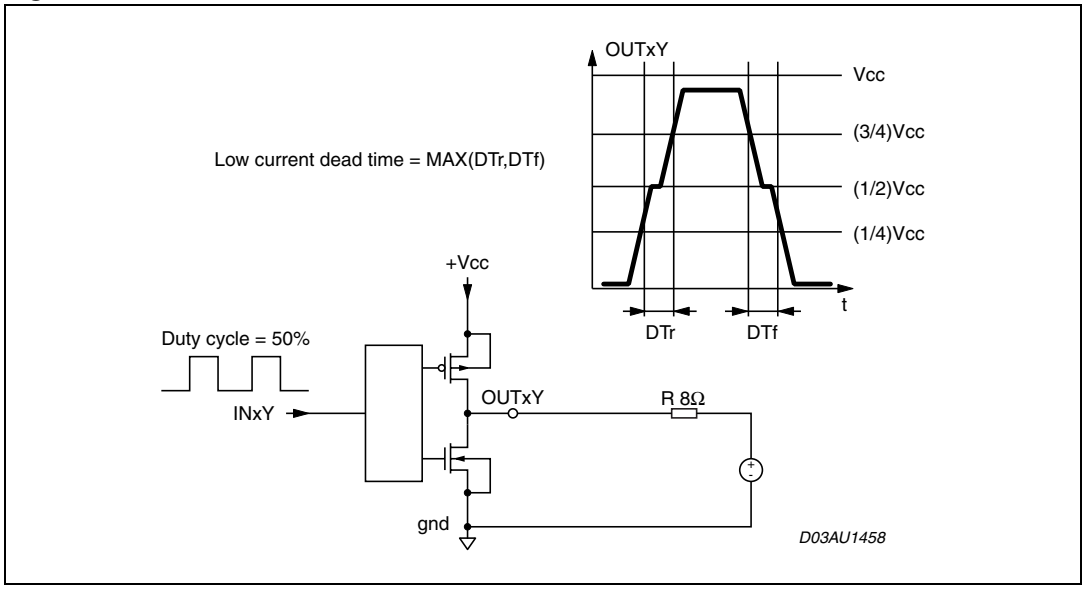
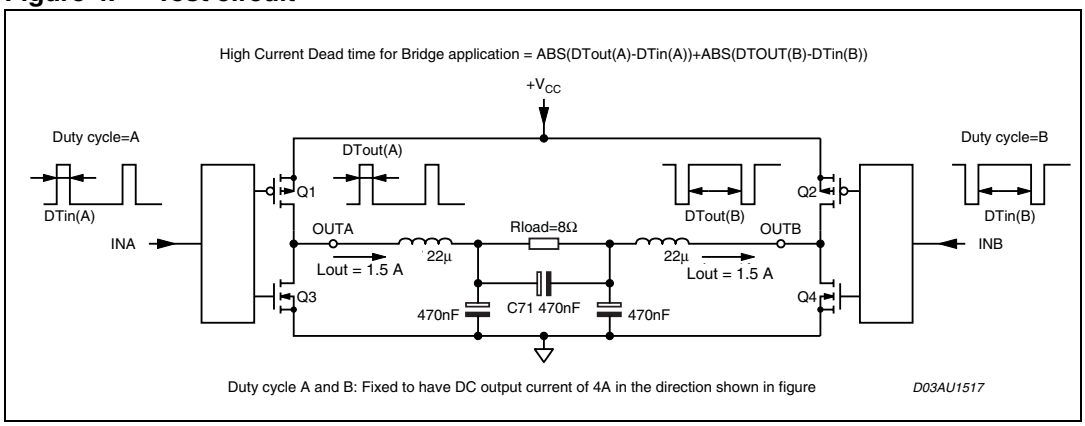



**Figure 4. Test circuit**



# 5 Functional description

## 5.1 Serial audio interface protocols

**Figure 5. $I^2S$**

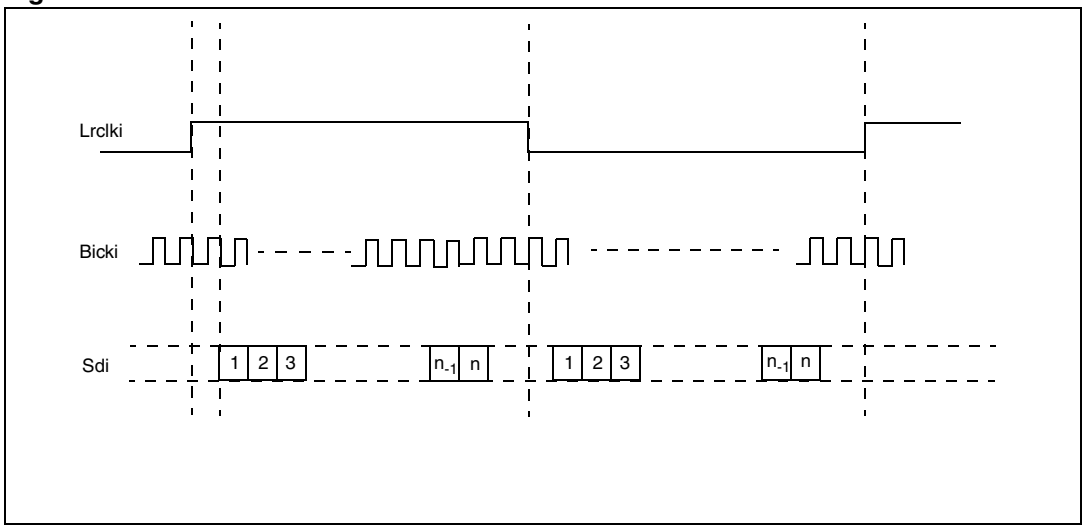
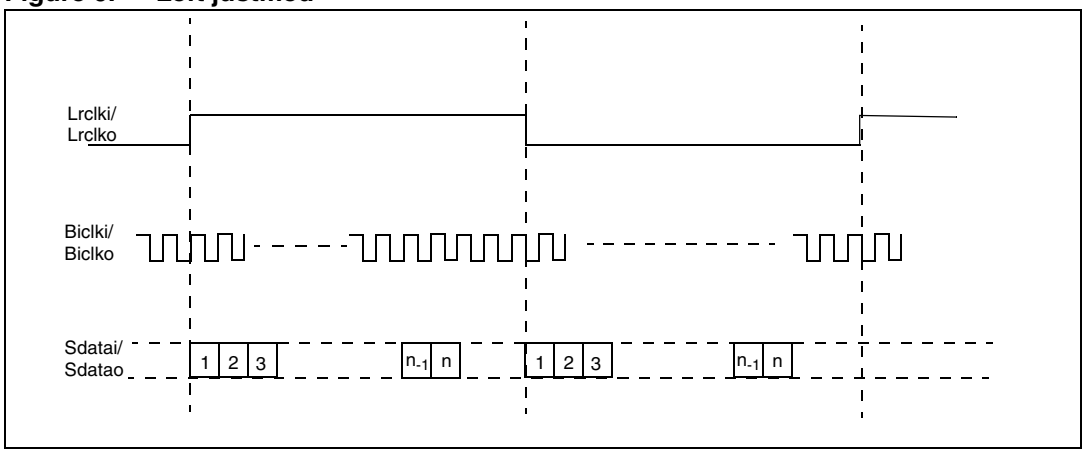



**Figure 6. Left justified**




## 5.2 Fault detect recovery bypass

The on-chip STA333ML power output block provides feedback to the digital controller using inputs to the power control block. The FAULT input is used to indicate a fault condition (either over-current or thermal). When FAULT is asserted (set to 0), the power control block attempts a recovery from the fault by asserting the tristate output (setting it to 0 which directs the power output block to begin recovery), holds it at 0 for 1 ms and then toggles it back to 1. This sequence is repeated for as long as the fault exists.

## 5.3 Zero-detect mute enable

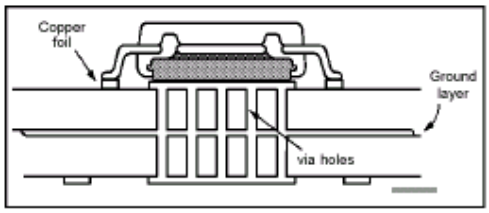
If this function is enabled, the zero-detect circuit examines each processing channel to see if 2048 consecutive zero value samples (regardless of fs) are received. If so the channel is muted.

# 6 Package thermal characteristics

A thermal resistance of 25 °C per Watt can be achieved using a ground copper area of 3 x 3 cm, and using 16 vias, on the PCB (see *Figure 7*). The amount of power dissipated within the device depends primarily on the supply voltage, load impedance and output modulation level.

The max estimated dissipated power for the STA333ML is 3 W. This gives, with the suggested board copper area, a maximum ΔTj of 75 °C. This gives a safety margin before the thermal protection intervention is invoked ($T_j$=150 °C) in consumer environments where a 50 °C is the maximum ambient temperature.

**Figure 7. Thermal characteristic**



# 7 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.ECOPACK is an ST trademark.

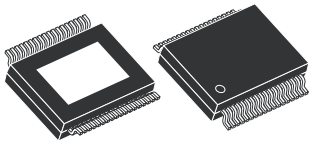
ECOPACK specifications are available at: www.st.com.

**Figure 8. PowerSSO36 exposed pad mechanical data and package dimensions**

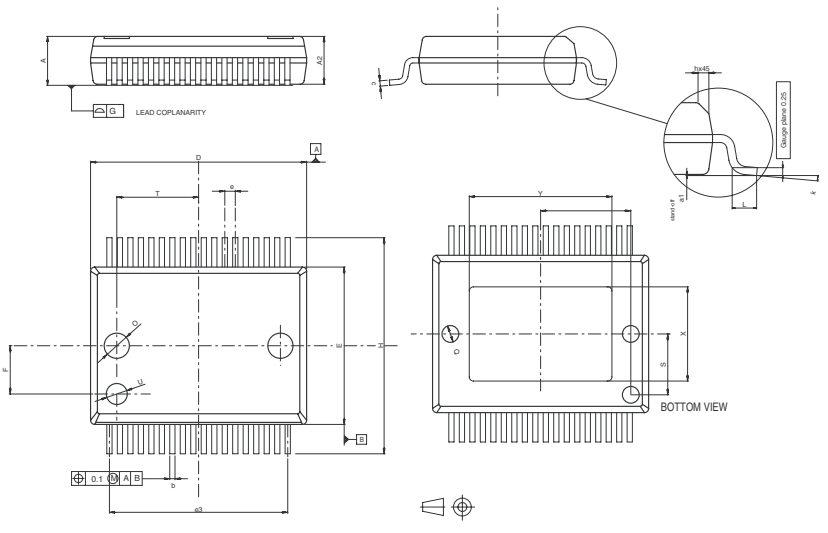
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 2.15 | | 2.47 | 0.084 | | 0.097 |
| A2 | 2.15 | | 2.40 | 0.084 | | 0.094 |
| a1 | 0 | | 0.075 | 0 | | 0.003 |
| b | 0.18 | | 0.36 | 0.007 | | 0.014 |
| c | 0.23 | | 0.32 | 0.009 | | 0.012 |
| D (1) | 10.10 | | 10.50 | 0.398 | | 0.413 |
| E (1) | 7.4 | | 7.6 | 0.291 | | 0.299 |
| e | | 0.5 | | | 0.019 | |
| e3 | | 8.5 | | | 0.335 | |
| F | | 2.3 | | | 0.090 | |
| G | | | 0.10 | | | 0.004 |
| G1 | | | 0.06 | | | 0.002 |
| H | 10.10 | | 10.50 | 0.398 | | 0.413 |
| h | | | 0.40 | | | 0.016 |
| k | | 5° | | | 5° | |
| L | 0.55 | | 0.90 | 0.022 | | 0.035 |
| M | | 4.3 | | | 0.169 | |
| N | | | 10° | | | 10° |
| O | | 1.2 | | | 0.047 | |
| Q | | 0.8 | | | 0.031 | |
| S | | 2.9 | | | 0.114 | |
| T | | 3.65 | | | 0.144 | |
| U | | 1.0 | | | 0.039 | |
| X | 4.1 | | 4.7 | 0.161 | | 0.185 |
| Y | 6.5 | | 7.3 | 0.256 | | 0.287 |

(1) "D" and "E" do not include mold flash or protrusions Mold flash or protrusions shall not exceed 0.15 mm per side(0.006")

**OUTLINE AND MECHANICAL DATA**



**PowerSSO-36 (exposed pad)**



# 8 Revision history

Table 7. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 1-Feb-2007 | 1 | Initial release. |

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