



STB160NF3LL

N-CHANNEL 30V - 0.0026 Ω - 160A D²PAK STripFET™ II POWER MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
ST160NF3LL	30 V	<0.003 Ω	160 A

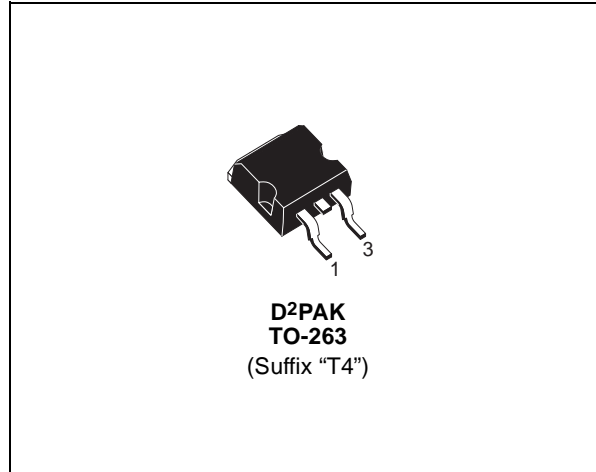
- TYPICAL R_{DS(on)} = 0.0026 Ω
- LOW THRESHOLD DRIVE
- ULTRA LOW ON-RESISTANCE
- LOGIC LEVEL DEVICE
- 100% AVALANCHE TESTED
- SURFACE-MOUNTING D²PAK (TO-263)
POWER PACKAGE IN TUBE (NO SUFFIX) OR
IN TAPE & REEL (SUFFIX "T4")

DESCRIPTION

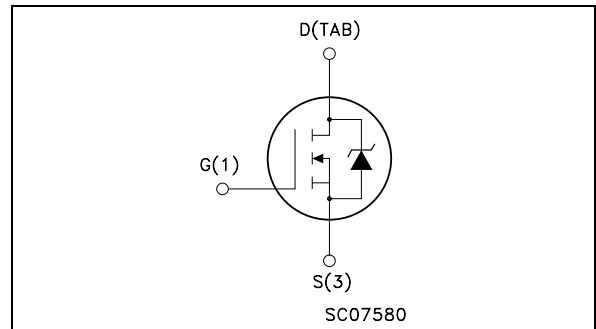
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- HIGH CURRENT, HIGH SWITCHING SPEED
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC & DC-AC CONVERTERS
- SOLENOID AND RELAY DRIVERS



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	30	V
V _{GS}	Gate- source Voltage	± 15	V
I _D (*)	Drain Current (continuous) at T _C = 25°C	160	A
I _D	Drain Current (continuous) at T _C = 100°C	160	A
I _{DM} (•)	Drain Current (pulsed)	640	A
P _{tot}	Total Dissipation at T _C = 25°C	300	W
	Derating Factor	2	W/°C
E _{AS} (¹)	Single Pulse Avalanche Energy	1.2	J
T _{stg}	Storage Temperature	-55 to 175	°C
T _j	Max. Operating Junction Temperature		

(•) Pulse width limited by safe operating area.

(*) Current Limited by Package

(1) Starting T_j = 25 °C, I_D = 80A, V_{DD} = 20V

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THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	0.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose		300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 15 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 80 A V _{GS} = 4.5 V I _D = 80 A		0.0026 0.0032	0.0030 0.0043	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} = 15 V I _D = 80 A		60		S
C _{iss}	Input Capacitance	V _{DS} = 25V f = 1 MHz V _{GS} = 0		6200		pF
C _{oss}	Output Capacitance			1720		pF
C _{rss}	Reverse Transfer Capacitance			300		pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	$V_{DD} = 15\text{ V}$ $I_D = 80\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 3)		50 350		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD}=24\text{V}$ $I_D=160\text{A}$ $V_{GS}=5\text{V}$		95 25 45	125	nC nC nC

SWITCHING OFF(*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 15\text{ V}$ $I_D = 80\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 3)		150 120		ns ns

SOURCE DRAIN DIODE(*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (*)	Source-drain Current Source-drain Current (pulsed)				160 640	A A
V_{SD} (*)	Forward On Voltage	$I_{SD} = 160\text{ A}$ $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 160\text{ A}$ $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		90 200 5		ns nC A

(*)Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.(*)Pulse width limited by T_{jmax}

Fig. 1: Unclamped Inductive Load Test Circuit

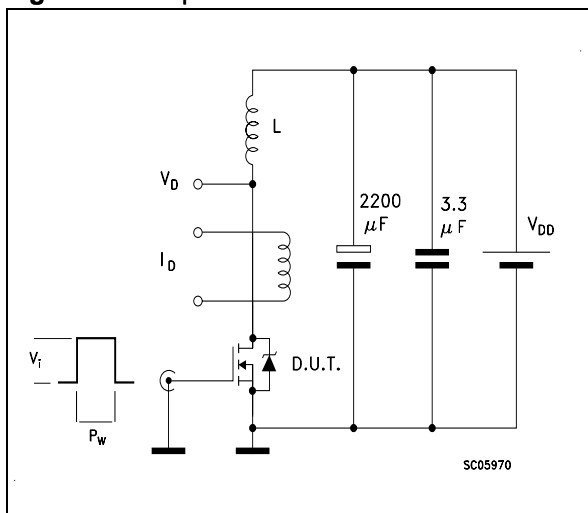


Fig. 2: Unclamped Inductive Waveform

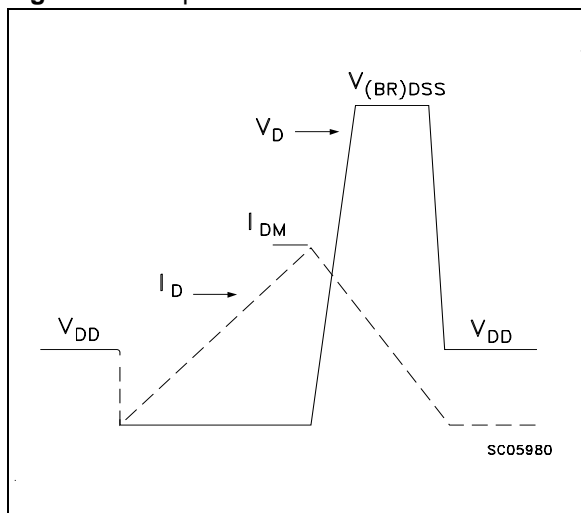


Fig. 3: Switching Times Test Circuits For Resistive Load

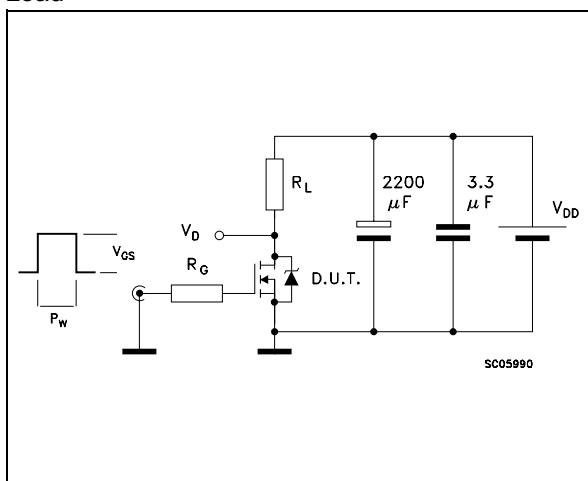


Fig. 4: Gate Charge test Circuit

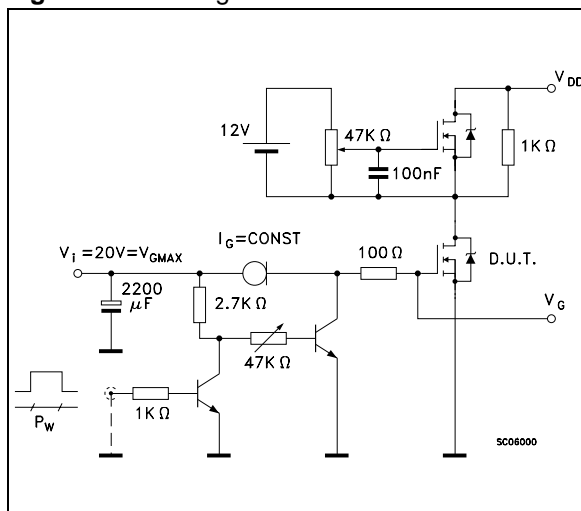
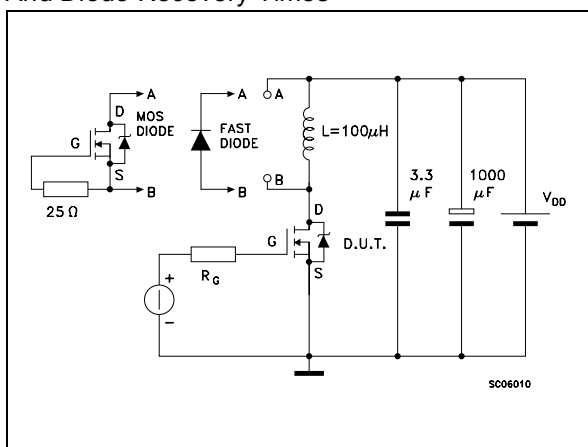
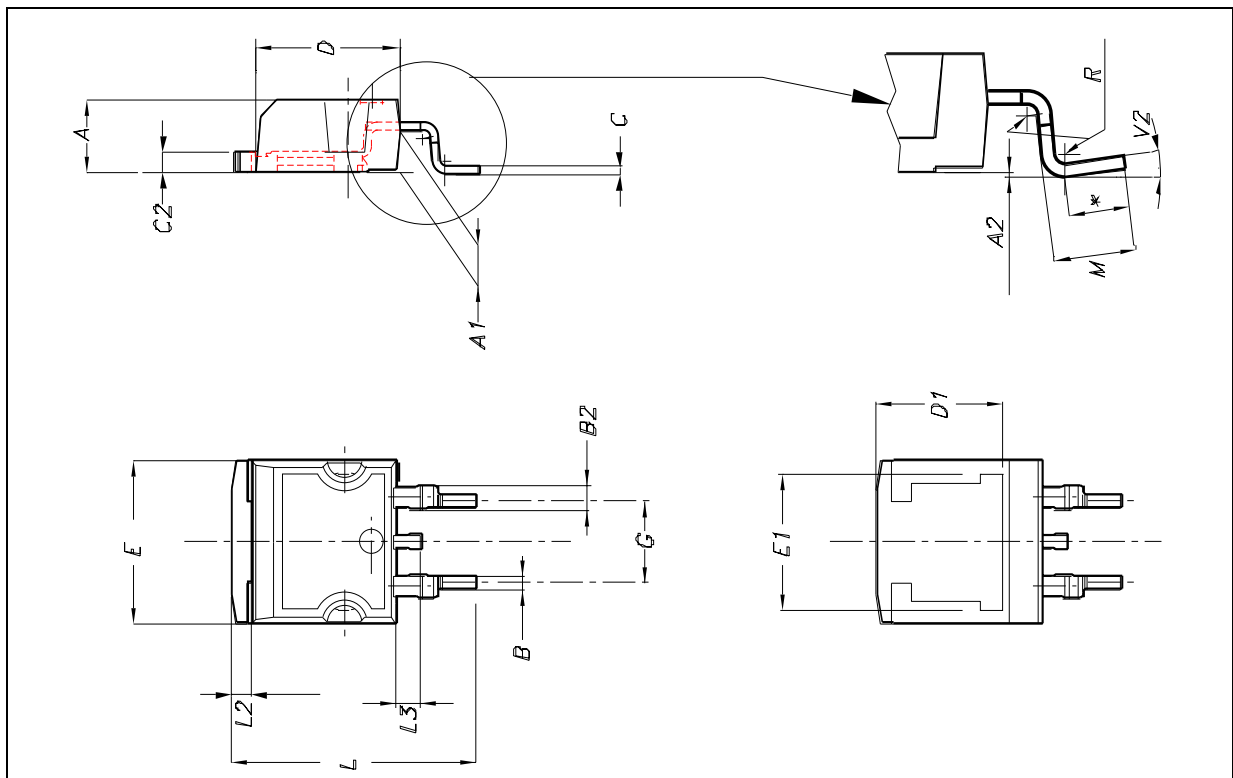


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



D²PAK MECHANICAL DATA

DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.028		0.037
B2	1.14		1.7	0.045		0.067
C	0.45		0.6	0.018		0.024
C2	1.21		1.36	0.048		0.054
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.394		0.409
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.591		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.069
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°	0°		8°



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