



## STB85NF3LL

N-channel 30V - 0.006 $\Omega$  - 85A - D<sup>2</sup>PAK  
Low gate charge STripFET™ II Power MOSFET

### General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STB85NF3LL	30V	<0.008 $\Omega$	85A

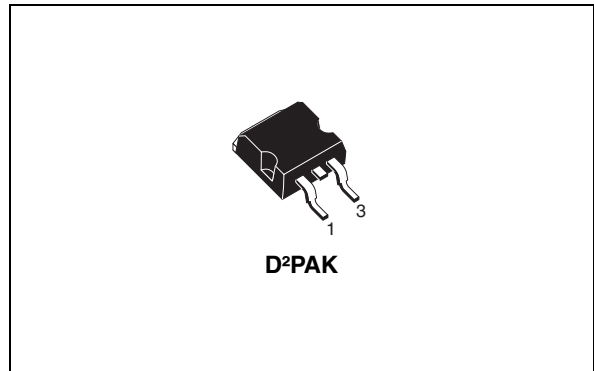
- Optimal R<sub>DS(on)</sub> x Q<sub>g</sub> trade-OFF @4.5V
- Conduction losses reduced
- Switching losses reduced

### Description

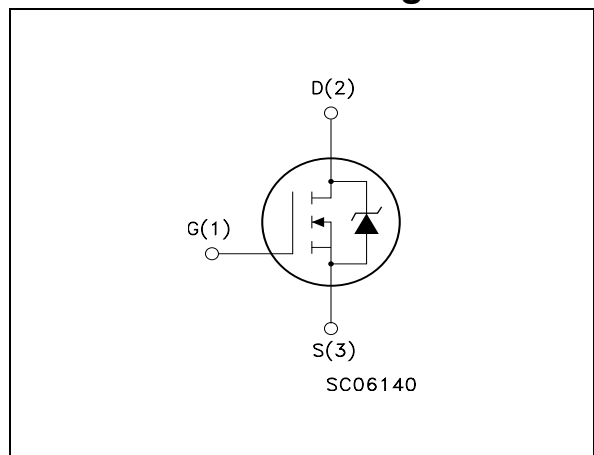
This application specific Power MOSFET is the third generation of STMicroelectronics unique “Single Feature Size” strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

### Applications

- Switching application



### Internal schematic diagram



### Order codes

Part number	Marking	Package	Packaging
STB85NF3LLT4	B85NF3LL	D <sup>2</sup> PAK	Tape & reel

# Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20K\Omega$ )	30	V
$V_{GS}$	Gate-source voltage	$\pm 16$	V
$V_{GSM}$	Gate-source voltage pulsed ( $t_p \leq 50\mu s$ ; duty cycle 25%; $T_J \leq 150^\circ C$ )	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ C$	85	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ C$	60	A
$I_{DM}^{(1)}$	Drain current (pulsed)	340	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ C$	110	W
	Derating factor	0.73	W/ $^\circ C$
$T_{stg}$	Storage temperature	-65 to 175	$^\circ C$
$T_J$	Max. Operating Junction Temperature	175	$^\circ C$

1. Pulse width limited by safe operating area

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance junction-case Max	0.36	$^\circ C/W$
$R_{thJA}$	Thermal resistance junction-ambient Max	62.5	$^\circ C/W$
$T_I$	Maximum lead temperature for soldering purpose	300	$^\circ C$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 16V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 40A$ $V_{GS} = 4.5V, I_D = 40A$		0.006 0.0075	0.008 0.0095	$\Omega$ $\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max},$ $I_D = 40 A$		30		S
$C_{iss}$	Input capacitance	$V_{DS} = 25V, f = 1 \text{ MHz},$ $V_{GS} = 0$		2210		pF
$C_{oss}$	Output capacitance			635		pF
$C_{rss}$	Reverse transfer capacitance			138		pF
$Q_g$	Total gate charge	$V_{DD} = 24V, I_D = 60A$ $V_{GS} = 4.5V$		30	40	nC
$Q_{gs}$	Gate-source charge			9		nC
$Q_{gd}$	Gate-drain charge			12.5		nC

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15V, I_D = 30A,$ $R_G = 4.7\Omega, V_{GS} = 4.5V$ <i>Figure 12 on page 8</i>		22		ns
$t_r$	Rise time			130		ns
$t_{d(off)}$	Turn-off delay time			36.5		ns
$t_f$	Fall time			36.5		ns
$t_{d(off)}$	Off-voltage rise time	$V_{clamp} = 24V, I_D = 30A$ $R_G = 4.7\Omega, V_{GS} = 4.5V$ <i>Figure 14 on page 8</i>		32		ns
$t_f$	Fall time			23		ns
$t_c$	Cross-over time			40		ns

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				85	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				340	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 85A, V_{GS} = 0$			1.3	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 85A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 15V, T_J = 150^\circ C$ <i>Figure 14 on page 8</i>		65 105 3.4		ns $\mu C$ A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

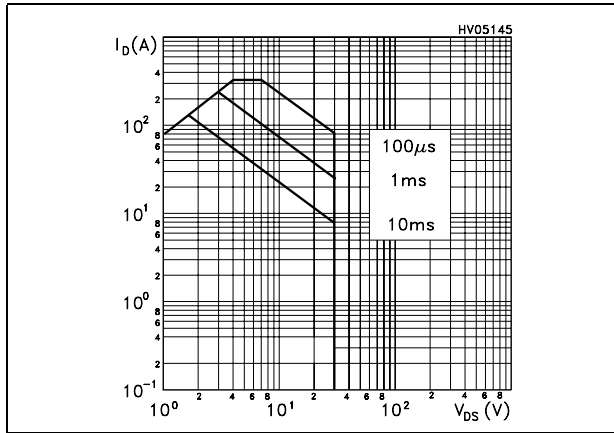


Figure 2. Thermal impedance

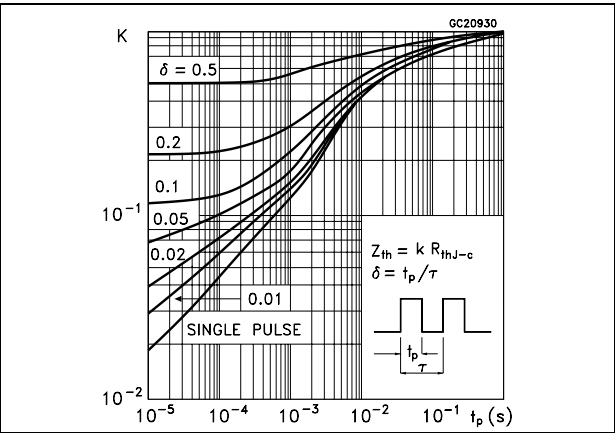


Figure 3. Output characteristics

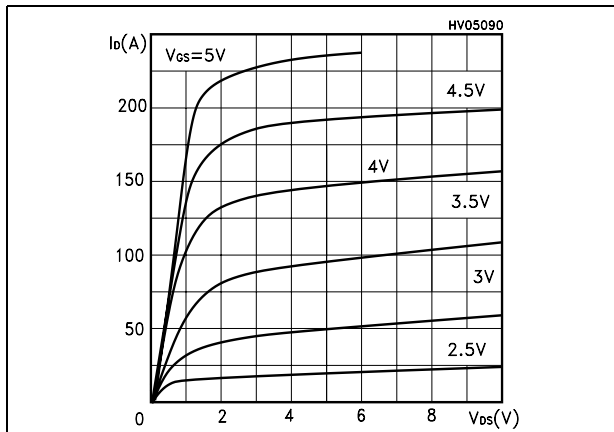


Figure 4. Transfer characteristics

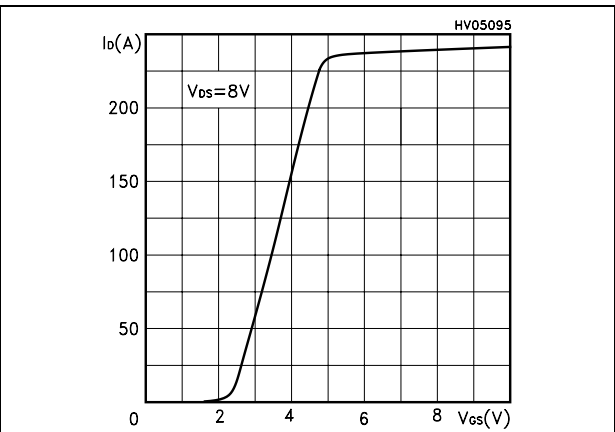


Figure 5. Transconductance

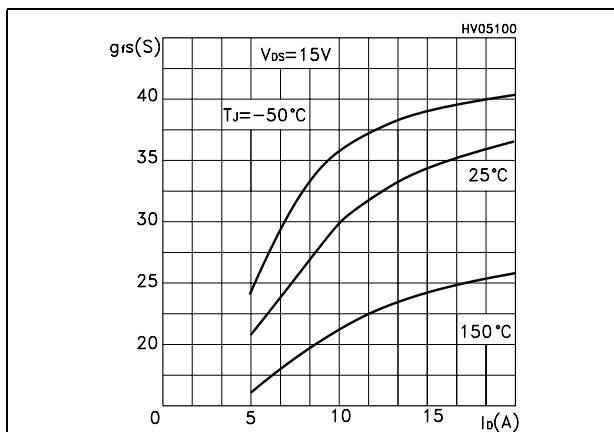


Figure 6. Static drain-source on resistance

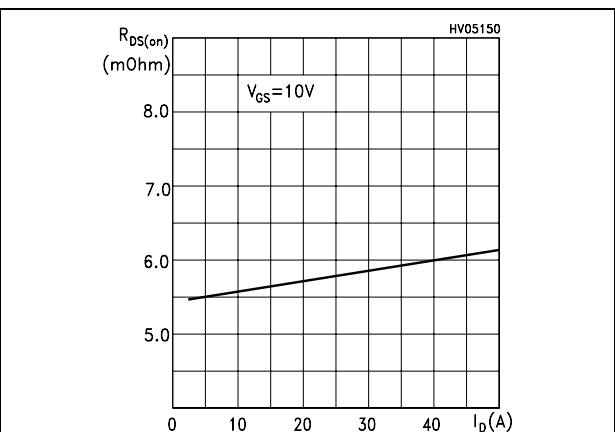


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

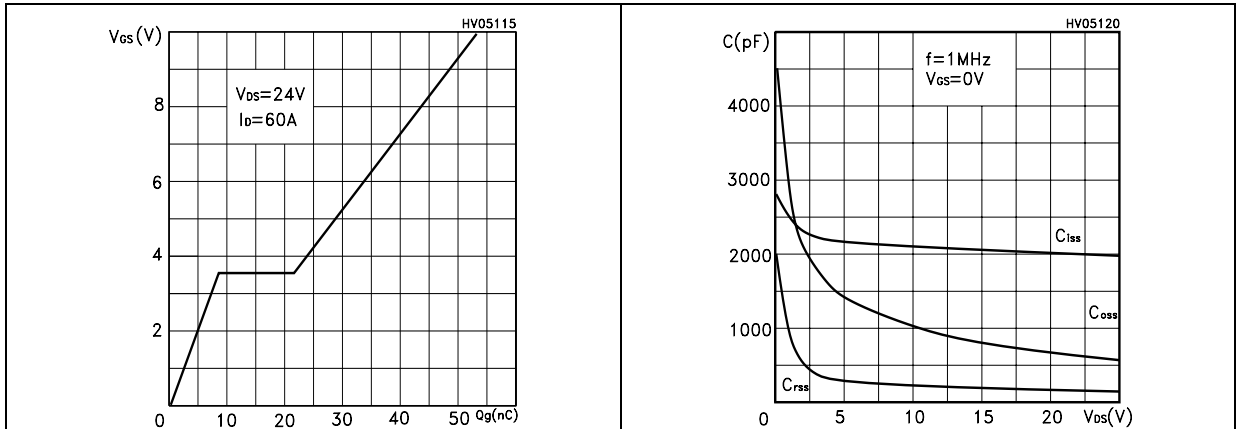


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

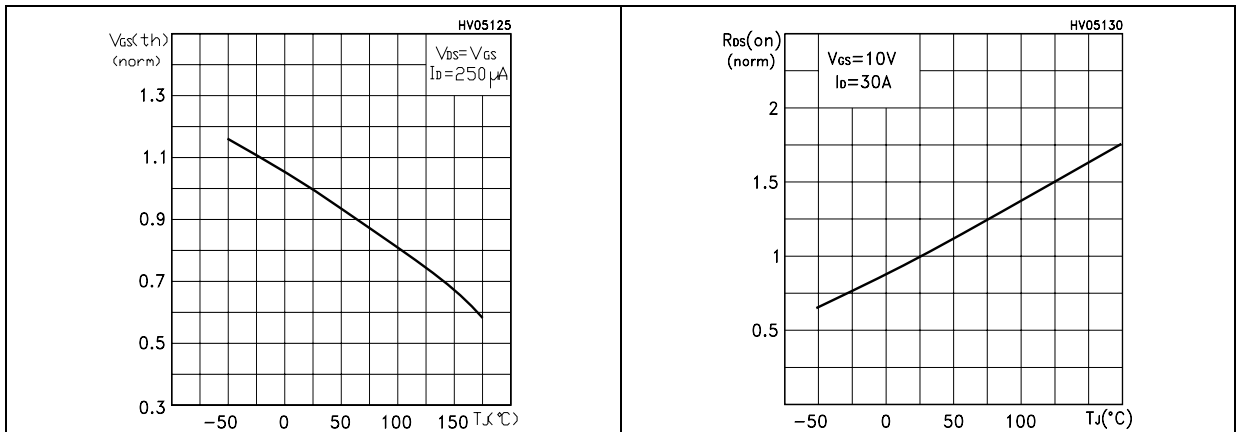
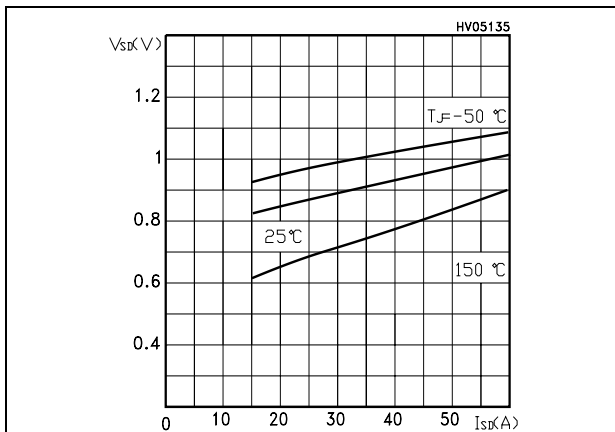


Figure 11. Source-drain diode forward characteristics



### 3 Test circuit

Figure 12. Switching times test circuit for resistive load

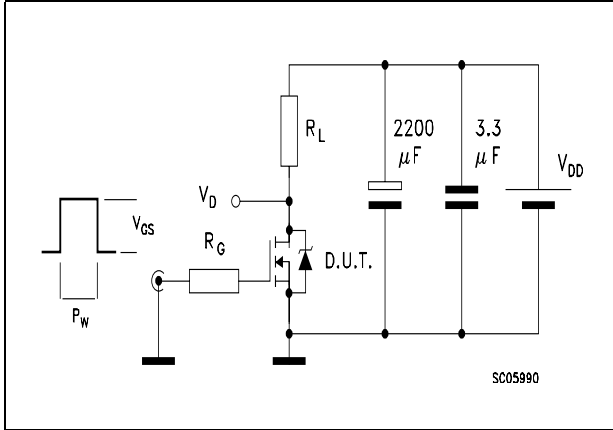


Figure 13. Gate charge test circuit

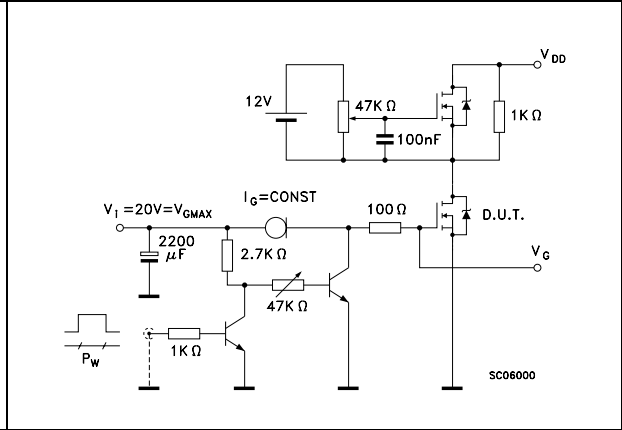


Figure 14. Test circuit for inductive load switching and diode recovery times

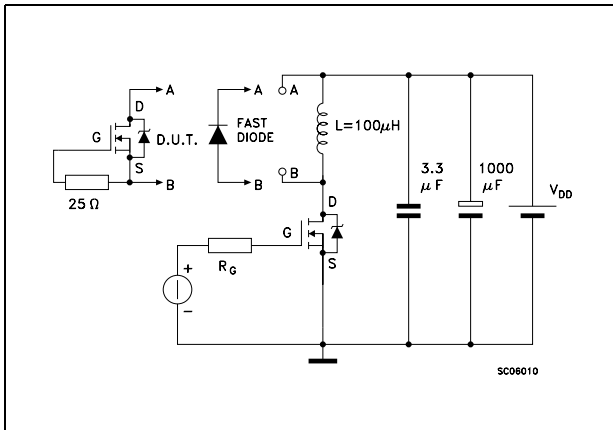


Figure 15. Unclamped Inductive load test circuit

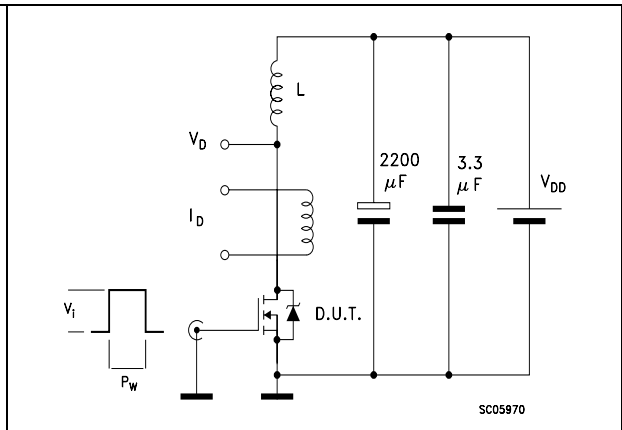
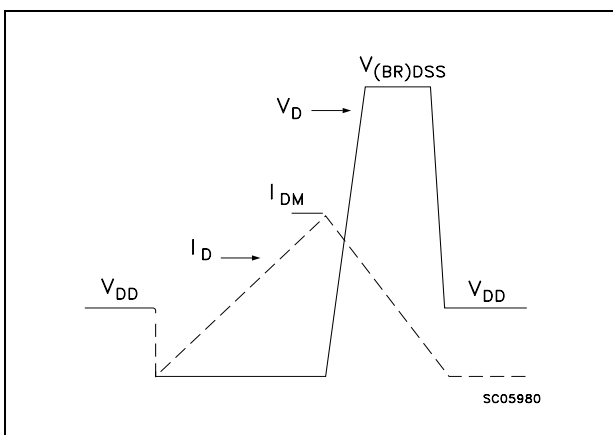


Figure 16. Unclamped inductive waveform



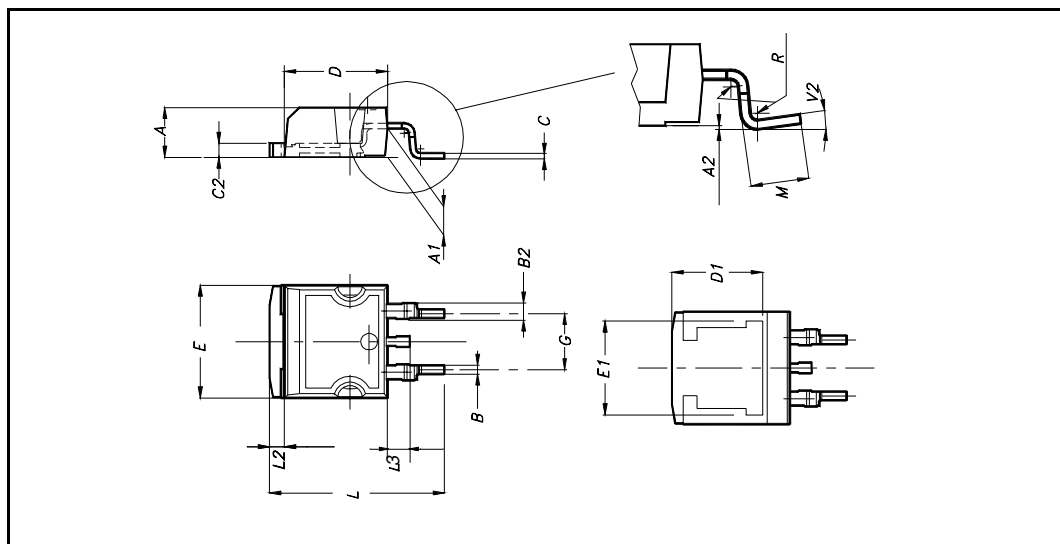


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

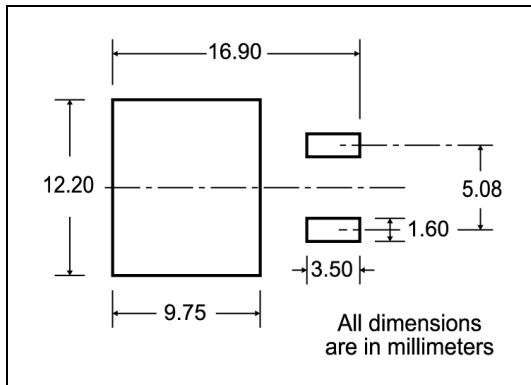
**D<sup>2</sup>PAK MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



## 5 Packaging mechanical data

### D<sup>2</sup>PAK FOOTPRINT



### TAPE AND REEL SHIPMENT

**TAPE MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

**REEL MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

10 pitches cumulative tolerance on tape +/- 0.2 mm

Center line of cavity

User Direction of Feed

FEED DIRECTION

Bending radius

R min.

\* on sales type

## 6 Revision history

**Table 7. Revision history**

Date	Revision	Changes
09-Sep-2004	3	Complete document
28-Jul-2006	4	New template, SOA updated

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