



## STD3NK60ZD

N-channel 600 V, 3.3  $\Omega$ , 2.4 A, DPAK  
SuperFREDMesh™ Power MOSFET

### Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STD3NK60ZD	600 V	< 3.6 $\Omega$	2.4 A

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Fast internal recovery diode

### Application

- Switching applications

### Description

The SuperFREDMesh™ series associates all advantages of reduced on-resistance, Zener gate protection and very high dv/dt capability with a fast body-drain recovery diode. Such series complements the “FDmesh™” advanced technology.

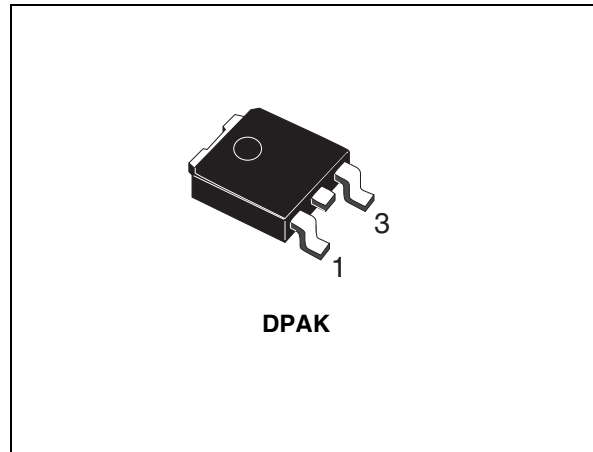


Figure 1. Internal schematic diagram

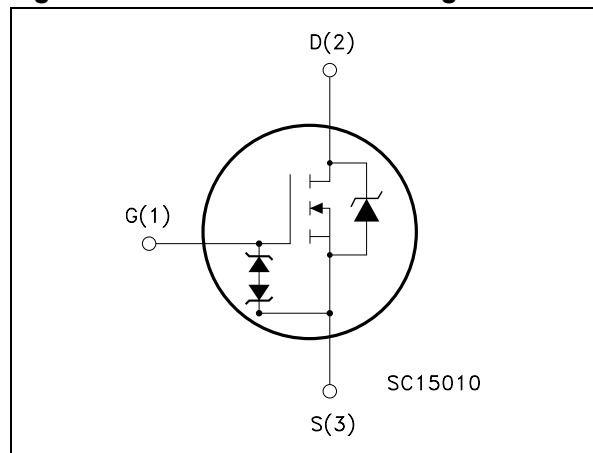


Table 1. Device summary

Order code	Marking	Package	Packaging
STD3NK60ZD	3NK60ZD	DPAK	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	600	V
$V_{GS}$	Gate- source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	2.4	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	1.51	A
$I_{DM}^{(1)}$	Drain current (pulsed)	9.6	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	45	W
	Derating factor	0.36	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 2.4\text{ A}$ ,  $di/dt \leq 600\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal resistance junction-ambient max	100	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max	50	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Max value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	2.4	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	150	mJ

## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	600			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating V <sub>DS</sub> = Max rating, T <sub>C</sub> = 125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			± 10	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 50 μA	3	3.75	4.5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.2 A		3.3	3.6	Ω

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0		311		pF
C <sub>oss</sub>	Output capacitance			43		pF
C <sub>rss</sub>	Reverse transfer capacitance			8		pF
C <sub>oss eq</sub> <sup>(1)</sup>	Equivalent output capacitance	V <sub>GS</sub> = 0, V <sub>DS</sub> = 0 to 400 V		27		pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 2.4 A, V <sub>GS</sub> = 10 V (see <a href="#">Figure 16</a> )		11.8		nC
Q <sub>gs</sub>	Gate-source charge			2.6		nC
Q <sub>gd</sub>	Gate-drain charge			6.4		nC

1. C<sub>oss eq</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>D</sub>S increases from 0 to 80% V<sub>DSS</sub>

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 480\text{ V}$ , $I_D = 3\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15</a> )		9		ns
$t_r$	Rise time			14		ns
$t_{d(off)}$	Turn-off-delay time			19		ns
$t_f$	Fall time			14		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				2.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				9.6	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 10\text{ A}$ , $V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 2.4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 20</a> )		98		ns
$Q_{rr}$	Reverse recovery charge			170		nC
$I_{RRM}$	Reverse recovery current			3.4		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 2.4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 20</a> )		105		ns
$Q_{rr}$	Reverse recovery charge			184		nC
$I_{RRM}$	Reverse recovery current			3.5		A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

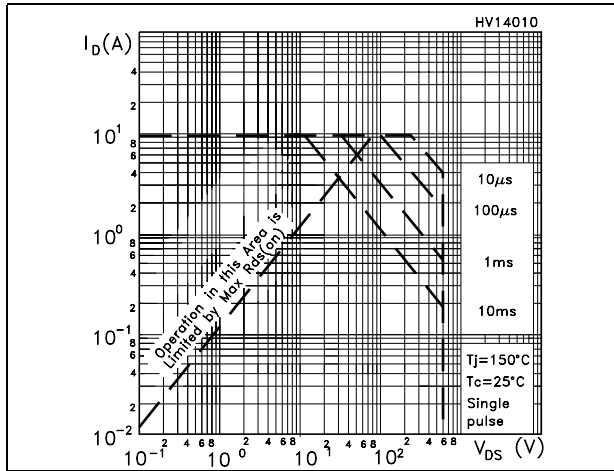


Figure 3. Thermal impedance

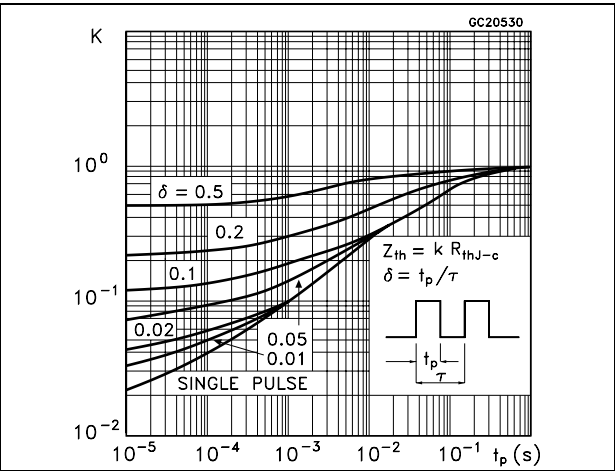


Figure 4. Output characteristics

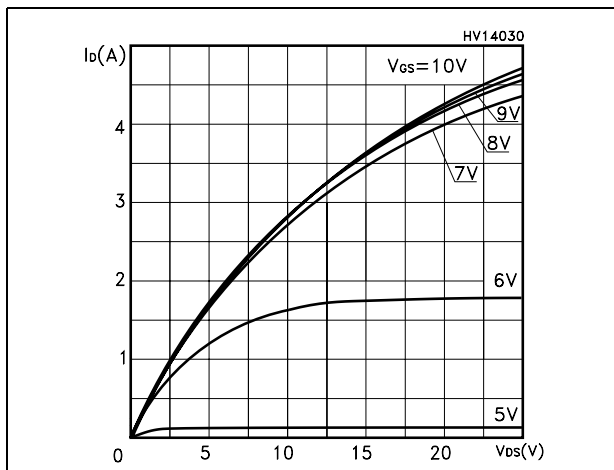


Figure 5. Transfer characteristics

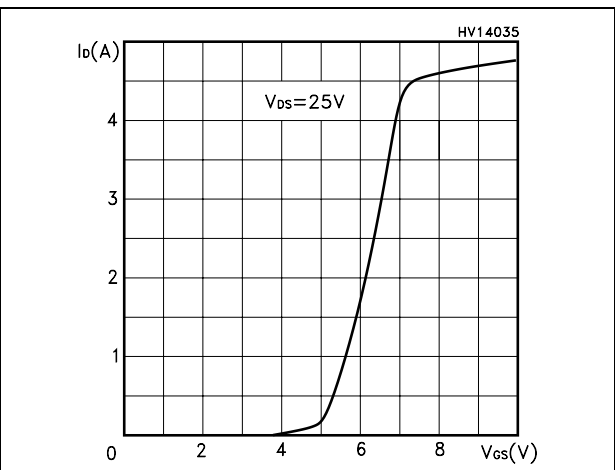


Figure 6. Transconductance

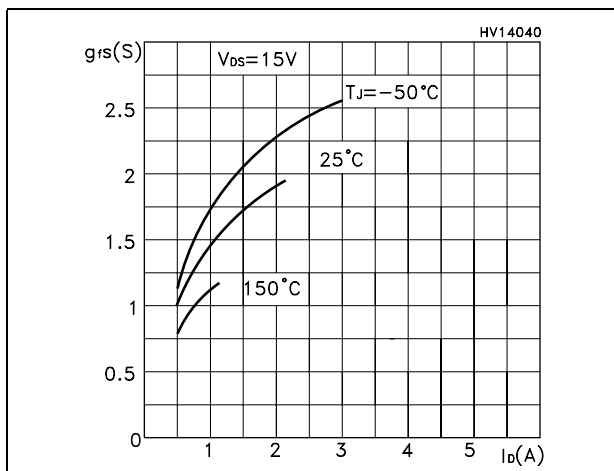


Figure 7. Static drain-source on resistance

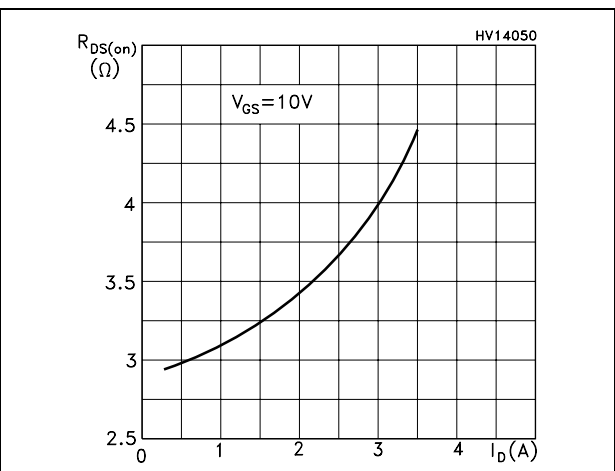


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

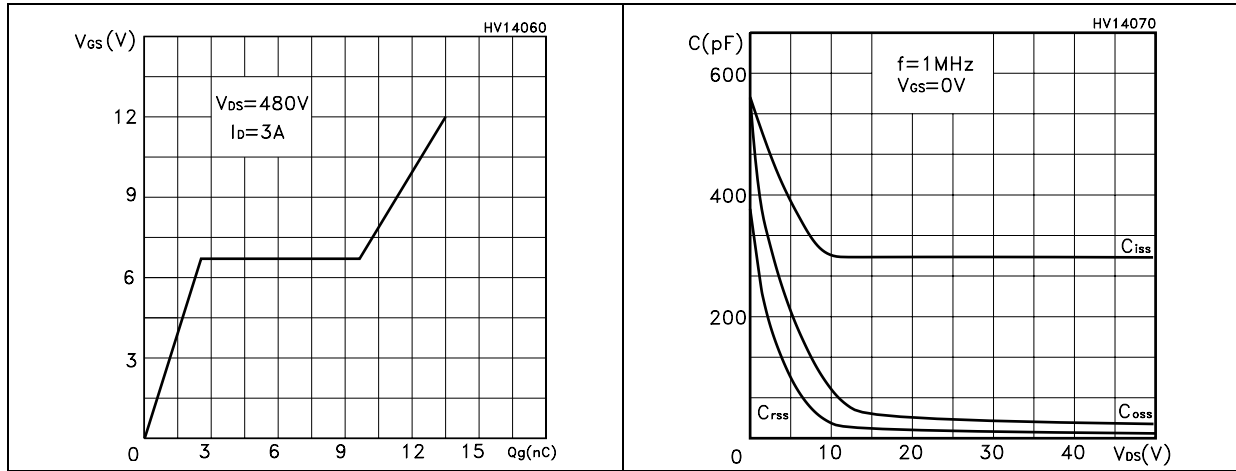


Figure 10. Normalized gate threshold voltage vs temperature

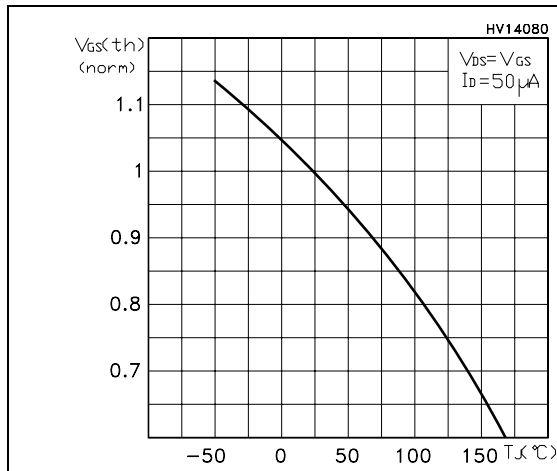


Figure 11. Normalized on resistance vs temperature

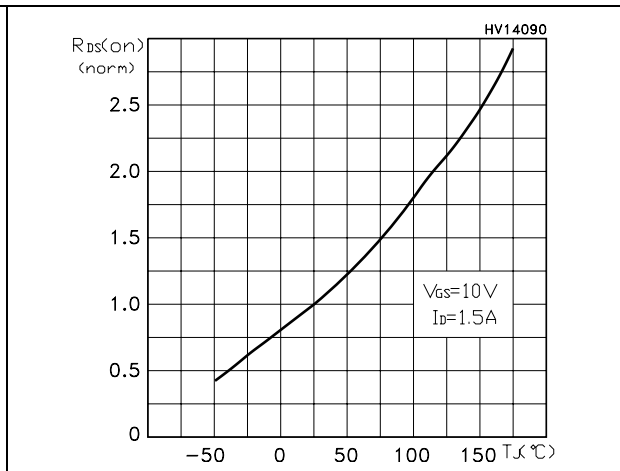


Figure 12. Source-drain diode forward characteristics

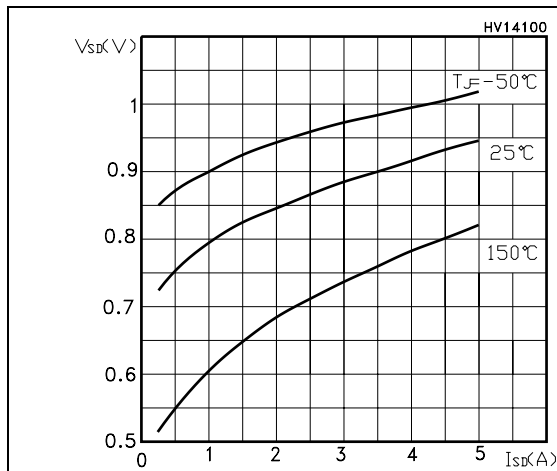


Figure 13. Normalized  $B_{VDS}$  vs temperature

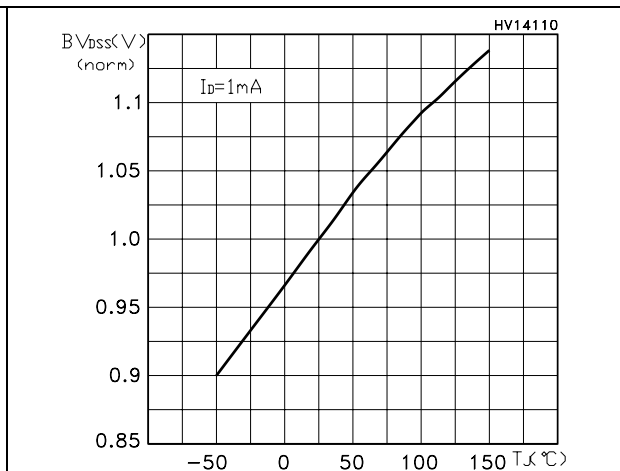
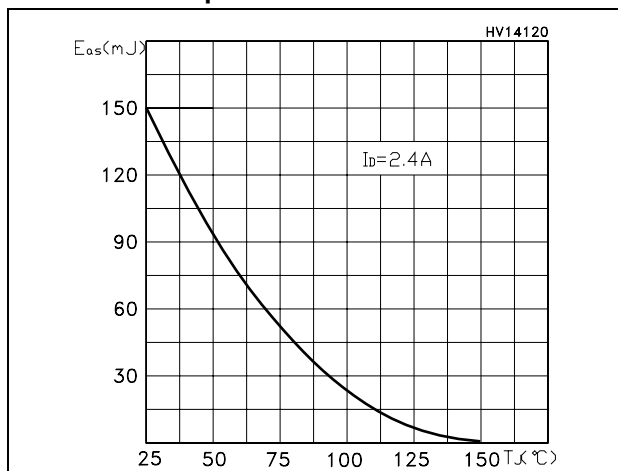


Figure 14. Maximum avalanche energy vs temperature





### 3 Test circuits

Figure 15. Switching times test circuit for resistive load

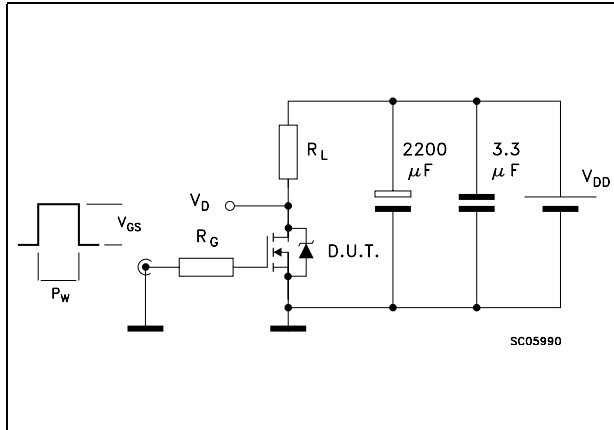


Figure 16. Gate charge test circuit

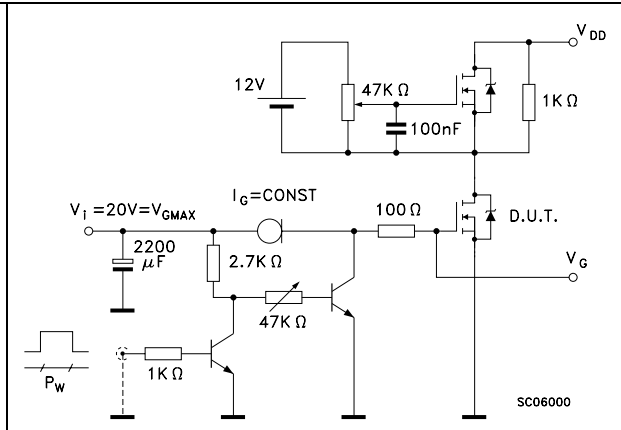


Figure 17. Test circuit for inductive load switching and diode recovery times

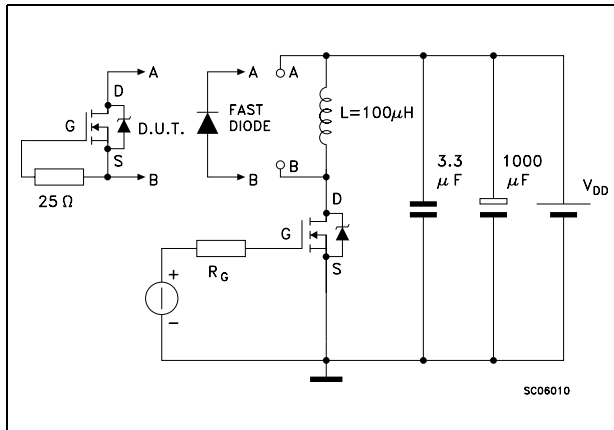


Figure 18. Unclamped Inductive load test circuit

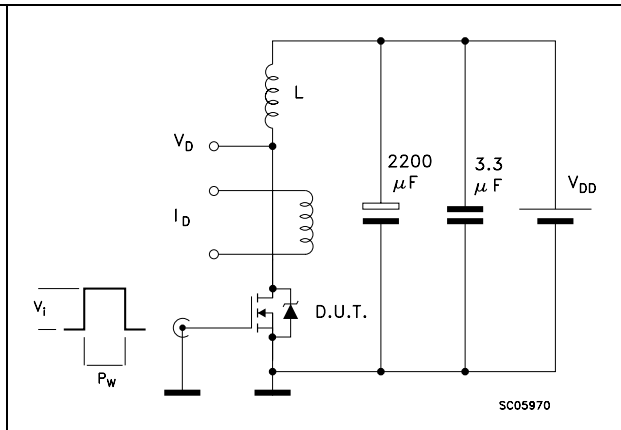


Figure 19. Unclamped inductive waveform

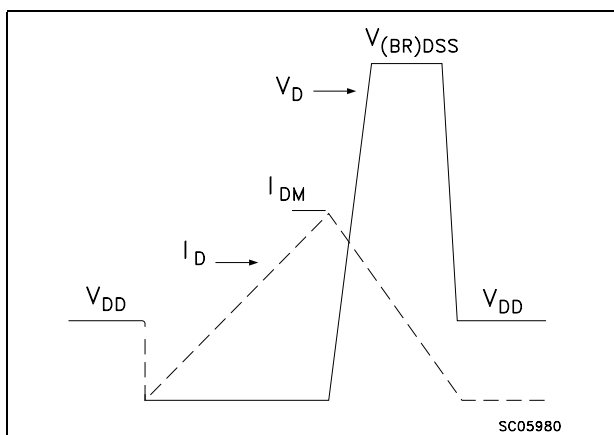
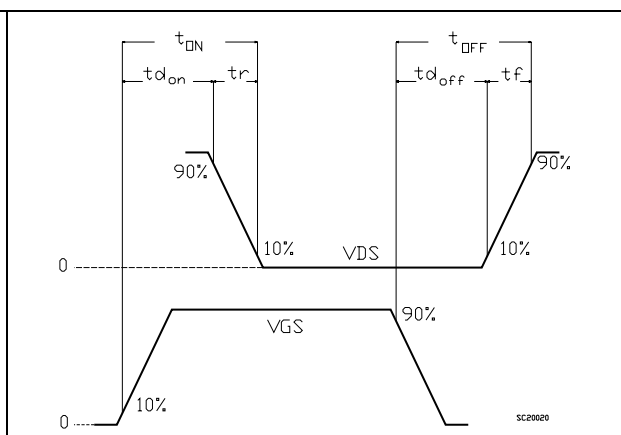


Figure 20. Switching time waveform

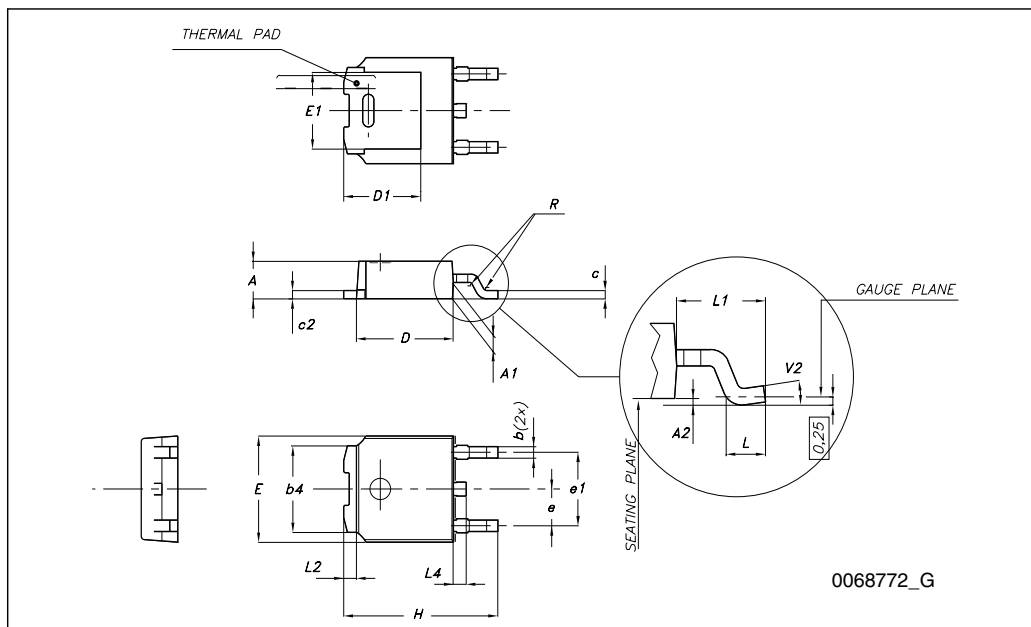


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**TO-252 (DPAK) mechanical data**

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°



# 5 Package mechanical data

## DPAK FOOTPRINT



## TAPE AND REEL SHIPMENT

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY		BULK QTY	
2500		2500	

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

## 6 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
24-Jul-2008	1	First release
11-Sep-2008	2	Document status changed from preliminary data to datasheet

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