



STD60N3LH5 STU60N3LH5

N-channel 30 V, 0.0072 Ω , 48 A - DPAK - IPAK
STripFET™ V Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} Max	I _D
STD60N3LH5	30V	0.008 Ω	48A
STU60N3LH5	30V	0.0084 Ω	48A

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

Application

- Switching applications

Description

This product utilizes the 5th generation of design rules of ST's proprietary STripFET™ technology. The lowest available R_{DS(on)}*Q_g, in the standard packages, makes this device suitable for the most demanding DC-DC converter applications, where high power density is to be achieved.

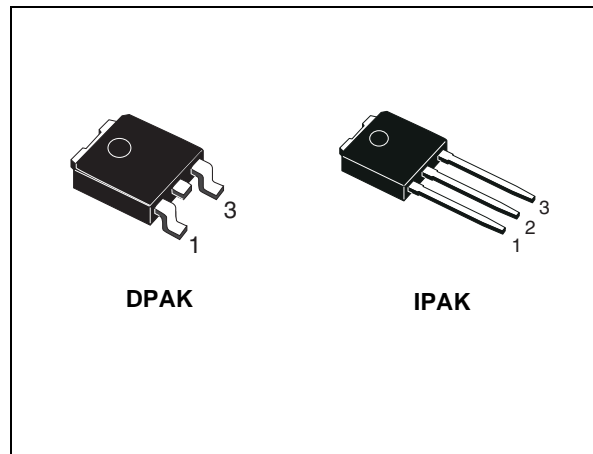


Figure 1. Internal schematic diagram

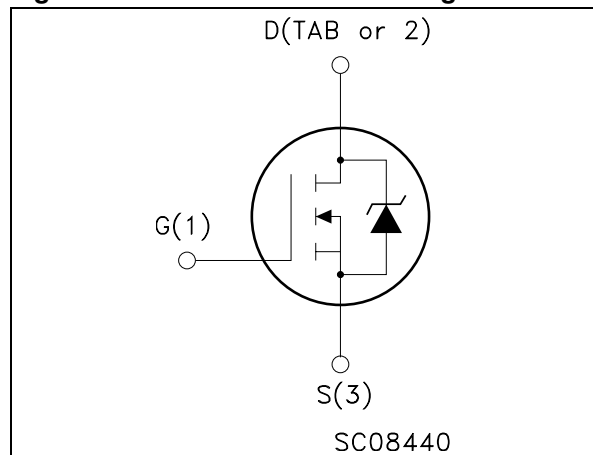


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD60N3LH5	60N3LH5	DPAK	Tape and reel
STU60N3LH5	60N3LH5	IPAK	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS}=0$)	30	V
V_{DS}	Drain-source voltage ($V_{GS} = 0$) @ T_{JMAX}	35	V
V_{GS}	Gate-Source voltage	± 22	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	48	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	42.8	A
$I_{DM}^{(2)}$	Drain current (pulsed)	192	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	60	W
	Derating factor	0.4	W/°C
$E_{AS}^{(3)}$	Single pulse avalanche energy	160	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Limited by wire bonding
2. Pulse width limited by safe operating area
3. Starting $T_j = 25^\circ\text{C}$, $I_d = 24\text{A}$, $V_{dd} = 12\text{V}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.5	°C/W
$R_{thj-amb}$	Thermal resistance junction-case max	100	°C/W
T_j	Maximum lead temperature for soldering purpose	275	°C

2 Electrical characteristics

($T_{CASE} = 25^{\circ}C$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	$I_D = 250\mu A, V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 30V$ $V_{DS} = 30V, T_c = 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 22V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 24A$ SMD version		0.0072	0.008	Ω
		$V_{GS} = 10V, I_D = 24A$		0.0076	0.0084	Ω
		$V_{GS} = 5V, I_D = 24A$ SMD version		0.0088	0.011	Ω
		$V_{GS} = 5V, I_D = 24A$		0.0092	0.0114	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25V, f = 1MHz,$ $V_{GS} = 0$		1350		pF
C_{oss}	Output capacitance			265		pF
C_{rss}	Reverse transfer capacitance			32		pF
Q_g	Total gate charge	$V_{DD} = 15V, I_D = 48A$		8.8		nC
Q_{gs}	Gate-source charge	$V_{GS} = 5V$		4.7		nC
Q_{gd}	Gate-drain charge	(Figure 14)		2.2		nC
Q_{gs1}	Pre V_{th} gate-to-source charge	$V_{DD} = 15V, I_D = 48A$		2.2		nC
Q_{gs2}	Post V_{th} gate-to-source charge	$V_{GS} = 5V$ (Figure 19)		2.5		nC
R_G	Gate input resistance	f=1MHz gate bias Bias= 0 test signal level=20mV open drain		1.1		Ω

Table 6. Switching on/off (resistive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=10V, I_D=24A,$ $R_G=4.7\Omega, V_{GS}=10V$ <i>(Figure 13 and Figure 18)</i>		6		ns
t_r	Rise time			33		ns
$t_{d(off)}$	Turn-off delay time	$V_{DD}=10V, I_D=24A,$ $R_G=4.7\Omega, V_{GS}=10V$ <i>(Figure 13 and Figure 18)</i>		19		ns
t_f	Fall time			4.2		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				48	A
I_{SDM}	Source-drain current (pulsed) ⁽¹⁾				192	A
V_{SD}	Forward on voltage	$I_{SD}=24A, V_{GS}=0$			1.1	V
t_{rr}	Reverse recovery time	$I_{SD}=48A, di/dt=100A/\mu s,$ $V_{DD}=20V, T_j=25^\circ C$ <i>(Figure 15)</i>		25		ns
Q_{rr}	Reverse recovery charge			18.5		nC
I_{RRM}	Reverse recovery current			1.5		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

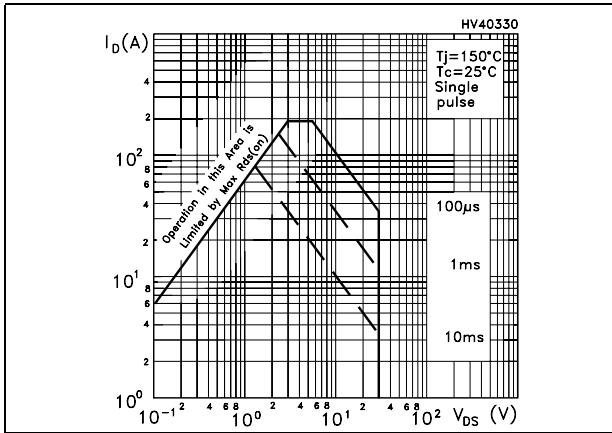


Figure 3. Thermal impedance

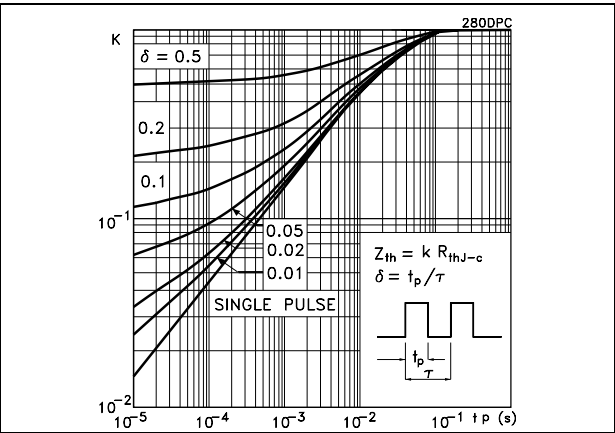


Figure 4. Output characteristics

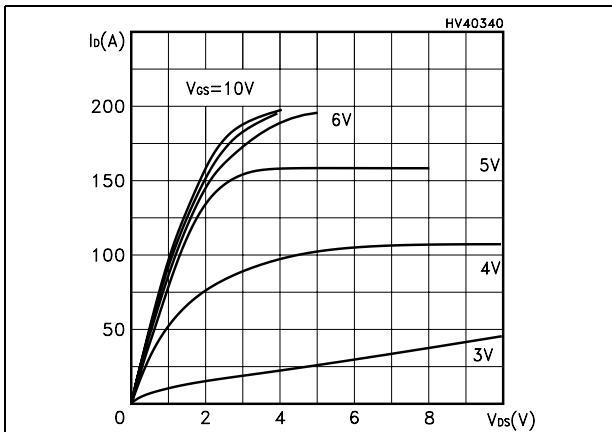


Figure 5. Transfer characteristics

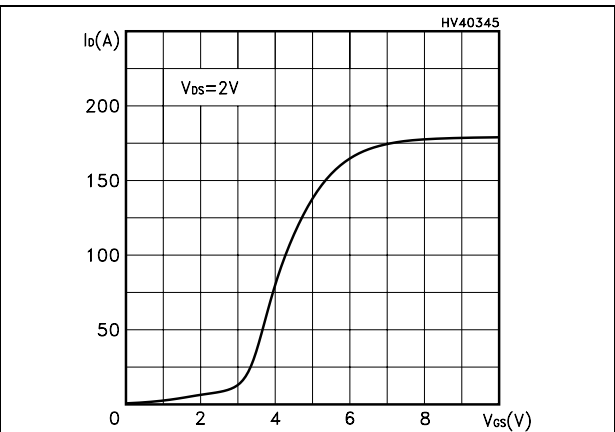


Figure 6. Normalized $B_{V_{DS}}$ vs temperature

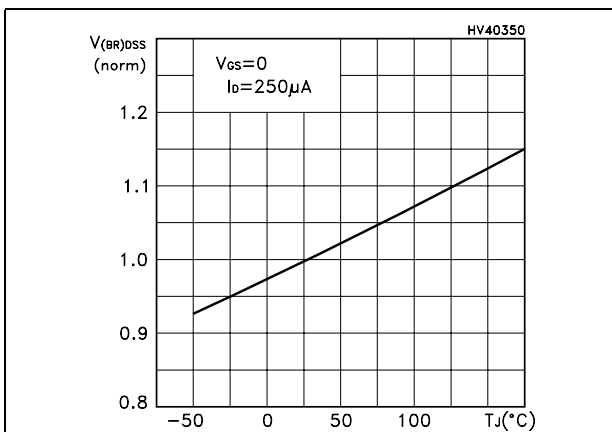


Figure 7. Static drain-source on resistance

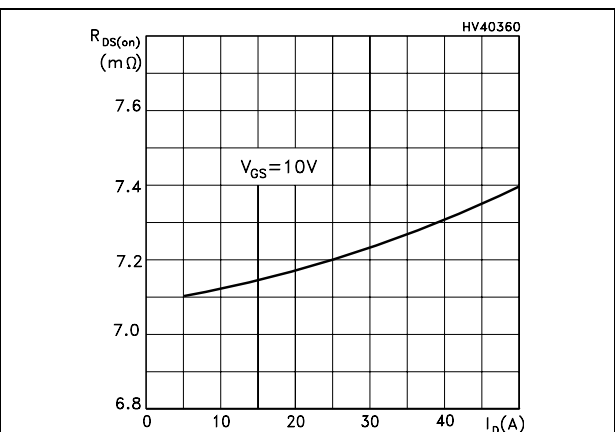


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

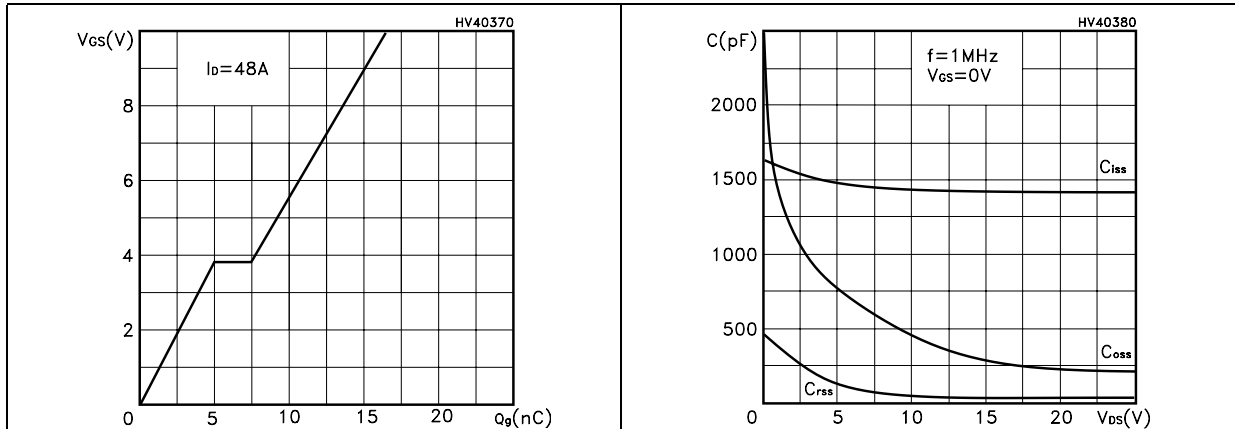


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

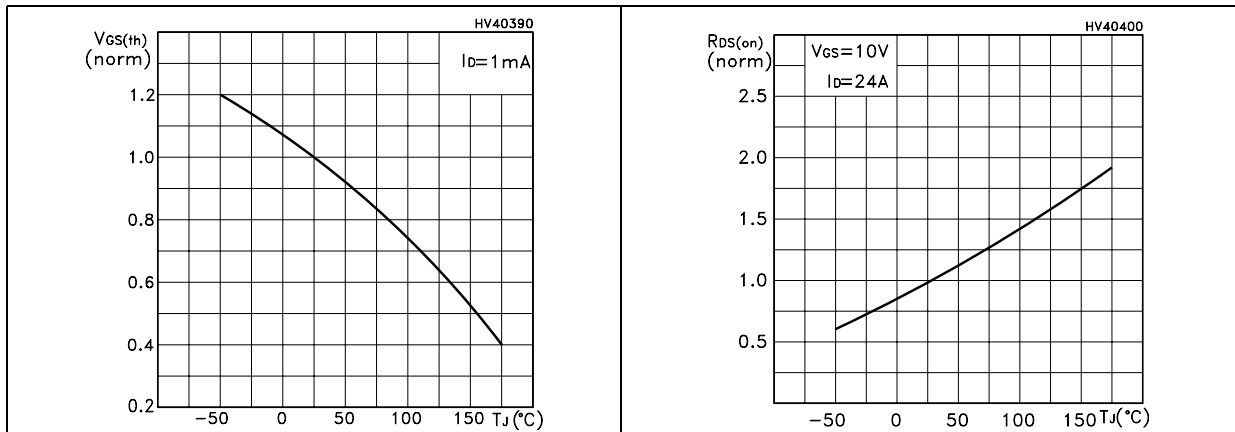
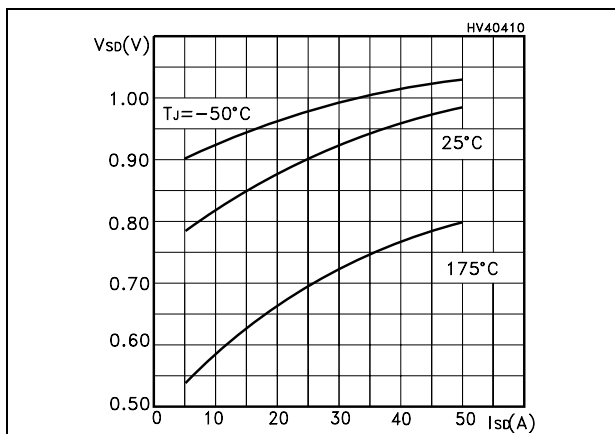


Figure 12. Source-drain diode forward characteristics



3 Test circuit

Figure 13. Switching times test circuit for resistive load

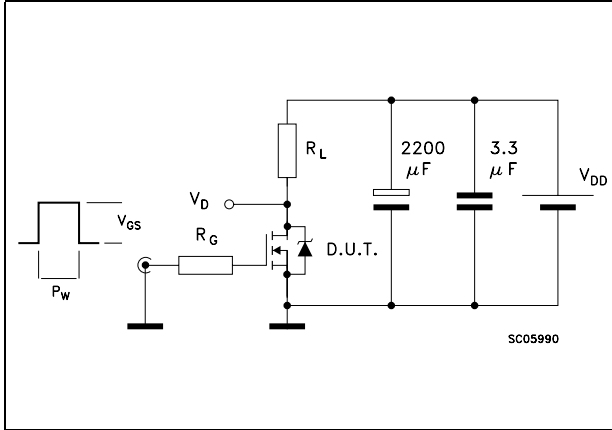


Figure 14. Gate charge test circuit

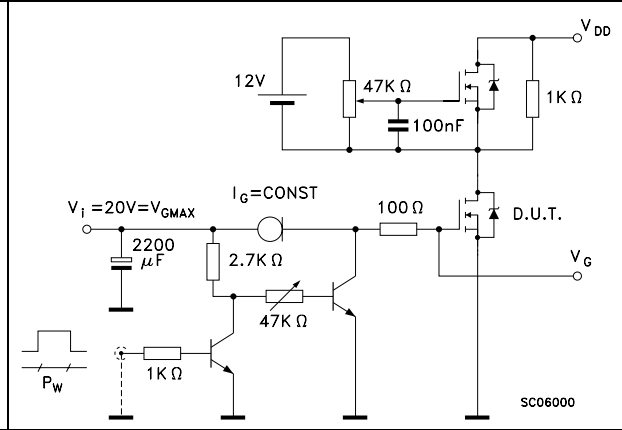


Figure 15. Test circuit for inductive load switching and diode recovery times

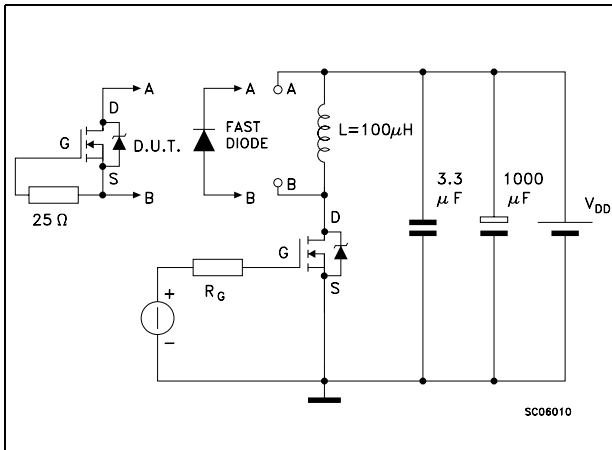


Figure 16. Unclamped Inductive load test circuit

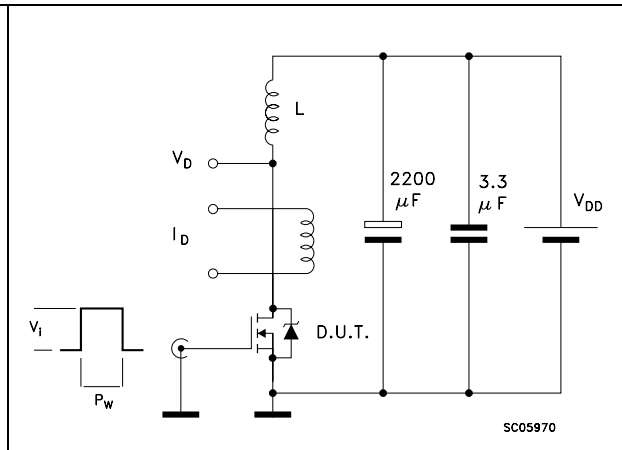


Figure 17. Unclamped inductive waveform

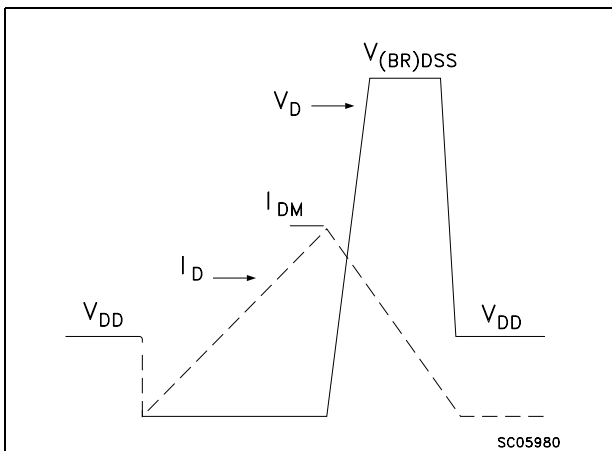


Figure 18. Switching time waveform

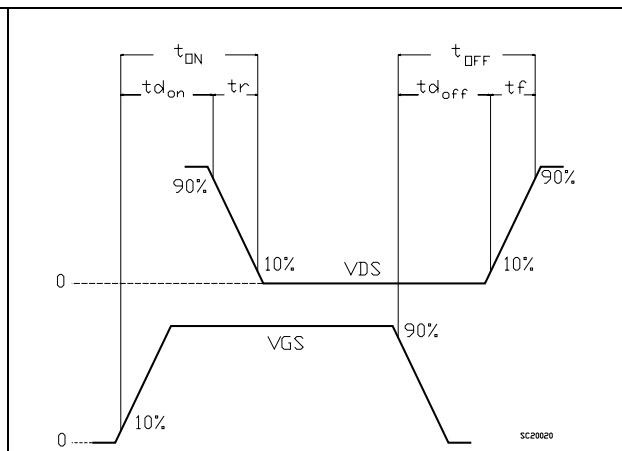
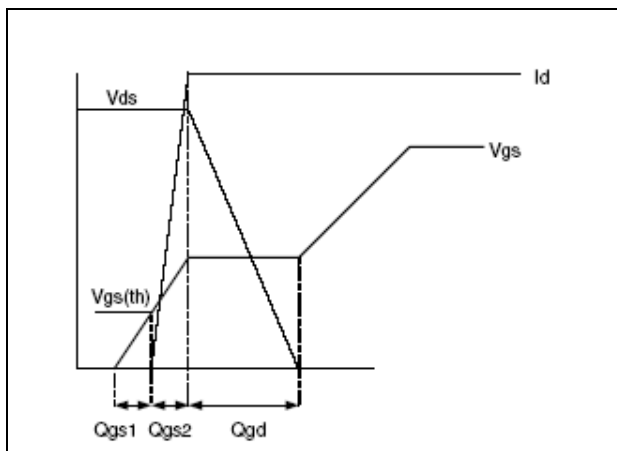


Figure 19. Gate charge waveform

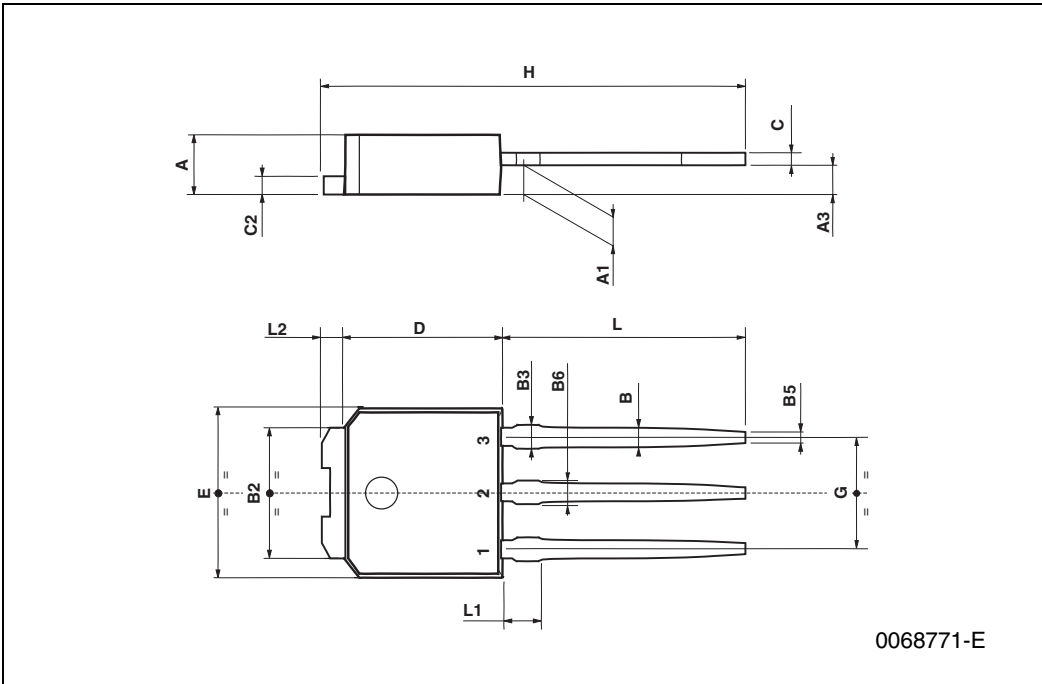


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

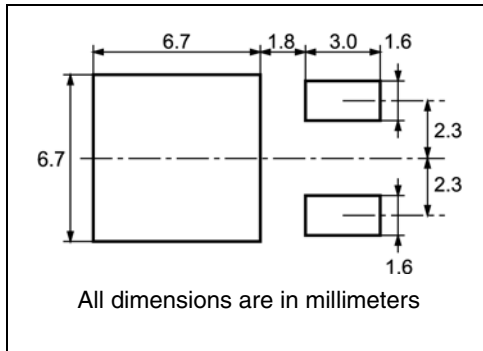
TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

TOP COVER TAPE

User Direction of Feed

Center line of cavity

Bending radius R min.

FEED DIRECTION

For machine ref. only including draft and radii concentric around B0

10 pitches cumulative tolerance on tape +/- 0.2 mm

6 Revision history

Table 8. Document revision history

Date	Revision	Changes
19-Oct-2007	1	First release
23-Sep-2008	2	V_{GS} value has been changed on Table 2 and Table 5

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