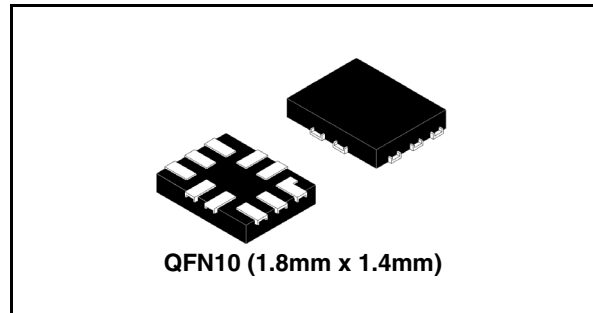


Low voltage high bandwidth dual SPDT switch

Features

- Ultra low power dissipation:
 - $I_{CC} = 0.2\mu\text{A}$ (Max.) at $T_A = 85^\circ\text{C}$
- Low “ON” resistance:
 - $R_{ON} = 4.6\Omega$ ($T_A = 25^\circ\text{C}$) at $V_{CC} = 4.3\text{V}$
 - $R_{ON} = 5.8\Omega$ ($T_A = 25^\circ\text{C}$) at $V_{CC} = 3.0\text{V}$
- Wide operating voltage range:
 - V_{CC} (Opr) = 1.65V to 4.3V single supply
- 4.3V tolerant and 1.8V compatible threshold on digital control input at $V_{CC} = 2.3\text{V}$ to 3.0V
- Typical bandwidth (-3dB) at 800MHz on all channels
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD performance exceeds JESD22
 - 2000-V Human body model (A114-A)
- USB (2.0) High speed (480Mbps) signal switching compliant



Description

The STG3682 is a high-speed CMOS low voltage dual analog S.P.D.T. (Single Pole Dual Throw) Switch or 2:1 Multiplexer /Demultiplexer Switch fabricated in silicon gate C²MOS technology. It is designed to operate from 1.65V to 4.3V, making this device ideal for portable applications.

The nSEL inputs are provided to control the switch. The switch S1 is ON (they are connected to common Ports Dn) when the nSEL input is held high and OFF (high impedance state exists between the two ports) when SEL is held low; the switch S2 is ON (it is connected to common Port D) when the nSEL input is held low and OFF (high impedance state exists between the two ports) when nSEL is held high.

Additional key features are fast switching speed, Break Before Make Delay Time and Ultra Low Power Consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Table 1. Device summary

Order code	Package	Packaging
STG3682QTR	QFN10 (1.8mm x 1.4mm)	Tape and reel

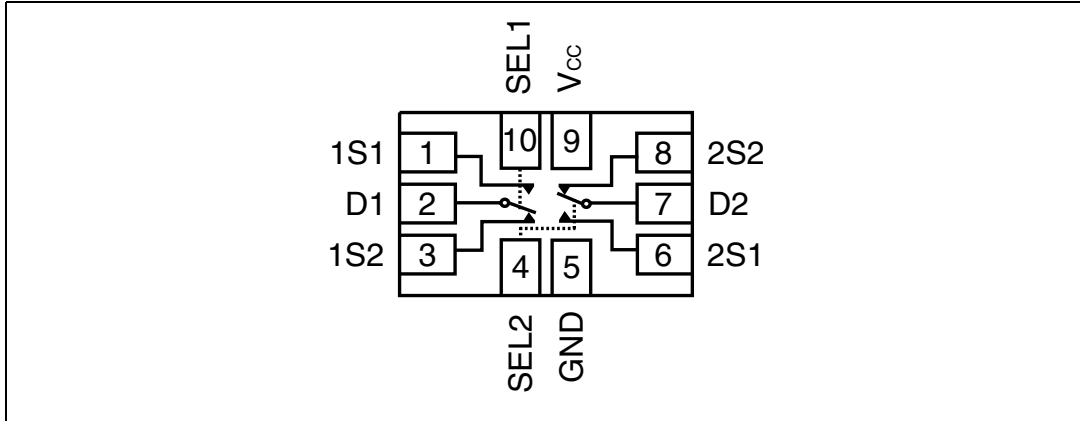
Contents

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1 Pin settings

1.1 Pin connection

Figure 1. Pin connection (top through view)



1.2 Pin description

Table 2. Pin description

Pin N°	Symbol	Name and function
1,3,6,8	1S1, 1S2, 2S1, 2S2	Independent channels
2,7	D1,D2	Common channels
10,4	SEL1,SEL2	Control
9	VCC	Positive supply voltage
5	GND	Ground (0V)

Note: Exposed pad must be soldered to a floating plane. Do NOT connect to power or ground.

2 Device summary

Figure 2. Input equivalent circuit

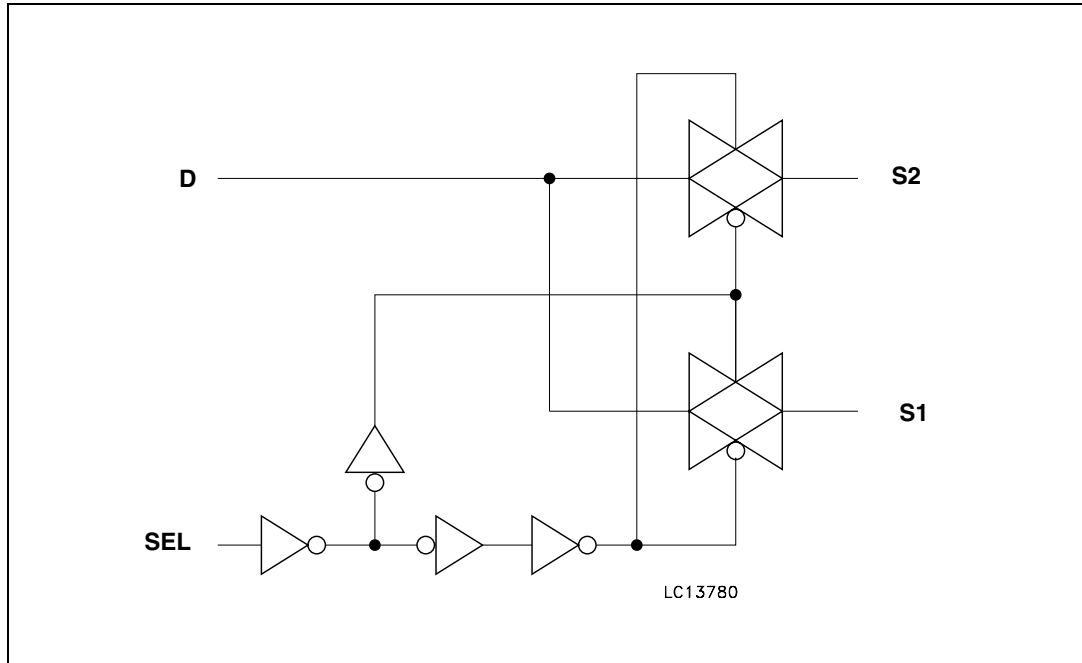


Table 3. Truth table

SEL	Switch S1	Switch S2
H	ON	OFF ⁽¹⁾
L	OFF ⁽¹⁾	ON

1. High impedance

3 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to $V_{CC} + 0.5$	V
V_{IC}	DC control input voltage	-0.5 to 5.5	V
V_O	DC output voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IKC}	DC input diode current on control pin ($V_{SEL} < 0V$)	-50	mA
I_{IK}	DC input diode current ($V_{SEL} < 0V$)	± 50	mA
I_{OK}	DC output diode current	± 20	mA
I_O	DC output current	± 128	mA
I_{OP}	DC output current peak (pulse at 1ms, 10% duty cycle)	± 300	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	± 100	mA
P_D	Power dissipation at $T_A = 70^\circ C$ ⁽¹⁾	1120	mW
T_{stg}	Storage temperature	-65 to 150	$^\circ C$
T_L	Lead temperature (10 sec)	300	$^\circ C$

1. Derate above 70°C by 18.5mW/C

3.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	1.65 to 4.3	V
V_I	Input voltage	0 to V_{CC}	V
V_{IC}	Control input voltage	0 to 4.3	V
V_O	Output voltage	0 to V_{CC}	V
T_{op}	Operating temperature	-40 to 85	$^\circ C$
dt/dv	Input rise and fall time control input	$V_{CC} = 1.65V$ to $2.7V$	0 to 20
		$V_{CC} = 3.0$ to $4.3V$	0 to 10
			ns/V

1. Truth Table guaranteed: 1.2V to 4.3V

4 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	Test conditions		Value					Unit
				T _A = 25°C			-40 to 85°C		
		V _{CC} (V)		Min	Typ	Max	Min	Max	
V _{IH}	High level input voltage	1.65 -1.95		0.65V _{CC}			0.65V _{CC}		V
		2.3-2.5		1.2			1.2		
		2.7-3.0		1.3			1.3		
		3.3-3.6		1.4			1.4		
		4.3		1.6			1.6		
V _{IL}	Low level input voltage	1.65-1.95				0.25			V
		2.3-2.5				0.25			
		2.7-3.0				0.25			
		3.3-3.6				0.30			
		4.3				0.40			
R _{PEAK}	Switch ON peak resistance	1.8	V _S = 0V to V _{CC} I _S = 8mA		12.0	16.0			Ω
		2.7			6.3	8.0			
		3.0			5.8	7.5			
		3.7			5.0	6.5			
		4.3			4.6	6.0			
R _{ON}	Switch On resistance	3.0	V _S = 3V I _S = 8mA		4.0	5.2			Ω
		3.0	V _S = 0.8V I _S = 8mA		5.0	6.5			
ΔR _{ON}	ON resistance match between channels ⁽¹⁾	1.8	V _S @ R _{ON} Max I _S = 8mA						Ω
		2.7							
		3.0			0.3				
		3.7							
		4.3							
R _{FLAT}	ON resistance flatness ⁽²⁾	1.8	V _S = 0V to V _{CC} I _S = 8mA		6.6				Ω
		2.7			2.0				
		3.0			1.7				
		3.7			1.5				
		4.3			1.6				
I _{OFF}	OFF state leakage current (SN), (D)	4.3	V _S = 0.3 or 4V			±20		±100	nA

Table 6. DC specifications

Symbol	Parameter	Test conditions		Value					Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
I _{IN}	Input leakage current	0 to 4.3	V _{SEL} = 0 to 4.3V			±0.1		±1	μA
I _{CC}	Quiescent supply current	1.65 to 4.3	V _{SEL} = V _{CC} or GND			±0.1		±1.0	μA
I _{CCLV}	Quiescent supply current low voltage driving	4.3	V _{1-2SEL} , V _{3-4SEL} = 1.65V		±37	±50		±100	μA
			V _{1-2SEL} , V _{3-4SEL} = 1.80V		±33	±40		±50	
			V _{1-2SEL} , V _{3-4SEL} = 2.60V		±11	±20		±30	

- Note 1: $\Delta R_{on} = \max |mSN - nSNI|$, where $m = 1..4$ and $n = 1..4$, $N = 1..2$
- Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 7. AC electrical characteristics ($C_L = 35\text{pF}$, $R_L = 50\Omega$, $t_r = t_f \leq 5\text{ns}$)

Symbol	Parameter	Test conditions		Value					Unit
		Vcc (V)		T _A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation delay	1.65-1.95			0.30				ns
		2.3-2.7			0.30				
		3.0-3.3			0.25				
		3.6-4.3			0.25				
t _{ON}	Turn-ON time	1.65-1.95	V _S = 0.8V		31				ns
		2.3-2.7	V _S = 1.5V		20	26		34	
		3.0-3.3			15	20		26	
		3.6-4.3			12	15		20	
t _{OFF}	Turn-OFF time	1.65-1.95	V _S = 0.8		22				ns
		2.3-2.7	V _S = 1.5V		14	18		23	
		3.0-3.3			11	14		18	
		3.6-4.3			10	13		17	
t _D	Break before make time delay	1.65-1.95	C _L = 35pF R _L = 50Ω V _S = 1.5V	1	7				ns
		2.3-2.7		1	5				
		3.0-3.3		1	4				
		3.6-4.3		1	3				
Q	Charge injection	1.65	C _L = 100pF V _{GEN} = 0V R _{GEN} = 0Ω		2.8				pC
		2.3			3.5				
		3.0			3.8				
		4.3			5.0				

Table 8. Analog switch characteristics ($C_L = 5\text{pF}$, $R_L = 50\Omega$, $T_A = 25^\circ\text{C}$)

Symbol	Parameter	Test conditions		Value					Unit
		Vcc (V)		T _A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
OIRR	OFF Isolation ⁽¹⁾	1.65 - 4.3	$V_S = 1V_{RMS}$, $f = 1\text{MHz}$ Signal = 0 dBm		-79				dB
			$V_S = 1V_{RMS}$, $f = 10\text{MHz}$ Signal = 0 dBm		-60				
Xtalk	Crosstalk	1.65 - 4.3	$V_S = 1V_{RMS}$, $f = 1\text{MHz}$ Signal = 0 dBm		-78				dB
			$V_S = 1V_{RMS}$, $f = 10\text{MHz}$ Signal = 0 dBm		-61				
BW	-3dB bandwidth	3.0 - 4.3	$R_L = 50\Omega$ Signal = 0dBm		800				MHz
D _G	Differential gain	3.0 - 4.3	$R_L = 150\Omega$		0.64				%
D _P	Differential phase	3.0 - 4.3	$R_L = 150\Omega$		0.1				deg
C _{IN}	Control pin input capacitance		$V_{CC} = 0V$		6.2				pF
C _{ON}	Sn Port capacitance when switch is enabled	3.3	$f = 1\text{MHz}$		12				
C _{OFF}	Sn Port capacitance when switch is disabled	3.3	$f = 1\text{MHz}$		5				

1. Off Isolation = $20\text{Log}_{10}(V_D/V_S)$, V_D = output. V_S = input to off switch.

Table 9. USB related AC electrical characteristics

Symbol	Parameter	Test conditions		Value					Unit
		Vcc (V)		T _A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
t _{SK(0)}	Channel-to-channel skew	3.0 to 3.6	$C_L = 10\text{pF}$		26				ps
t _{SK(P)}	Skew of opposite transition of the same output	3.0 to 3.6	$C_L = 10\text{pF}$		60				ps
T _J	Total jitter	3.0 to 3.6	$R_L = 50\Omega$, $C_L = 10\text{pF}$, $t_R = t_F = 750\text{ps}$ at 480Mbps		130				ps

5 Test circuits

Figure 3. ON-resistance

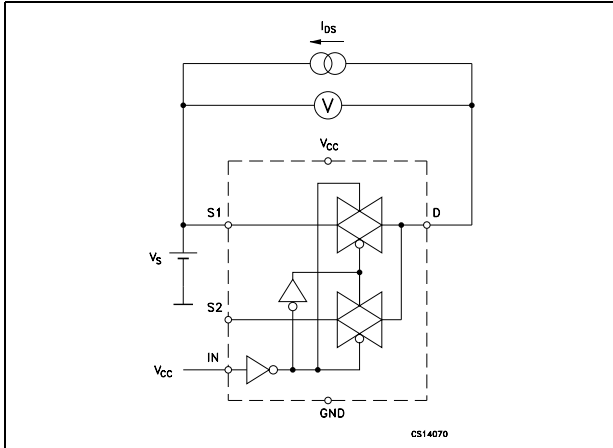


Figure 4. Bandwidth

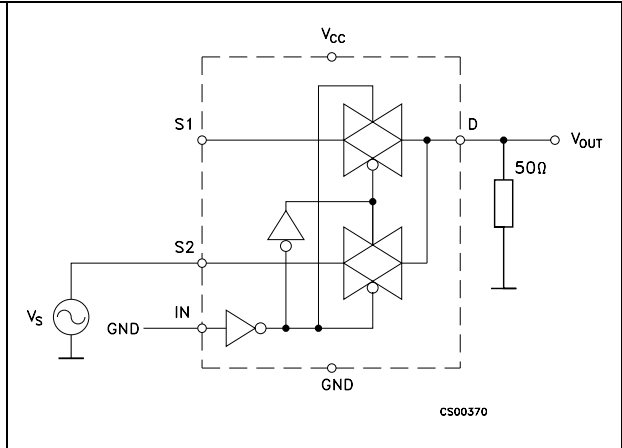


Figure 5. OFF leakage

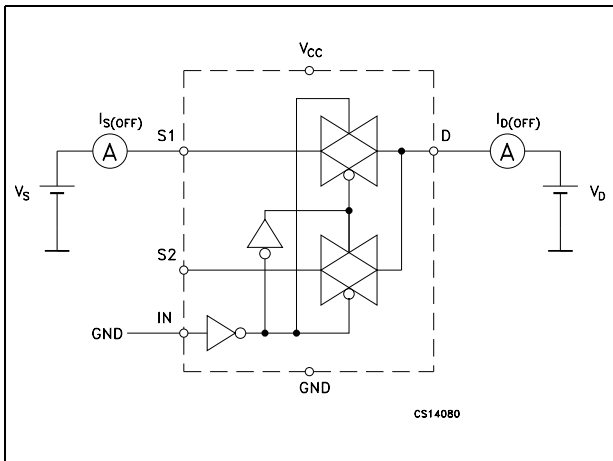


Figure 6. Channel to channel crosstalk

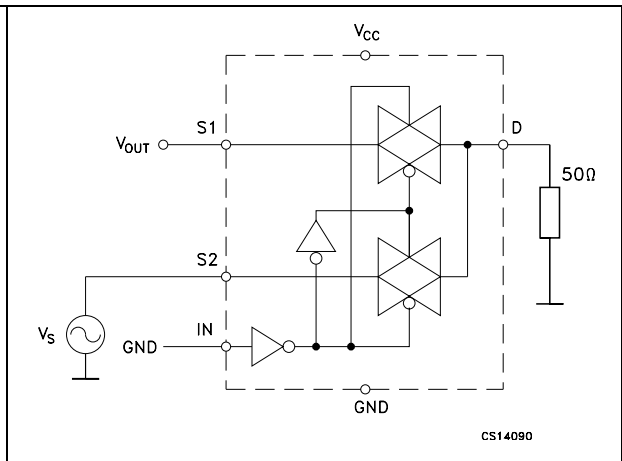


Figure 7. OFF isolation

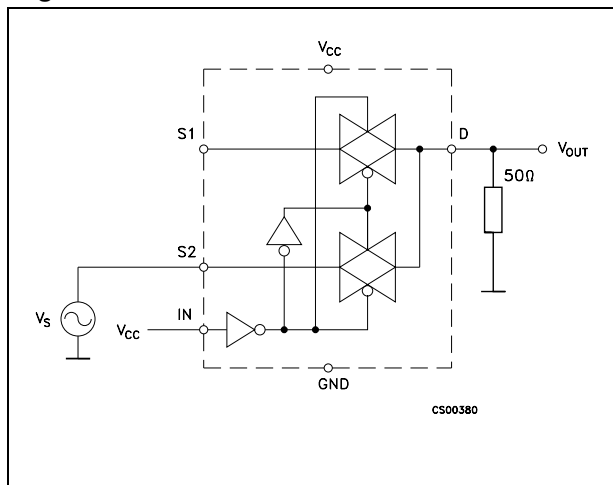
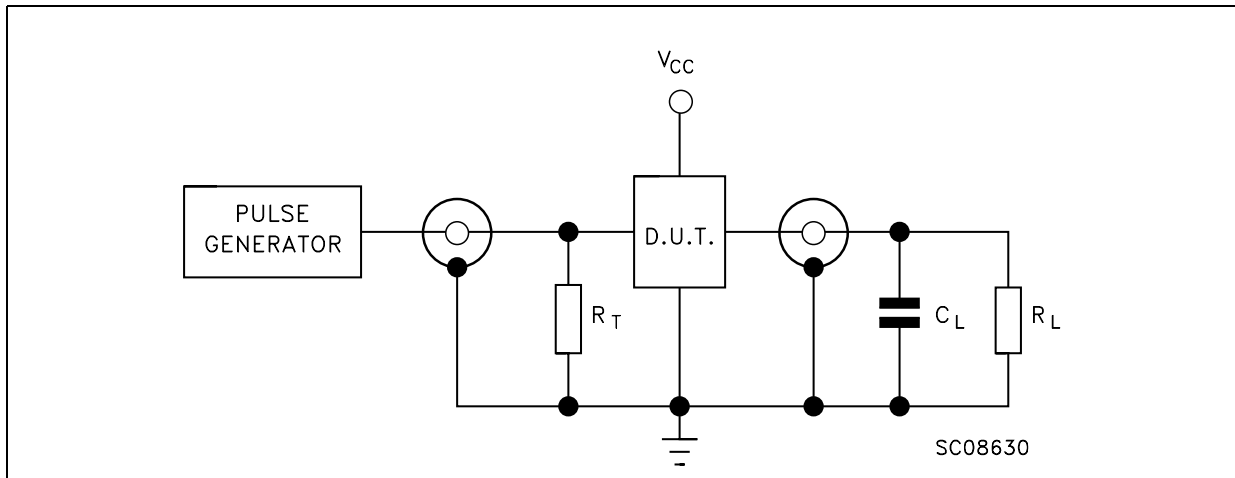


Figure 8. Test circuit



- Note: 1 $C_L = 5/35\text{pF}$ or equivalent: (includes jig capacitance)
2 $R_L = 50\Omega$ or equivalent
3 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 9. Break-before-make time delay

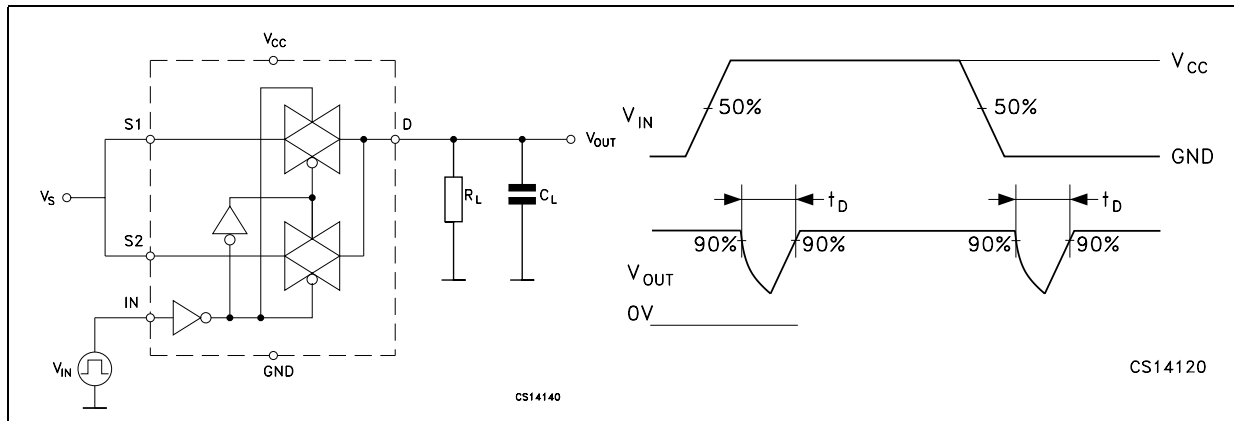


Figure 10. Switching time and charge injection
 ($V_{GEN} = 0V$, $R_{GEN} = 0\Omega$, $R_L = 1M\Omega$, $C_L = 100pF$)

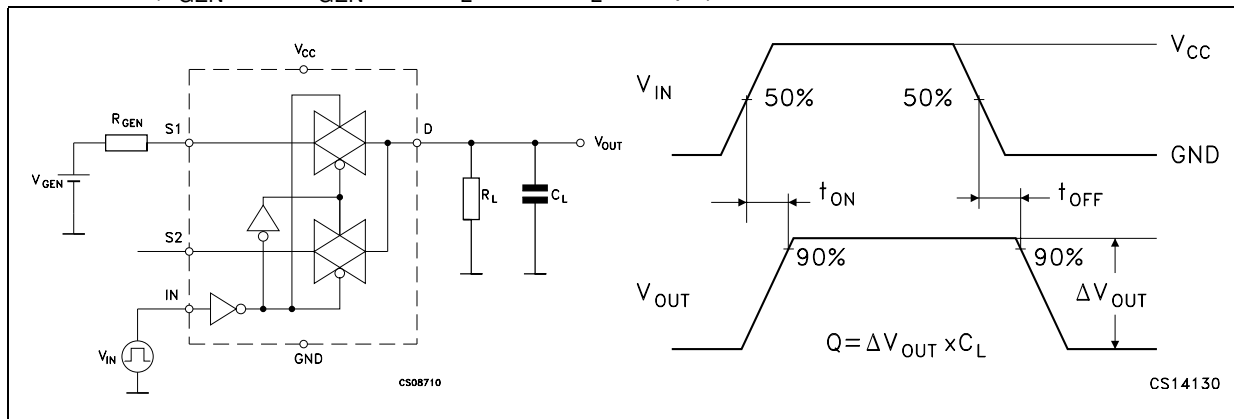
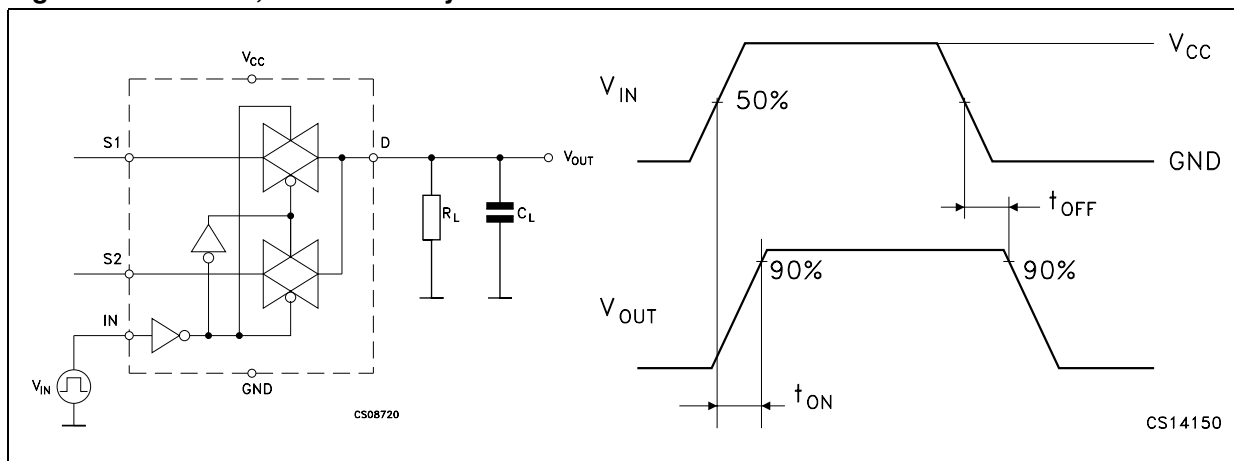


Figure 11. Turn ON, turn OFF delay time



6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 10. QFN10L(1.8x1.4) Mechanical data

ref.	mm			inch		
	Nom	Min	Max	Nom	Min	Max
A	0.50	0.45	0.55	0.020	0.017	0.021
A1	0.02	0	0.05	0.001	0	0.002
A3	0.127			0.005	0	0
b	0.20	0.15	0.25	0.007	0.006	0.010
D	1.80	1.70	1.90	0.070	0.066	0.074
E	1.40	1.30	1.50	0.055	0.051	0.059
e	0.40			0.015		
L	0.40	0.30	0.50	0.015	0.011	0.020

Figure 12. Package dimension

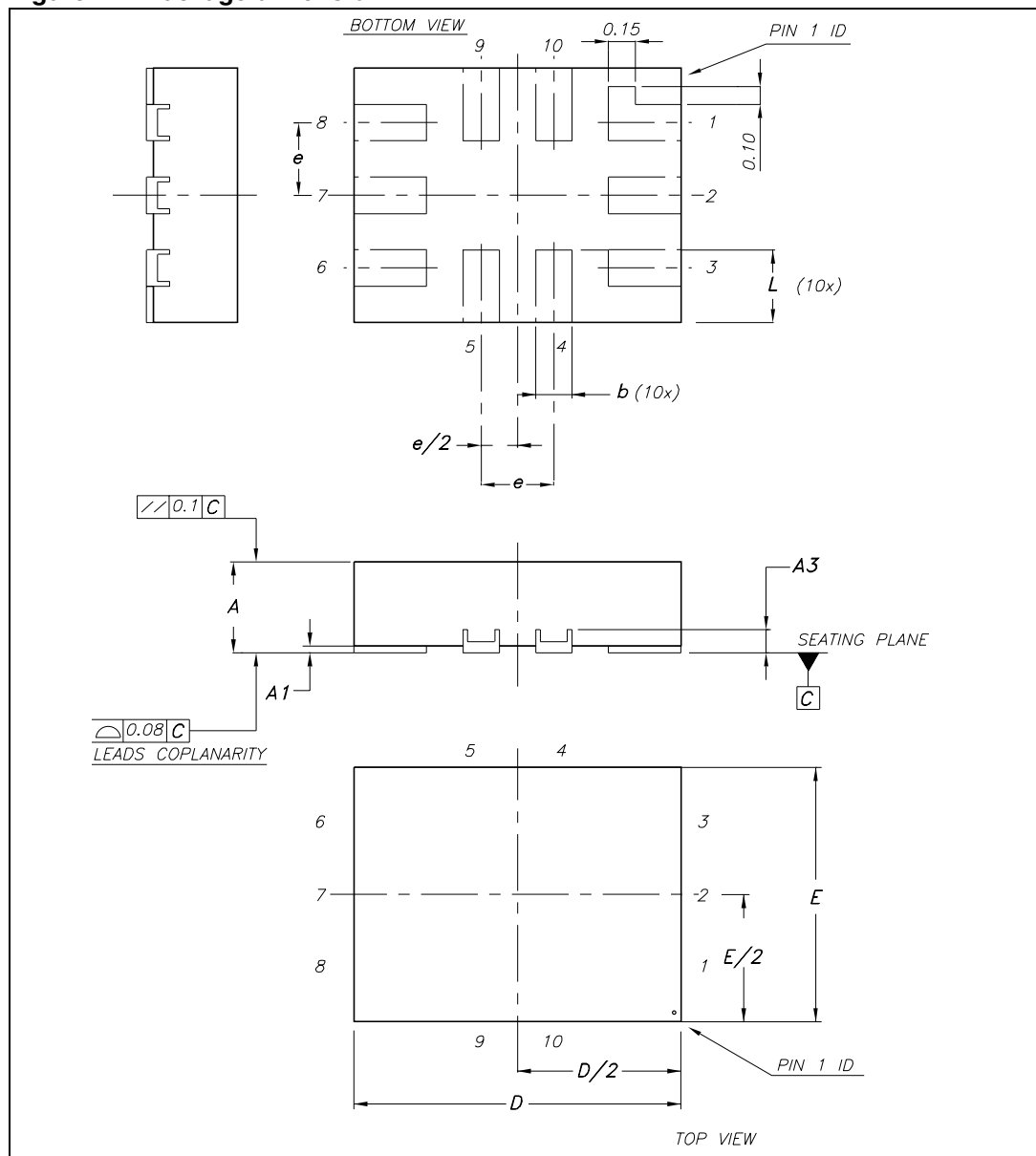


Figure 13. QFN10L (1.8mm x 1.4mm) foot print recommendation

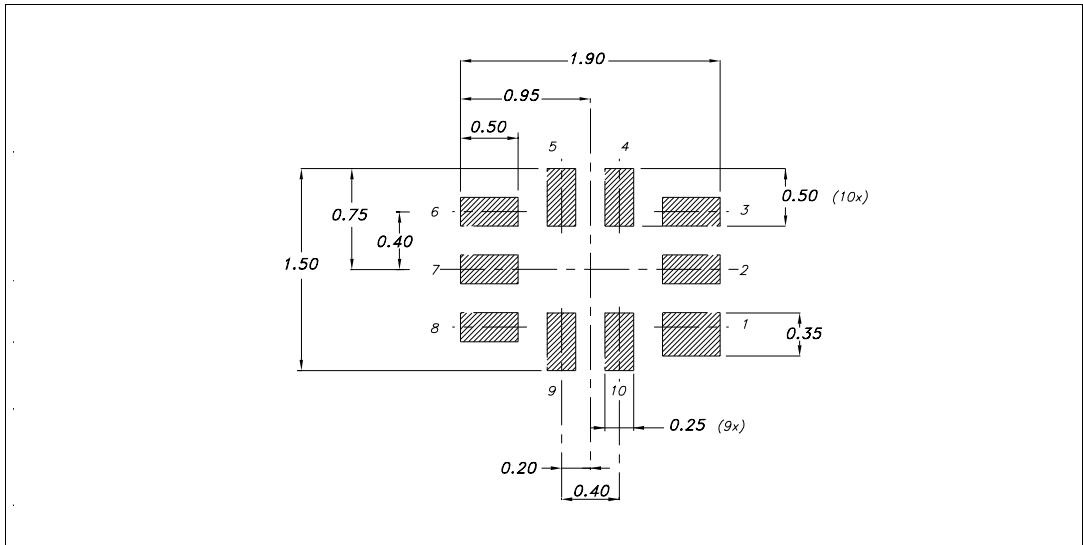


Figure 14. QFN10L (1.8mm x 1.4mm) carrier type

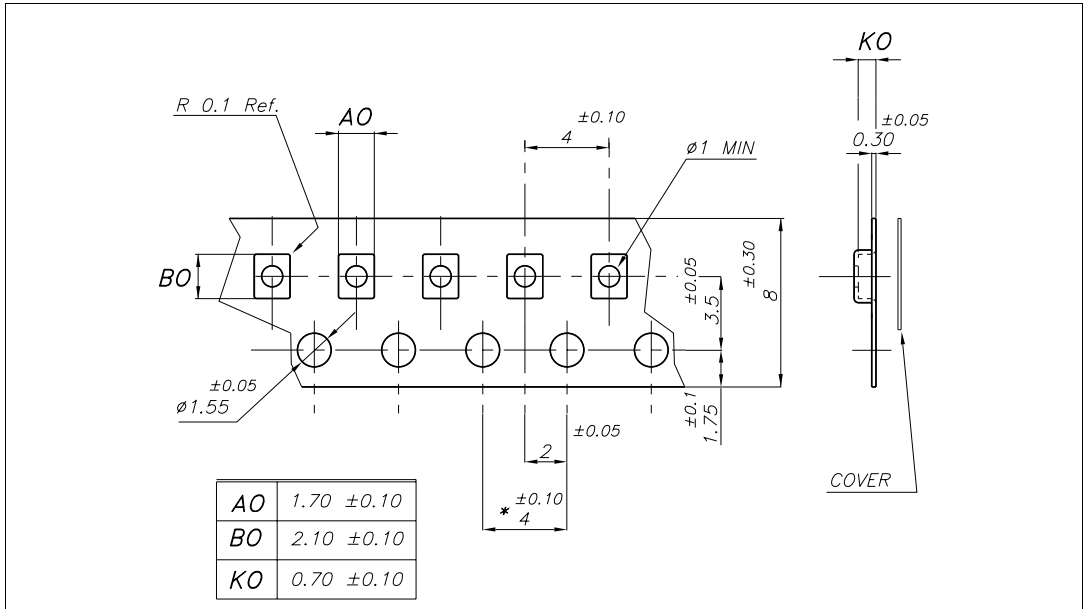
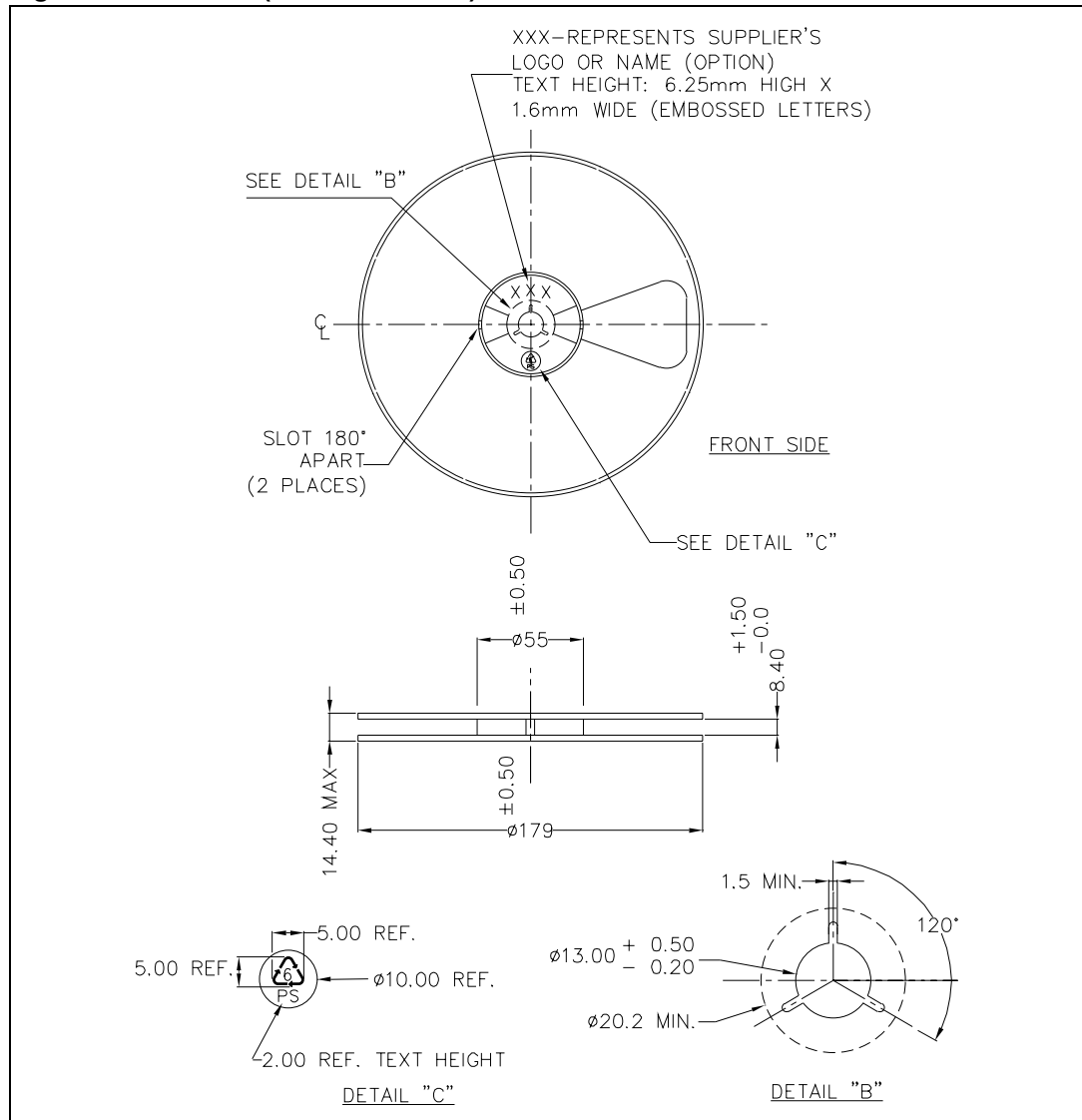


Figure 16. QFN10L(1.8mm x 1.4mm) reel information



7 Revision history

Table 11. Revision history

Date	Revision	Changes
08-Jan-2007	1	First release
03-Jul-2007	2	Updated C _{ON} , C _{OFF} Table 8 on page 9

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