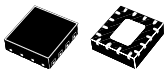
STG3684

LOW VOLTAGE 0.5Ω MAX DUAL SPDT SWITCH WITH BREAK BEFORE MAKE FEATURE

- HIGH SPEED:
  t_{PD} = 0.3ns (TYP.) at V_{CC} = 3.0V
  t_{PD} = 0.4ns (TYP.) at V_{CC} = 2.3V
- ULTRA LOW POWER DISSIPATION:
  I_{CC} = 0.2µA (MAX.) at T_A = 85°C
- LOW "ON" RESISTANCE V_{IN} = 0V:
  R_{ON} = 0.5Ω (MAX. T_A = 25°C) at V_{CC} = 2.7
  R_{ON} = 0.8Ω (MAX. T_A = 25°C) at V_{CC} = 2.3V
  R_{ON} = 3.0Ω (MAX. T_A = 25°C) at V_{CC} = 1.8V
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 1.65V to 4.3V SINGLE SUPPLY
- 4.3V TOLERANT AND 1.8V COMPATIBLE THRESHOLD ON DIGITAL CONTROL INPUT at V_{CC} = 2.3 to 3.0V
- LATCH-UP PERFORMANCE EXCEEDS 300mA (JESD 17)



QFN

ORDER CODES

PACKAGE	T & R
QFN	STG3684QTR

DESCRIPTION

The STG3684 is an high-speed CMOS DUAL ANALOG S.P.D.T. (Single Pole Dual Throw) SWITCH or DUAL 2:1 Multiplexer/Demultiplexer Bus Switch fabricated in silicon gate C^2MOS technology. It is designed to operate from 1.65V to 4.3V, making this device ideal for portable applications.

It offers very low ON-Resistance (<0.5Ω) at V_{CC}=3.0V. The nIN inputs are provided to control the switches. The switches nS1 are ON (they are connected to common Ports Dn) when the nIN input is held high and OFF (high impedance state exists between the two ports) when nIN is held low; the switches nS2 are ON (they are connected to common Ports Dn) when the nIN input is held low and OFF (high impedance state exists between the two ports) when IN is held high. Additional key features are fast switching speed, Break Before Make Delay Time and Ultra Low Power Consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage. It's available in the commercial temperature range in the QFN package.

PIN CONNECTION

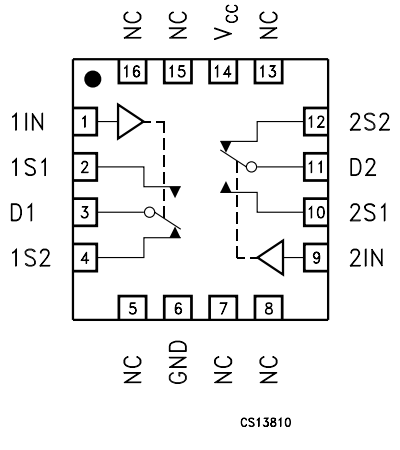


Figure 1: Input Equivalent Circuit

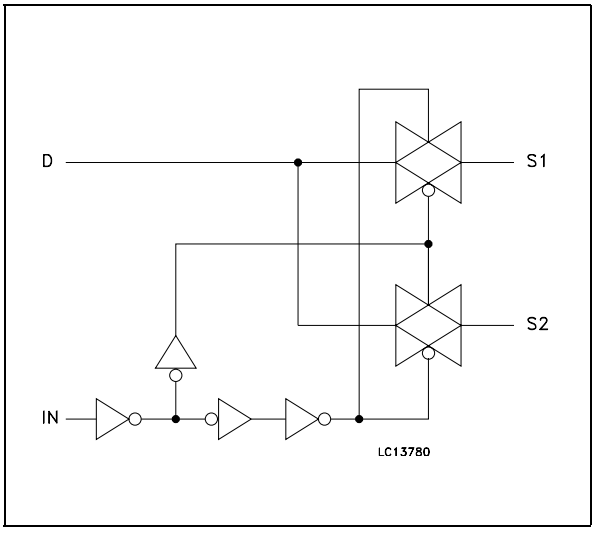


Table 1: Pin Description

QFN PIN N°	SYMBOL	NAME AND FUNCTION
1, 9	1IN, 2IN	Controls
2, 10 4, 12	1S1 to 2S1 1S2 to 2S2	Independent Channels
3, 11	D1, D2	Common Channels
5,7,8,13,15,16	NC	Not Connected
6	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

Table 2: Truth Table

IN	SWITCH S1	SWITCH S2
H	ON	OFF(*)
L	OFF(*)	ON

(*) High Impedance

Table 3: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 4.6	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_{IC}	DC Control Input Voltage	-0.5 to 4.6	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IKC}	DC Input Diode Current on control pin (V_{IN} < 0V)	– 50	mA
I_{IK}	DC Input Diode Current (V_{IN} < 0V)	± 50	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 300	mA
I_{OP}	DC Output Current Peak (pulse at 1ms, 10% duty cycle)	± 500	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 100	mA
P_D	Power Dissipation at T_a=70°C (1)	1120	mW
T_{stg}	Storage Temperature	-65 to 150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
(1) Derate above 70°C: by 18.5mW/°C.

Table 4: Recommended Operating Conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage (note 1)		1.65 to 4.3	V
V_I	Input Voltage		0 to V_{CC}	V
V_{IC}	Control Input Voltage		0 to 4.3	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
dt/dv	Input Rise and Fall Time Control Input	V_{CC}= 1.65V to 2.7V	0 to 20	ns/V
		V_{CC}= 3.0V to 4.3V	0 to 10	

1) Truth Table guaranteed: 1.2V to 4.3V.

Table 5: DC Specifications

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	1.65-1.95		0.65V_{CC}			0.65V_{CC}		0.65V_{CC}		V
		2.3-2.5		1.4			1.4		1.4		
		2.7-3.0		1.4			1.4		1.4		
		3.3		1.5			1.5		1.5		
		3.6		1.7			1.7		1.7		
		4.3		2.2			2.2		2.2		
V_{IL}	Low Level Input Voltage	1.65-1.95				0.40		0.40		0.40	V
		2.3-2.5				0.50		0.50		0.50	
		2.7-3.6				0.50		0.50		0.50	
		3.3				0.50		0.50		0.50	
		3.6				0.50		0.50		0.50	
		4.3				1.3		1.3		1.3	
R_{ON}	Switch ON Resistance (1)	4.3	V_S=0V to V_{CC} I_S=100mA		0.40	0.50		0.50			Ω
		3.0			0.40	0.50		0.60			
		2.7			0.40	0.50		0.60			
		2.3			0.50	0.80		0.80			
		1.8			0.70	3.0		4.0			
		1.65			0.80	3.0		4.0			
ΔR_{ON}	ON Resistance Match between channels (1,2)	2.7	V_S=1.5V I_S=100mA		0.06						Ω
R_{FLAT}	ON Resistance FLATNESS (3)	4.3	V_S=1.5V I_S=100mA								Ω
		3.0									
		2.7			0.07	0.15		0.15			
		2.3									
		1.65	V_S=0.8V I_S=100mA								
I_{OFF}	OFF State Leakage Current (nSn), (Dn)	4.3	V_S=0.3 or 4V			±10		± 100			nA
I_{IN}	Input Leakage Current	0 - 4.3	V_{IN}= 0 to 4.3V			±0.1		± 1			µA
I_{CC}	Quiescent Supply Current (1)	1.65-4.3	V_{IN}=V_{CC} or GND			±0.05		±0.2		±1	µA

Note 1: Guaranteed by design
Note 2: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.
Note 3: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 6: AC Electrical Characteristics (C_L = 35pF, R_L = 50Ω, $t_r = t_f \leq$ 5ns)

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay	1.65-1.95	V_I=OPEN		0.45						ns
		2.3-2.7			0.40						
		3.0-3.6			0.30						
		3.6-4.3			0.30						
t_{ON}	TURN-ON time	1.65-1.95	V_S=0.8V		70						ns
		2.3-2.7	V_S=1.5V		30	50		60			
		3.0-3.6	V_S=1.5V		30	50		60			
		3.6-4.3	V_S=1.5V		30	50		60			
t_{OFF}	TURN-OFF time	1.65-1.95	V_S=0.8V		45						ns
		2.3-2.7	V_S=1.5V		25	30		40			
		3.0-3.6	V_S=1.5V		25	30		40			
		3.6-4.3	V_S=1.5V		25	30		40			
t_D	Break Before Make Time Delay	1.65-1.95	C_L=35pF, R_L= 50Ω, V_S=1.5V								ns
		2.3-2.7		2	15						
		3.0-3.6		2	15						
		3.6-4.3		2	15						
Q	Charge injection	1.65-1.95	C_L= 100pF, R_L= 1MΩ, V_{GEN}= 0V, R_{GEN}= 0Ω								pC
		2.3-2.7			200						
		3.0-3.6			200						
		3.6-4.3			200						

Table 7: Analog Switch Characteristics (C_L = 5pF, R_L = 50Ω, T_A = 25°C)

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
OIRR	Off Isolation (1)	1.65-4.3	V_S= 1V_{RMS} f= 100KHz		-64						dB
Xtalk	Crosstalk	1.65-4.3	V_S= 1V_{RMS} f= 100KHz		-54						dB
THD	Total Harmonic Distortion	2.3-4.3	R_L= 600Ω, V_{IN}= 2V_{PP}, f= 20Hz to 20kHz		0.03						%
BW	-3dB Bandwidth	1.65-4.3	R_L= 50Ω		50						MHz
C_{IN}	Control Pin Input Capacitance				5						pF
C_{Sn}	Sn Port Capacitance	3.3	f= 1MHz		37						
C_D	D Port Capacitance when Switch is Enabled	3.3	f= 1MHz		84						

Note 1: Off Isolation = 20Log_{10} (V_D/V_S), V_D = output. V_S = input at off switch

Figure 2: ON Resistance

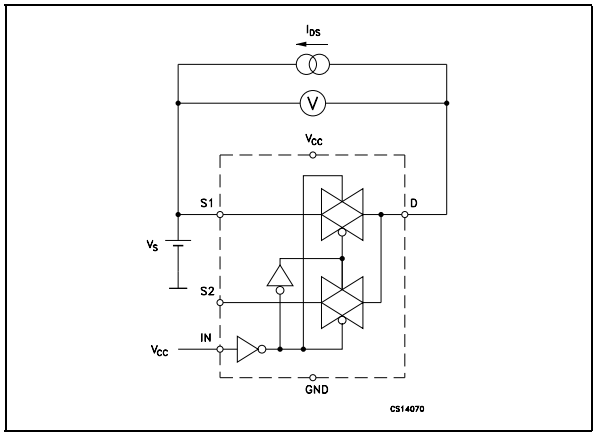
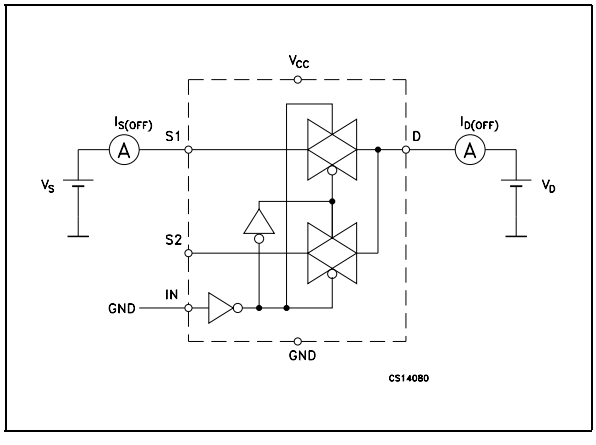


Figure 3: OFF Leakage



OFF Isolation

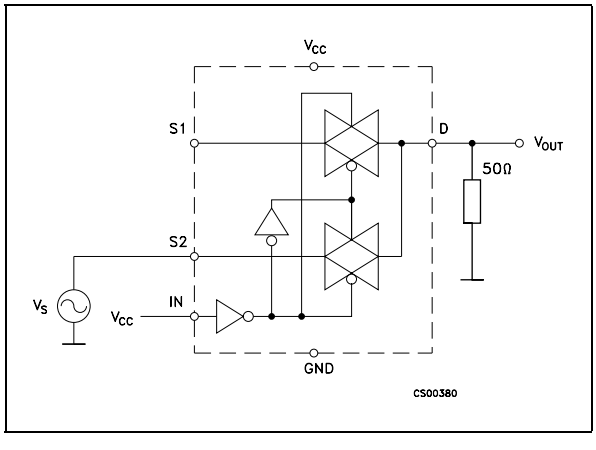


Figure 4: Bandwidth

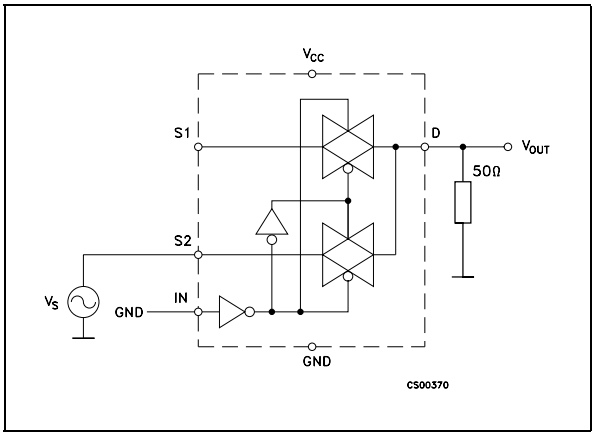


Figure 5: Channel To Channel Crosstalk

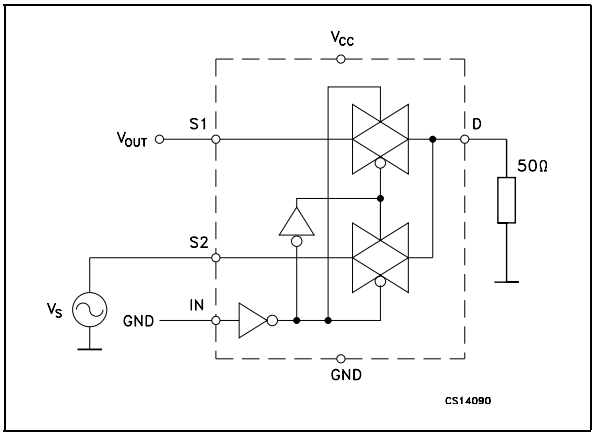
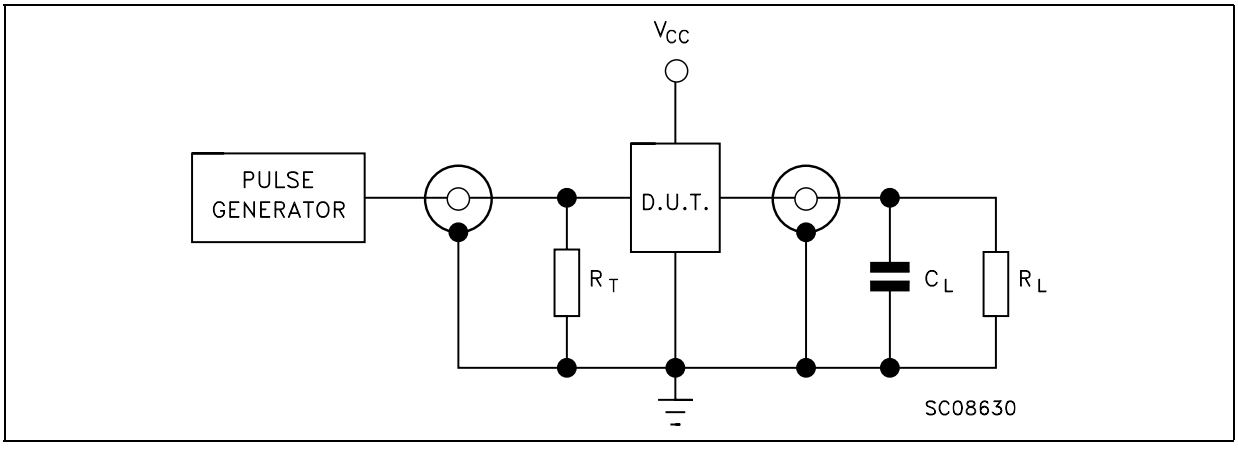


Table 8: Test Circuit



C_L = 5/35pF or equivalent (includes jig and probe capacitance)
R_L = 50Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 6: Break Before Make Time Delay

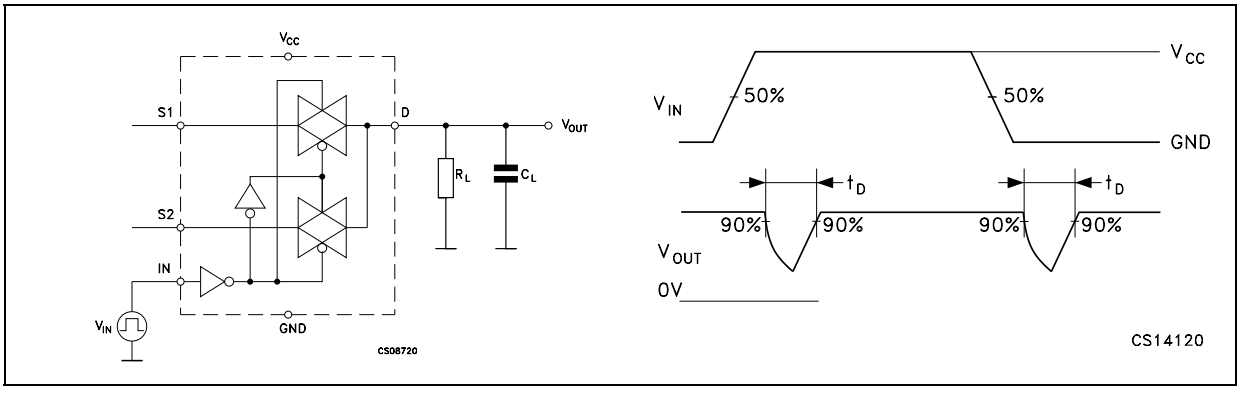


Figure 7: Charge Injection (V_{GEN}=0V, R_{GEN}=0Ω, R_L=1MΩ, C_L=100pF)

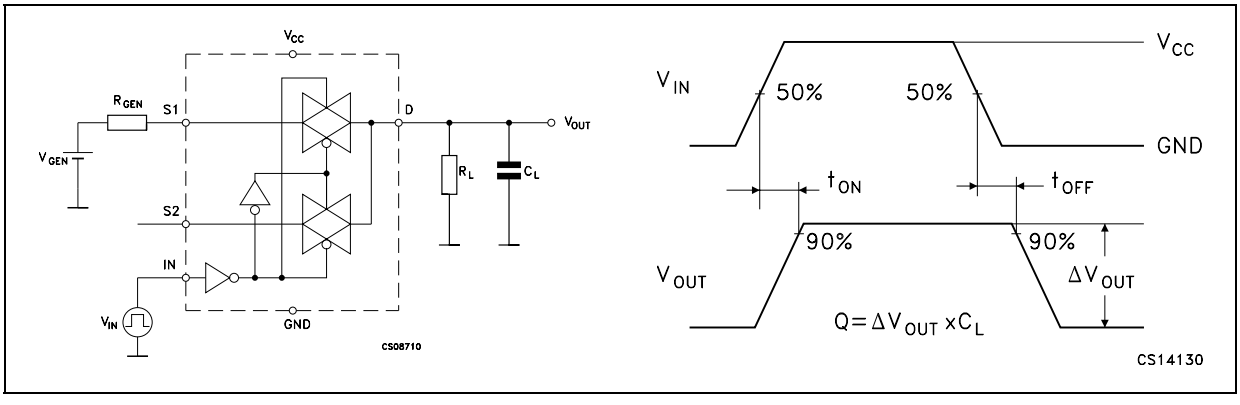
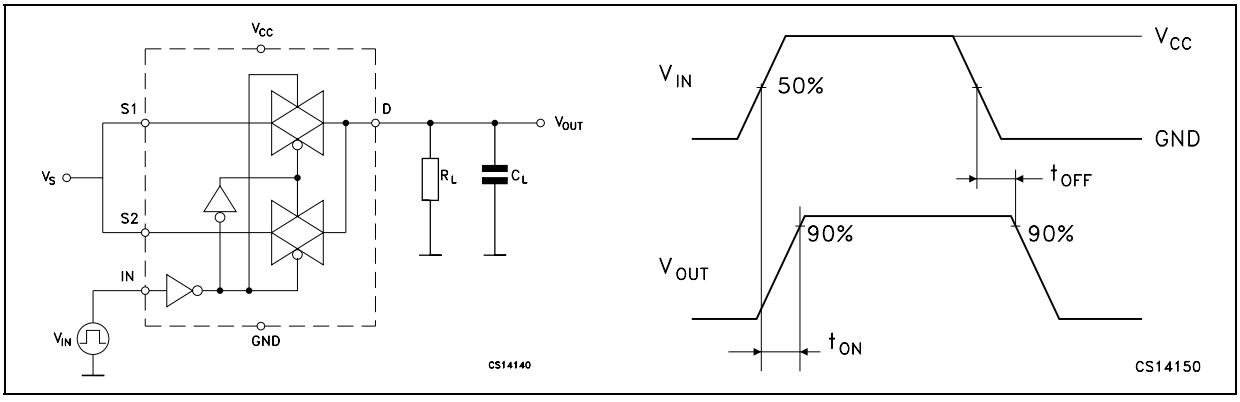
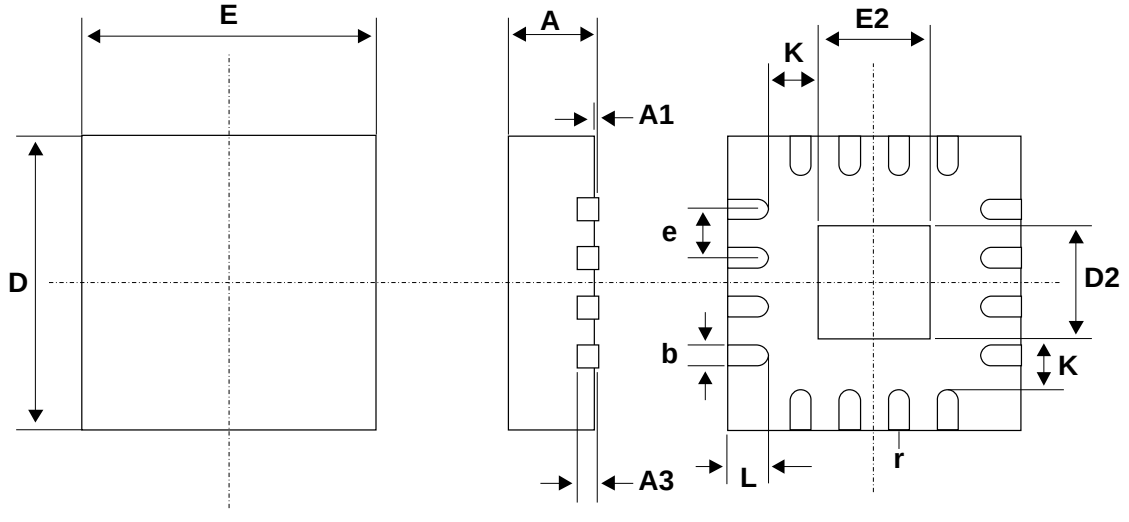


Table 9: Turn On, Turn Off Delay Time



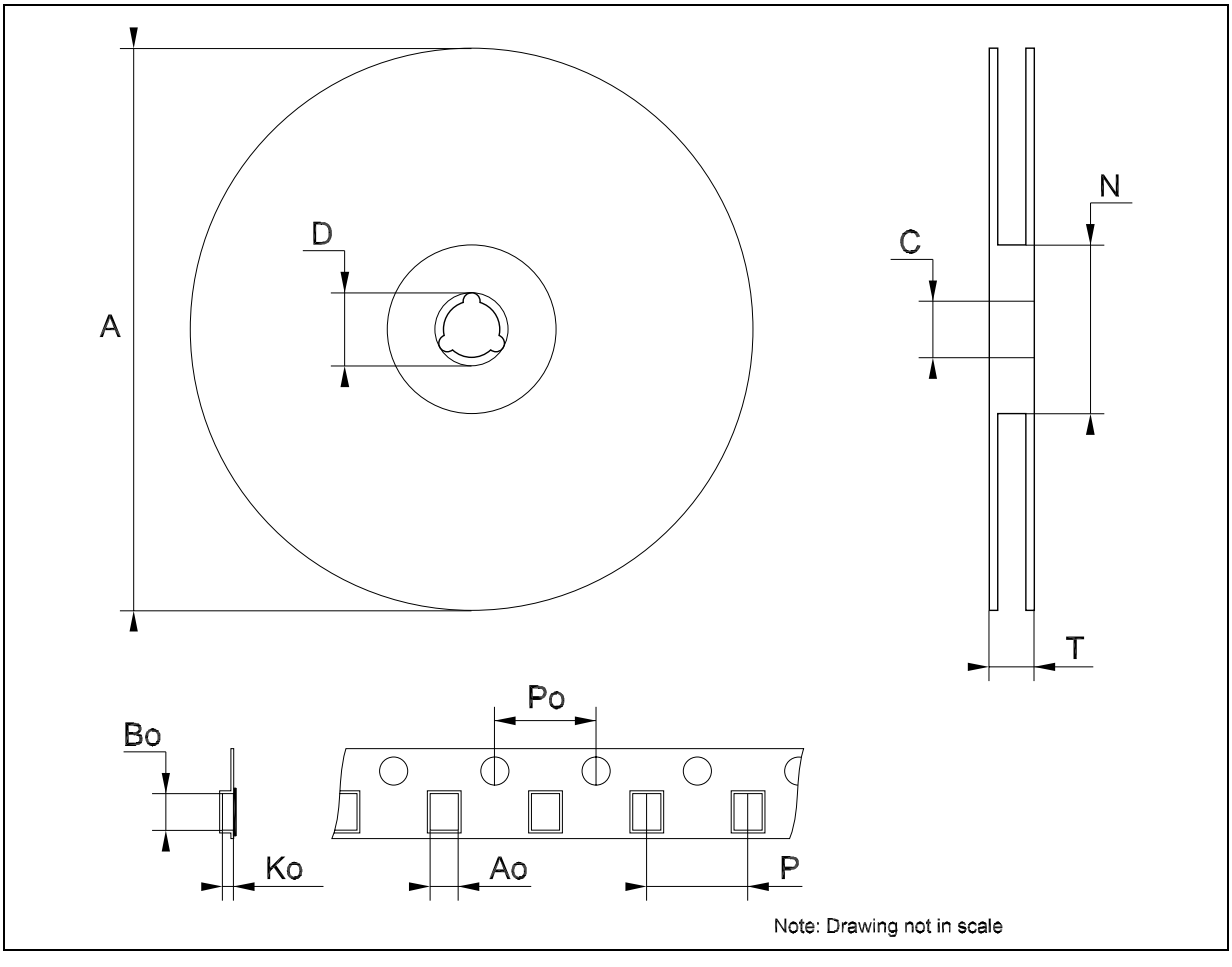
QFN16 (3x3) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	0.032	0.035	0.039
A1		0.02	0.05		0.001	0.002
A3		0.20			0.008	
b	0.18	0.25	0.30	0.007	0.010	0.012
D		3.00			0.118	
D2	1.55	1.70	1.80	0.061	0.067	0.071
E		3.00			0.118	
E2	1.55	1.70	1.80	0.061	0.067	0.071
e		0.50			0.020	
K		0.20			0.008	
L	0.30	0.40	0.50	0.012	0.016	0.020
r	0.09			0.006		



Tape & Reel QFNxx/DFNxx (3x3) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			18.4			0.724
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



Note: Drawing not in scale

Table 10: Revision History

Date	Revision	Description of Changes
18-May-2004	2	Characteristics at V_{CC} = 4.3 V Added on Tables 3, 4, 5, 6 and 7.