



# STK16C68

## 8K x 8 *AutoStorePlus*<sup>TM</sup> nvSRAM

### *QuantumTrap*<sup>TM</sup> CMOS

### Nonvolatile Static RAM

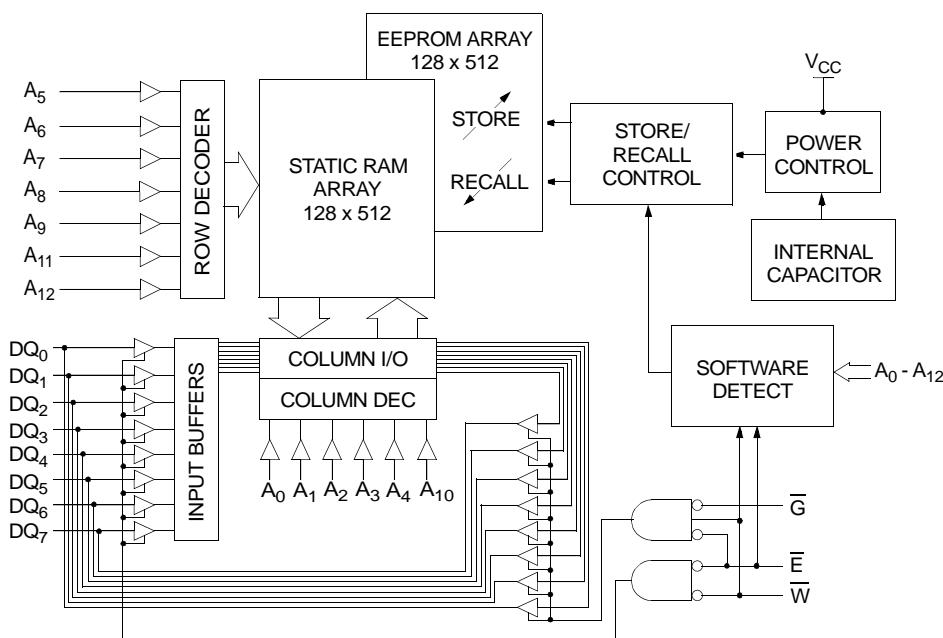
#### FEATURES

- Transparent Data Save on Power Down
- Internal Capacitor Guarantees *AutoStore*<sup>TM</sup> Regardless of Power-Down Slew Rate
- Nonvolatile Storage without Battery Problems
- Directly Replaces 8K x 8 Static RAM, Battery-Backed RAM or EEPROM
- 20ns, 25ns, 35ns and 45ns Access Times
- *STORE* to EEPROM Initiated by Software or *AutoStorePlus*<sup>TM</sup> on Power Down
- *RECALL* to SRAM Initiated by Software or Power Restore
- 10mA Typical  $I_{CC}$  at 200ns Cycle Time
- Unlimited READ, WRITE and *RECALL* Cycles
- 1,000,000 *STORE* Cycles to EEPROM
- 100-Year Data Retention over Full Industrial Temperature Range
- No Data Loss from Undershoot
- Commercial and Industrial Temperatures
- 28-Pin 600 mil PDIP and 350 mil SOIC Packages

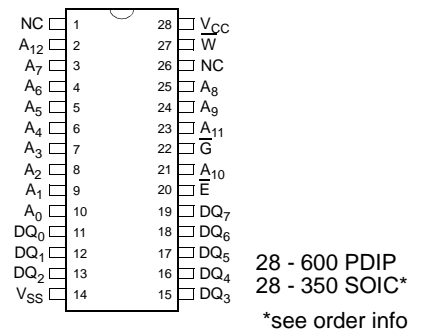
#### DESCRIPTION

The STK16C68 is a fast SRAM with a nonvolatile EEPROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the *STORE* operation) can take place automatically on power down. An internal capacitor guarantees the *STORE* operation regardless of power-down slew rate. Transfers from the EEPROM to the SRAM (the *RECALL* operation) take place automatically on restoration of power. Initiation of *STORE* and *RECALL* cycles can also be controlled by entering control sequences on the SRAM inputs. The STK16C68 is pin-compatible with 8k x 8 SRAMs and battery-backed SRAMs, allowing direct substitution while enhancing performance. The STK12C68, which uses an external capacitor, and the STK15C68, which uses charge stored in system capacitance, are alternatives for systems needing *AutoStore*<sup>TM</sup> operation.

#### BLOCK DIAGRAM



#### PIN CONFIGURATIONS



#### PIN NAMES

A <sub>0</sub> - A <sub>12</sub>	Address Inputs
$\bar{W}$	Write Enable
DQ <sub>0</sub> - DQ <sub>7</sub>	Data In/Out
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
V <sub>CC</sub>	Power (+ 5V)
V <sub>SS</sub>	Ground

**ABSOLUTE MAXIMUM RATINGS<sup>a</sup>**

Voltage on Input Relative to $V_{SS}$ . . . . .	-0.6V to ( $V_{CC} + 0.5V$ )
Voltage on $DQ_{0-7}$ . . . . .	-0.5V to ( $V_{CC} + 0.5V$ )
Temperature under Bias . . . . .	-55°C to 125°C
Storage Temperature . . . . .	-65°C to 150°C
Power Dissipation . . . . .	1W
DC Output Current (1 output at a time, 1s duration) . . . . .	15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC CHARACTERISTICS**

( $V_{CC} = 5.0V \pm 10%$ )<sup>b</sup>

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
$I_{CC1}$ <sup>c</sup>	Average $V_{CC}$ Current		100		N/A	mA	$t_{AVAV} = 20ns$ $t_{AVAV} = 25ns$ $t_{AVAV} = 35ns$ $t_{AVAV} = 45ns$
			90		90	mA	
			75		75	mA	
			65		65	mA	
$I_{CC2}$ <sup>d</sup>	Average $V_{CC}$ Current during <i>STORE</i>		3		3	mA	All Inputs Don't Care, $V_{CC} = max$
$I_{CC3}$ <sup>c</sup>	Average $V_{CC}$ Current at $t_{AVAV} = 200ns$ 5V, 25°C, Typical		10		10	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All Others Cycling, CMOS Levels
$I_{SB1}$ <sup>e</sup>	Average $V_{CC}$ Current (Standby, Cycling TTL Input Levels)		32		N/A	mA	$t_{AVAV} = 20ns, \overline{E} \geq V_{IH}$ $t_{AVAV} = 25ns, \overline{E} \geq V_{IH}$ $t_{AVAV} = 35ns, \overline{E} \geq V_{IH}$ $t_{AVAV} = 45ns, \overline{E} \geq V_{IH}$
			27		28	mA	
			23		24	mA	
			20		21	mA	
$I_{SB2}$ <sup>e</sup>	$V_{CC}$ Standby Current (Standby, Stable CMOS Input Levels)		1.5		1.5	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All Others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
$I_{ILK}$	Input Leakage Current		$\pm 1$		$\pm 1$	$\mu A$	$V_{CC} = max$ $V_{IN} = V_{SS}$ to $V_{CC}$
$I_{OLK}$	Off-State Output Leakage Current		$\pm 5$		$\pm 5$	$\mu A$	$V_{CC} = max$ $V_{IN} = V_{SS}$ to $V_{CC}$ , $\overline{E}$ or $\overline{G} \geq V_{IH}$
$V_{IH}$	Input Logic "1" Voltage	2.2	$V_{CC} + .5$	2.2	$V_{CC} + .5$	V	All Inputs
$V_{IL}$	Input Logic "0" Voltage	$V_{SS} - .5$	0.8	$V_{SS} - .5$	0.8	V	All Inputs
$V_{OH}$	Output Logic "1" Voltage	2.4		2.4		V	$I_{OUT} = -4mA$
$V_{OL}$	Output Logic "0" Voltage		0.4		0.4	V	$I_{OUT} = 8mA$
$T_A$	Operating Temperature	0	70	-40	85	°C	

Note b: The STK16C68-20 requires  $V_{CC} = 5.0V \pm 5%$  supply to operate at specified speed.  
 Note c:  $I_{CC1}$  and  $I_{CC3}$  are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.  
 Note d:  $I_{CC2}$  and  $I_{CC4}$  are the average currents required for the duration of the respective *STORE* cycles ( $t_{STORE}$ ).  
 Note e:  $\overline{E} \geq V_{IH}$  will not produce standby current levels until any nonvolatile cycle in progress has timed out.

**AC TEST CONDITIONS**

Input Pulse Levels . . . . .	0V to 3V
Input Rise and Fall Times . . . . .	$\leq 5ns$
Input and Output Timing Reference Levels . . . . .	1.5V
Output Load . . . . .	See Figure 1

**CAPACITANCE<sup>f</sup>** ( $T_A = 25^\circ C, f = 1.0MHz$ )

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
$C_{IN}$	Input Capacitance	8	pF	$\Delta V = 0$ to 3V
$C_{OUT}$	Output Capacitance	7	pF	$\Delta V = 0$ to 3V

Note f: These parameters are guaranteed but not tested.

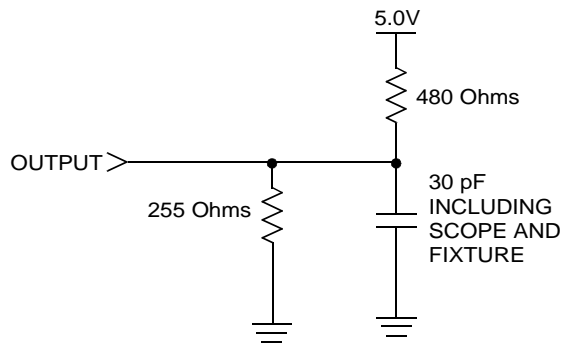


Figure 1: AC Output Loading

SRAM READ CYCLES #1 & #2

( $V_{CC} = 5.0V \pm 10\%$ )<sup>b</sup>

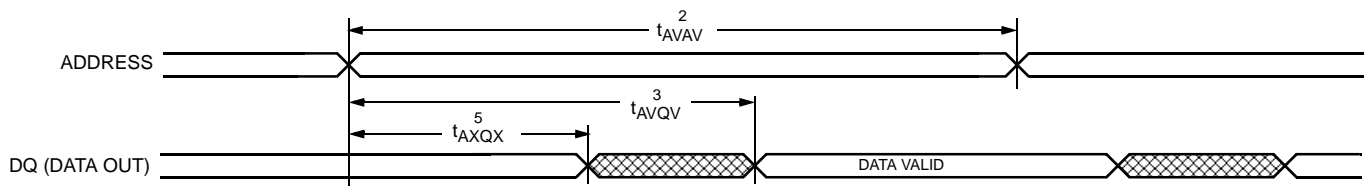
NO.	SYMBOLS		PARAMETER	STK16C68-20		STK16C68-25		STK16C68-35		STK16C68-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{ELQV}$	$t_{ACS}$	Chip Enable Access Time		20		25		35		45	ns
2	$t_{AVAV}^g$	$t_{RC}$	Read Cycle Time	20		25		35		45		ns
3	$t_{AVQV}^h$	$t_{AA}$	Address Access Time		22		25		35		45	ns
4	$t_{GLQV}$	$t_{OE}$	Output Enable to Data Valid		8		10		15		20	ns
5	$t_{AXQX}^h$	$t_{OH}$	Output Hold after Address Change	5		5		5		5		ns
6	$t_{ELQX}$	$t_{LZ}$	Chip Enable to Output Active	5		5		5		5		ns
7	$t_{EHQZ}^i$	$t_{HZ}$	Chip Disable to Output Inactive		7		10		13		15	ns
8	$t_{GLQX}$	$t_{OLZ}$	Output Enable to Output Active	0		0		0		0		ns
9	$t_{GHQZ}^i$	$t_{OHZ}$	Output Disable to Output Inactive		7		10		13		15	ns
10	$t_{ELICCH}^f$	$t_{PA}$	Chip Enable to Power Active	0		0		0		0		ns
11	$t_{EHICCL}^{e, f}$	$t_{PS}$	Chip Disable to Power Standby		25		25		35		45	ns

Note g:  $\bar{W}$  must be high during SRAM READ cycles and low during SRAM WRITE cycles.

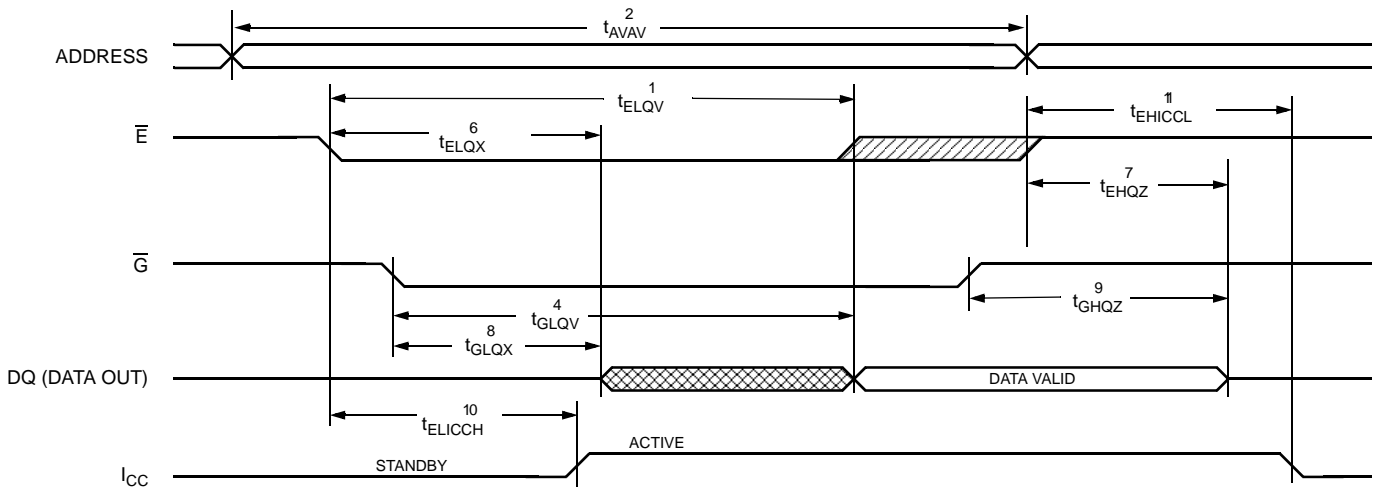
Note h: I/O state assumes  $\bar{E}, \bar{G} \leq V_{IL}$  and  $\bar{W} \geq V_{IH}$ ; device is continuously selected.

Note i: Measured  $\pm 200mV$  from steady state output voltage.

SRAM READ CYCLE #1: Address Controlled<sup>g, h</sup>



SRAM READ CYCLE #2:  $\bar{E}$  Controlled<sup>g</sup>



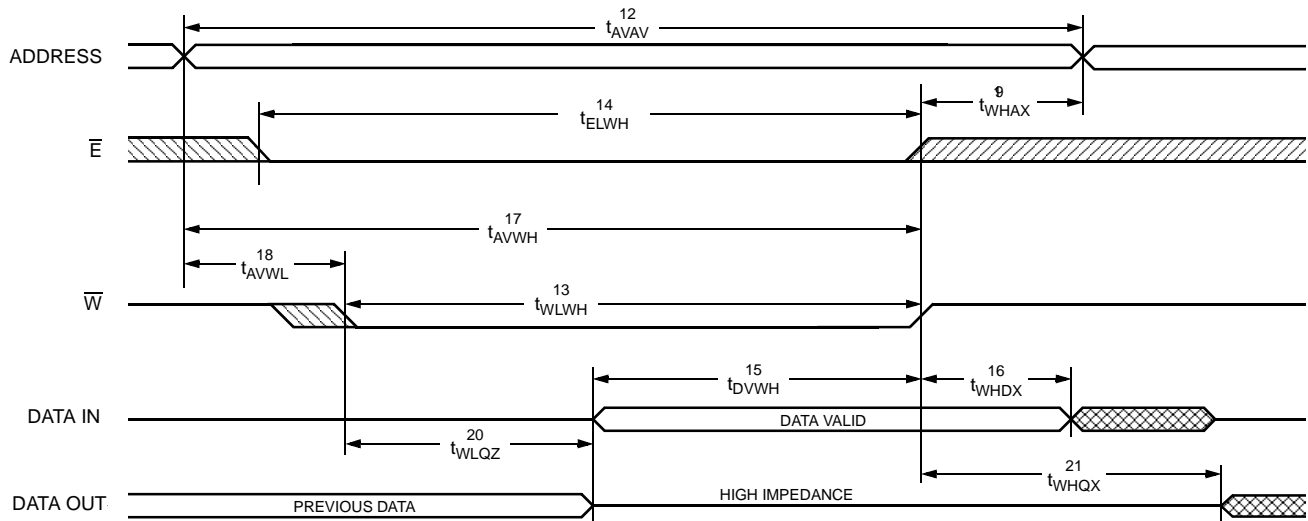
SRAM WRITE CYCLES #1 & #2

( $V_{CC} = 5.0V \pm 10\%$ )<sup>b</sup>

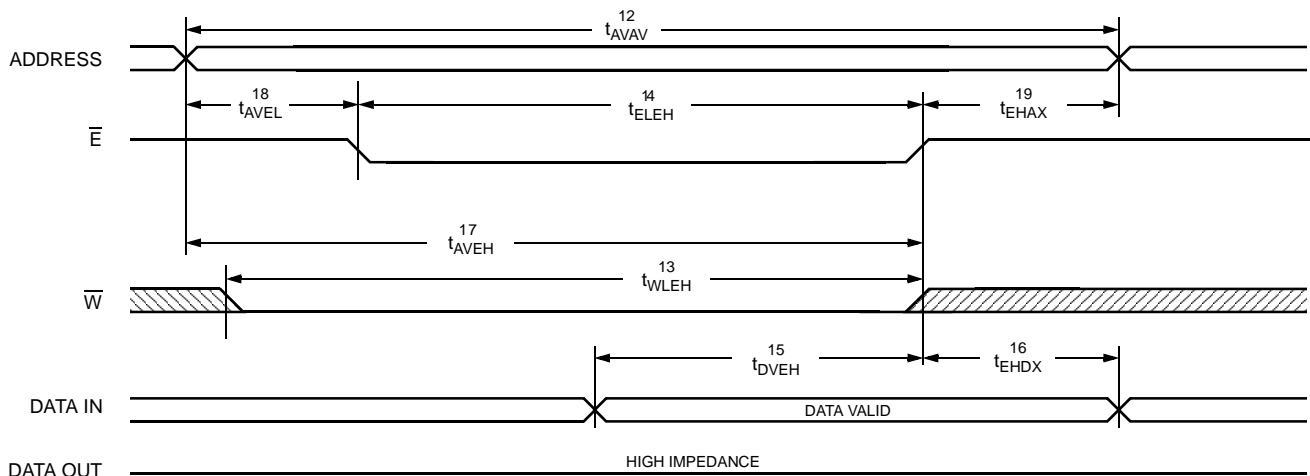
NO.	SYMBOLS			PARAMETER	STK16C68-20		STK16C68-25		STK16C68-35		STK16C68-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
12	$t_{AVAV}$	$t_{AVAV}$	$t_{WC}$	Write Cycle Time	20		25		35		45		ns
13	$t_{WLWH}$	$t_{WLEH}$	$t_{WP}$	Write Pulse Width	15		20		25		30		ns
14	$t_{ELWH}$	$t_{ELEH}$	$t_{CW}$	Chip Enable to End of Write	15		20		25		30		ns
15	$t_{DVWH}$	$t_{DVEH}$	$t_{DW}$	Data Set-up to End of Write	8		10		12		15		ns
16	$t_{WHDX}$	$t_{EHDX}$	$t_{DH}$	Data Hold after End of Write	0		0		0		0		ns
17	$t_{AVWH}$	$t_{AVEH}$	$t_{AW}$	Address Set-up to End of Write	15		20		25		30		ns
18	$t_{AVWL}$	$t_{AVEL}$	$t_{AS}$	Address Set-up to Start of Write	0		0		0		0		ns
19	$t_{WHAX}$	$t_{EHAX}$	$t_{WR}$	Address Hold after End of Write	0		0		0		0		ns
20	$t_{WLQZ}^{i,j}$		$t_{WZ}$	Write Enable to Output Disable		7		10		13		15	ns
21	$t_{WHQX}$		$t_{OW}$	Output Active after End of Write	5		5		5		5		ns

Note j: If  $\bar{W}$  is low when  $\bar{E}$  goes low, the outputs remain in the high-impedance state.  
 Note k:  $\bar{E}$  or  $\bar{W}$  must be  $\geq V_{IH}$  during address transitions.

SRAM WRITE CYCLE #1:  $\bar{W}$  Controlled<sup>k</sup>



SRAM WRITE CYCLE #2:  $\bar{E}$  Controlled<sup>k</sup>



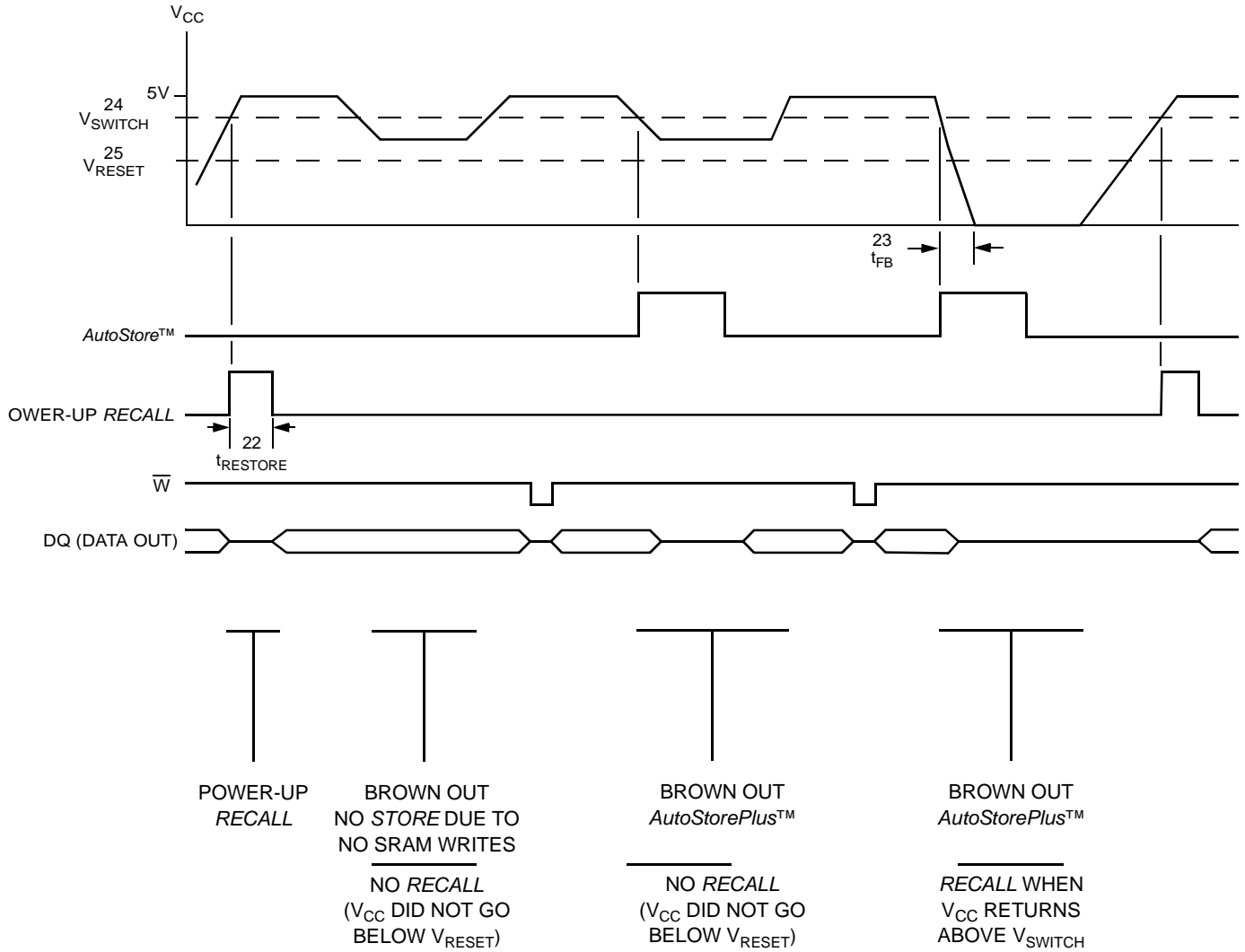
**AutoStorePlus™/POWER-UP RECALL**

( $V_{CC} = 5.0V \pm 10\%$ )<sup>b</sup>

NO.	SYMBOLS	PARAMETER	STK16C68		UNITS	NOTES
	Standard		MIN	MAX		
22	$t_{RESTORE}$	Power-up <i>RECALL</i> Duration		550	$\mu s$	l
23	$t_{FB}$	Maximum $V_{CC}$ Slew Time to Ground		500	ns	f, h
24	$V_{SWITCH}$	Low Voltage Trigger Level	4.0	4.5	V	
25	$V_{RESET}$	Low Voltage Reset Level		3.9	V	f

Note 1:  $t_{RESTORE}$  starts from the time  $V_{CC}$  rises above  $V_{SWITCH}$ .

**AutoStorePlus™/POWER-UP RECALL**



SOFTWARE STORE/RECALL MODE SELECTION

$\bar{E}$	$\bar{W}$	$\bar{G}$	A <sub>12</sub> - A <sub>0</sub> (hex)	MODE	I/O with $\bar{G}$ Low	I/O with $\bar{G}$ High	NOTES
L	H	X	0000 1555 0AAA 1FFF 10F0 0F0F	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile <i>STORE</i>	Output Data Output Data Output Data Output Data Output Data Output High Z	Output High Z Output High Z Output High Z Output High Z Output High Z Output High Z	m
L	H	X	0000 1555 0AAA 1FFF 10F0 0F0E	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile <i>RECALL</i>	Output Data Output Data Output Data Output Data Output Data Output High Z	Output High Z Output High Z Output High Z Output High Z Output High Z Output High Z	m

Note m: The six consecutive addresses must be in the order listed.  $\bar{W}$  must be high during all six consecutive cycles to enable a nonvolatile cycle.

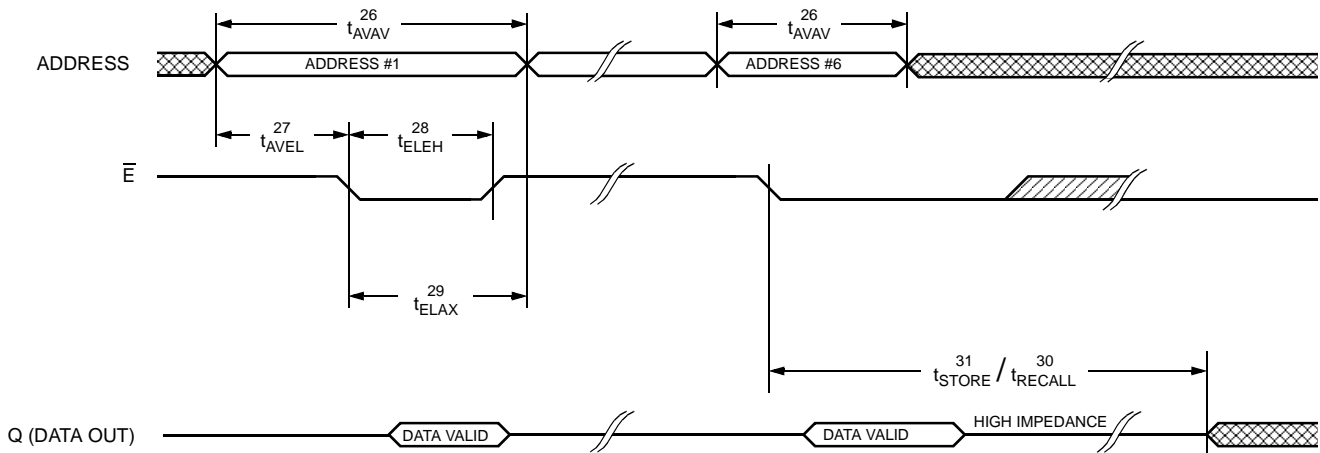
SOFTWARE STORE/RECALL CYCLE<sup>n, o</sup> (V<sub>CC</sub> = 5.0V ± 10%)<sup>b</sup>

NO.	SYMBOLS	PARAMETER	STK16C68-20		STK16C68-25		STK16C68-35		STK16C68-45		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
26	t <sub>AVAV</sub>	STORE/RECALL Initiation Cycle Time	20		25		35		45		ns
27	t <sub>AVEL</sub> <sup>n</sup>	Address Set-up Time	0		0		0		0		ns
28	t <sub>ELEH</sub> <sup>n</sup>	Clock Pulse Width	15		20		25		30		ns
29	t <sub>ELAX</sub> <sup>h, n</sup>	Address Hold Time	15		20		20		20		ns
30	t <sub>RECALL</sub>	RECALL Cycle Duration		20		20		20		20	μs
31	t <sub>STORE</sub>	STORE Cycle Duration		10		10		10		10	ms

Note n: The software sequence is clocked with  $\bar{E}$  controlled READs.

Note o: The six consecutive addresses must be in the order listed in the Software STORE/RECALL Mode Selection Table: (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a STORE cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a RECALL cycle.  $\bar{W}$  must be high during all six consecutive cycles.

SOFTWARE STORE/RECALL CYCLE:  $\bar{E}$  Controlled<sup>o</sup>



## DEVICE OPERATION

The *AutoStorePlus*<sup>™</sup> STK16C68 is a fast 8K x 8 SRAM that does not lose its data on power-down. The data is preserved in integral *QuantumTrap*<sup>™</sup> EEPROM while power is unavailable. The nonvolatility of the STK16C68 does not require any system intervention or support: *AutoStorePlus*<sup>™</sup> on power-down and automatic RECALL on power-up guarantee data integrity without the use of batteries.

### NOISE CONSIDERATIONS

Note that the STK16C68 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1 $\mu$ F connected between  $V_{CC}$  and  $V_{SS}$ , using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

### SRAM READ

The STK16C68 performs a READ cycle whenever  $\overline{E}$  and  $\overline{G}$  are low and  $\overline{W}$  is high. The address specified on pins  $A_{0-12}$  determines which of the 8,192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of  $t_{AVQV}$  (READ cycle #1). If the READ is initiated by  $\overline{E}$  or  $\overline{G}$ , the outputs will be valid at  $t_{ELQV}$  or at  $t_{GLQV}$ , whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the  $t_{AVQV}$  access time without the need for transitions on any control input pins, and will remain valid until another address change or until  $\overline{E}$  or  $\overline{G}$  is brought high or  $\overline{W}$  is brought low.

### SRAM WRITE

A WRITE cycle is performed whenever  $\overline{E}$  and  $\overline{W}$  are low. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either  $\overline{E}$  or  $\overline{W}$  goes high at the end of the cycle. The data on the common I/O pins  $DQ_{0-7}$  will be written into the memory if it is valid  $t_{DVWH}$  before the end of a  $\overline{W}$  controlled WRITE or  $t_{DVEH}$  before the end of an  $\overline{E}$  controlled WRITE.

It is recommended that  $\overline{G}$  be kept high during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If  $\overline{G}$  is left low, internal circuitry will turn off the output buffers  $t_{WLQZ}$  after  $\overline{W}$  goes low.

### *AutoStorePlus*<sup>™</sup> OPERATION

The STK16C68's automatic STORE on power-down is completely transparent to the system. The *AutoStore*<sup>™</sup> initiation takes less than 500ns when power is lost ( $V_{CC} < V_{SWITCH}$ ) at which point the part depends only on its internal capacitor for STORE completion. This safe transfer of data from SRAM to EEPROM takes place regardless of power supply slew rate.

In order to prevent unneeded STORE operations, the automatic STORE will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software-initiated STORE cycles are performed regardless of whether or not a WRITE operation has taken place.

### POWER-UP RECALL

During power up, or after any low-power condition ( $V_{CC} < V_{RESET}$ ), an internal RECALL request will be latched. When  $V_{CC}$  once again exceeds the sense voltage of  $V_{SWITCH}$ , a RECALL cycle will automatically be initiated and will take  $t_{RESTORE}$  to complete.

If the STK16C68 is in a WRITE state at the end of power-up RECALL, the SRAM data will be corrupted. To help avoid this situation, a 10k $\Omega$  resistor should be connected either between  $\overline{W}$  and system  $V_{CC}$  or between  $\overline{E}$  and system  $V_{CC}$ .

### SOFTWARE NONVOLATILE STORE

The STK16C68 software STORE cycle is initiated by executing sequential READ cycles from six specific address locations. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence or the sequence will be aborted and no STORE or RECALL will take place.

To initiate the software STORE cycle, the following READ sequence must be performed:

1. Read address 0000 (hex) Valid READ
2. Read address 1555 (hex) Valid READ
3. Read address 0AAA (hex) Valid READ
4. Read address 1FFF (hex) Valid READ
5. Read address 10F0 (hex) Valid READ
6. Read address 0F0F (hex) Initiate STORE cycle

The software sequence must be clocked with  $\bar{E}$  controlled READs.

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that  $\bar{G}$  be low for the sequence to be valid. After the  $t_{STORE}$  cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

**SOFTWARE NONVOLATILE RECALL**

A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of READ operations must be performed:

1. Read address 0000 (hex) Valid READ
2. Read address 1555 (hex) Valid READ
3. Read address 0AAA (hex) Valid READ
4. Read address 1FFF (hex) Valid READ
5. Read address 10F0 (hex) Valid READ
6. Read address 0F0E (hex) Initiate RECALL cycle

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared, and second, the nonvola-

tile information is transferred into the SRAM cells. After the  $t_{RECALL}$  cycle time the SRAM will once again be ready for READ and WRITE operations. The RECALL operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

**HARDWARE PROTECT**

The STK16C68 offers hardware protection against inadvertent STORE operation and SRAM WRITES during low-voltage conditions. When  $V_{CC} < V_{SWITCH}$ , software STORE operations and SRAM WRITES are inhibited.

**LOW AVERAGE ACTIVE POWER**

The STK16C68 draws significantly less current when it is cycled at times longer than 50ns. Figure 2 shows the relationship between  $I_{CC}$  and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range,  $V_{CC} = 5.5V$ , 100% duty cycle on chip enable). Figure 3 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK16C68 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READs to WRITES; 5) the operating temperature; 6) the  $V_{CC}$  level; and 7) I/O loading.

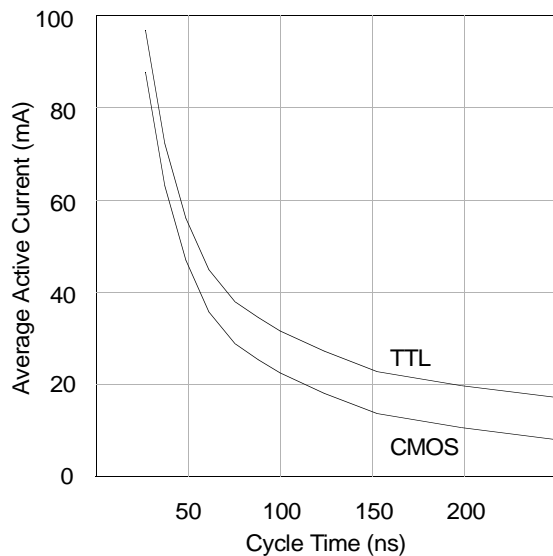


Figure 2:  $I_{CC}$  (max) Reads

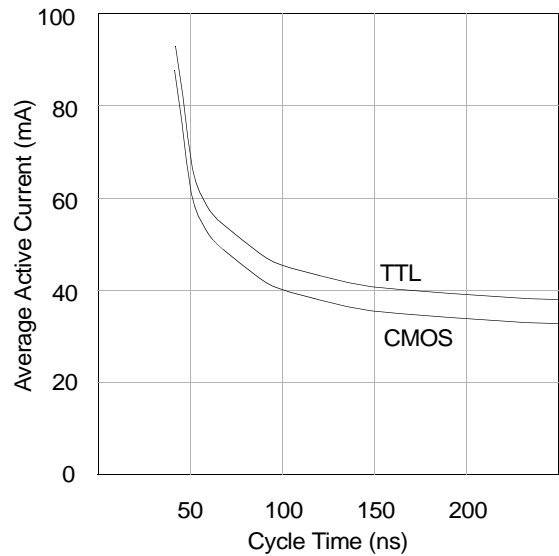
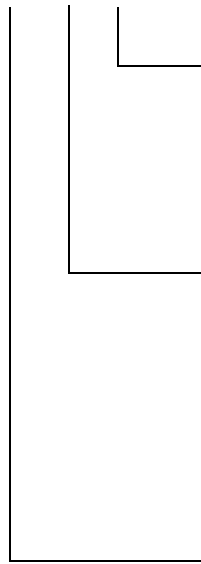


Figure 3:  $I_{CC}$  (max) Writes



ORDERING INFORMATION

STK16C68 - W 25 I



Temperature Range

Blank = Commercial (0 to 70°C)

I = Industrial (-40 to 85°C)

Access Time

20 = 20ns (Commercial only)

25 = 25ns

35 = 35ns

45 = 45ns

Package

W = Plastic 28-pin 600 mil DIP

S = Plastic 28-pin 350 mil SOIC \*(call factory for availability of this package)