Ordering number:ENN*5024

Thick Film Hybrid IC

# STK311-050

## RDS/RBDS Demodulator with Synchronization and Error Correction

**Preliminary**

## Overview

The STK311-050 is an RDS/RBDS demodulator hybrid IC for the Radio Data System (RDS) and the Radio Broadcast Data System (RBDS), or multiplexed FM broadcasting of various kinds of data, specified by the European Broadcasting Union (EBU) and US National Radio System Committee (NRSC), respectively. It demodulates the multiplexed data modulating signal to recover the RDS/RBDS signal and performs synchronization, error detection and error correction, Further, low-profile packaging is realized using Sanyo's insulated metal substrate technology (IMST) for the base, SC system and photoresist technologies and folded board construction.

## Applications

- Car stereos
- Home stereos

## Features

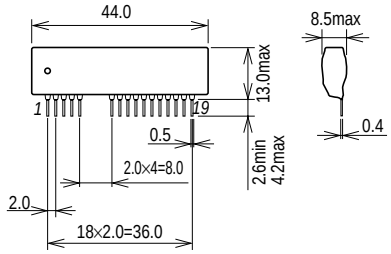
- 57kHz BPF built-in for adjustment-free operation
- 4MHz ceramic oscillator element built-in
- Few external components required for a complete RDS/RBDS data demodulation system
- ARI-SK/DK decoder built-in

## Package Dimensions

unit:mm

4132A

[STK311-050]




SANYO : SIP19C3

## Specifications

### Maximum Ratings at Ta = 25˚C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{CC}$ max | | 6.3 | V |
| Operating temperature | Topr | | –30 to +85 | ˚C |
| Storage temperature | Tstg | | –40 to +100 | ˚C |

### Recommended Operating Voltages at Ta = 25˚C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | 5 | V |
| Operating supply voltage range | $V_{CCOP}$ | | 4.7 to 5.5 | V |

## Operating Characteristics at Ta = 25˚C, $V_{CC}$=5V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Quiescent current | $I_{CCO}$ | | | 26 | 38 | mA |
| Band-pass filter gain | $VG_{BPF}$ | f=57kHz | 9 | 12.5 | 17 | dB |
| Band-pass filter selectivity | | f=60kHz (57kHz=0dB) | –6 | –2.5 | 0 | dB |
| | | f=54kHz (57kHz=0dB) | –6 | –3.5 | 0 | dB |
| | | f=38kHz (57kHz=0dB) | | –39 | –33 | dB |
| PLL capture range | CR | 5mVrms, CW input | | –0.5 +1.1 | | % |
| RDS/RBDS detector sensitivity | | Pin 12 low, input on pin 4 | | 0.4 | 1.0 | mVrms |
| SK detector sensitivity | | Pin 11 low, input on pin 4 | | 1.0 | 2.0 | mVrms |
| DK detector sensitivity | | Pin 10 low, input on pin 4 | | 1.9 | 2.9 | mVrms |
| RDS/RBDS input dynamic range | | Pin 12 low, (ARI+RDS/RBDS) signal maximum input on pin 4 | 30 | 50 | | mVrms |
| | | RDS/RBDS data demodulated correctly, RDS/RBDS signal maximum input on pin 4 | 250 | | | mVrms |
| DK input dynamic range | | Pin 10 low, ARI signal maximum input on pin 4 | 75 | 100 | | mVrms |
| VCO free-running frequency | $f_{OSC}$ | | 453 | 456 | 459 | kHz |
| High level ouput voltage | $V_{OH}$ | $I_{OH}$=–50μA*1 | $V_{CC}$–1.2 | | | V |
| | | $I_{OH}$=–10μA*1 | $V_{CC}$–0.5 | | | V |
| Low level output voltage | $V_{OL}$ | $I_{OL}$=10mA*2 | | | 1.5 | V |
| | | $I_{OL}$=1.8mA*2 | | | 0.4 | V |
| Ceramic oscillator stabilization time | $t_{CFS}$ | See Figure 1. | | | 10 | ms |
| Reset time | $t_{RST}$ | | See Figure 2. | | | |

*1. DATA START, DATA OUT, CLOCK OUT
*2. RECEIVE, CORRECTION, ERROR, DATA START, DATA OUT, CLOCK OUT

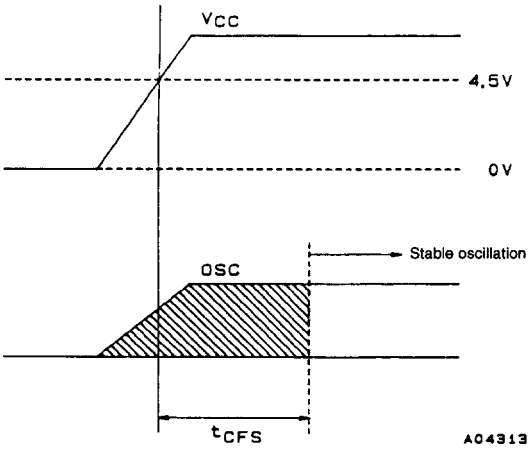



**Figure 1. Oscillator stabilization time**

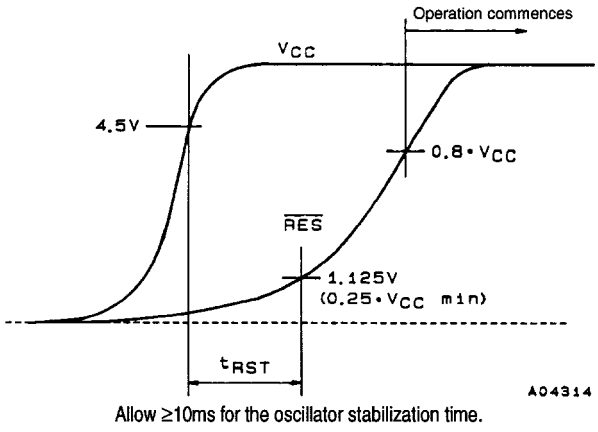



**Figure 2. Reset time**

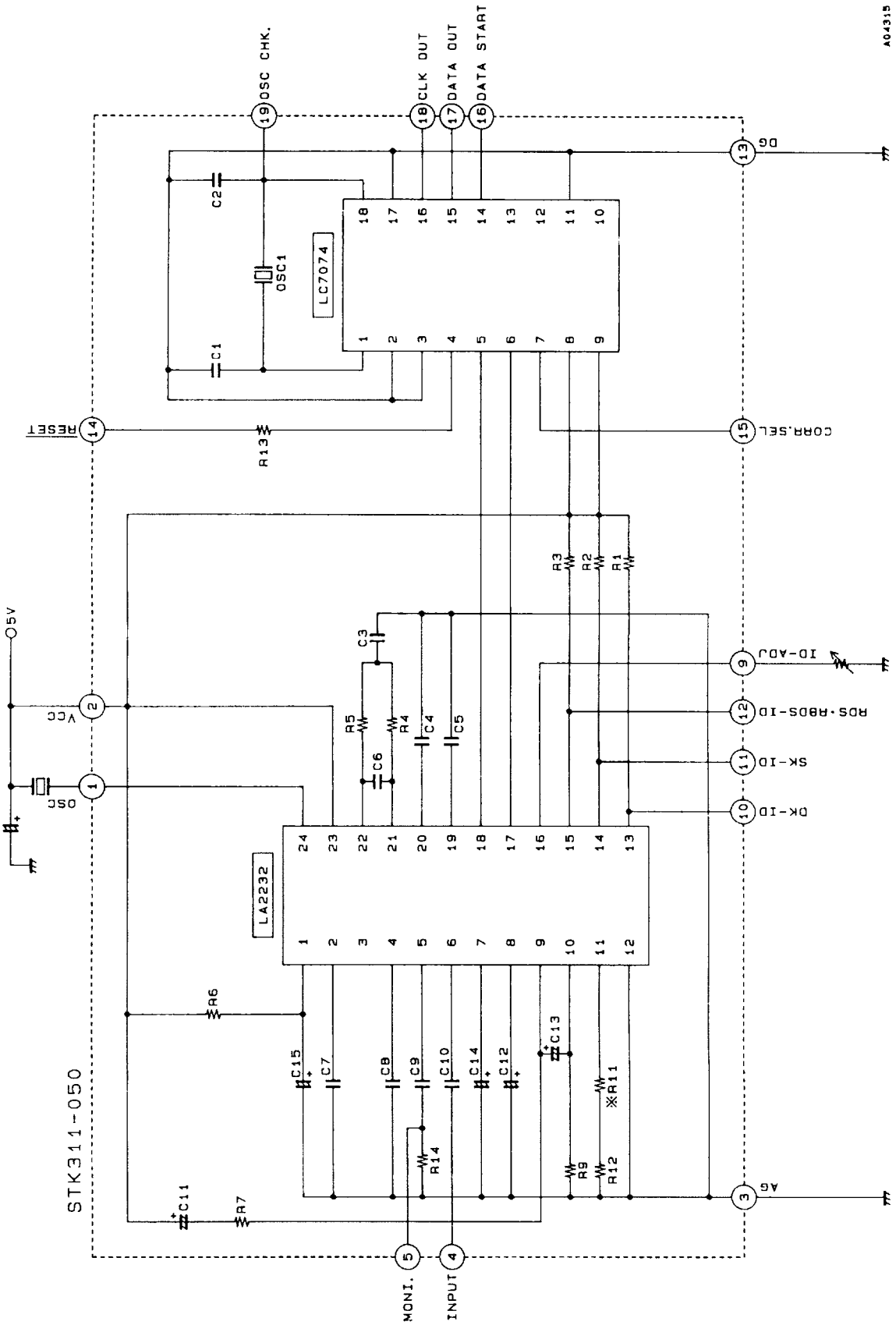
## Output Signal Settings

CLK OUT and DATA START output signals can be set as shown in the following table.

| Setting*1 | CLK OUT polarity | DATA START output |
|---|---|---|
| 1 | Falling edge | Each block |
| 2 | Falling edge | Second block only |
| 3 | Rising edge | Each block |
| 4 | Rising edge | Second block only |

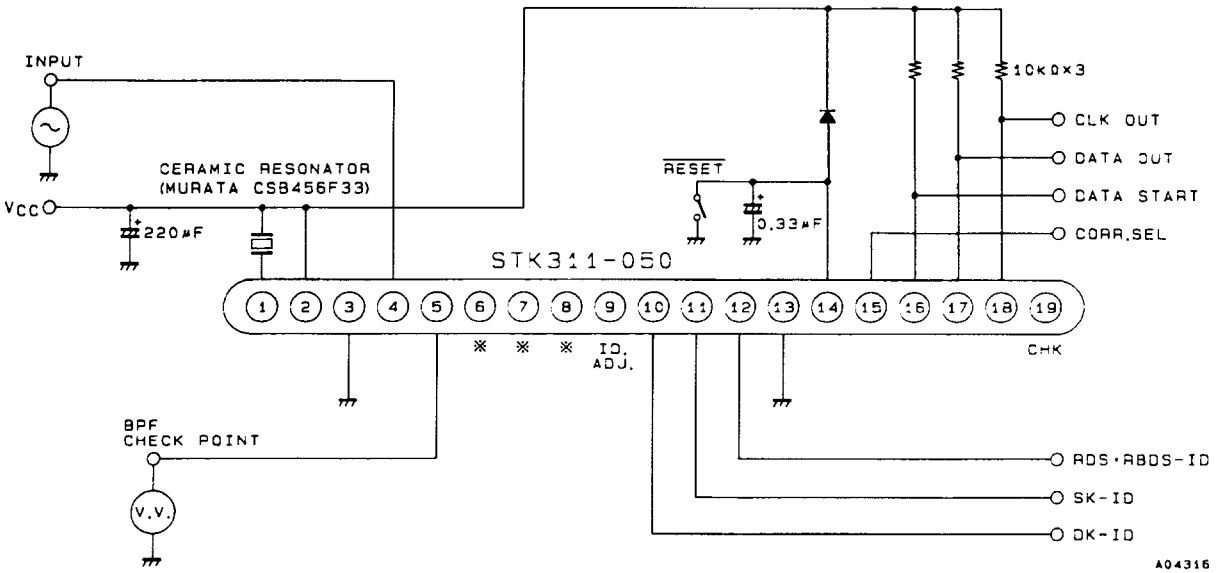
*1. Setting 1 is the default setting.

## Equivalent Circuit



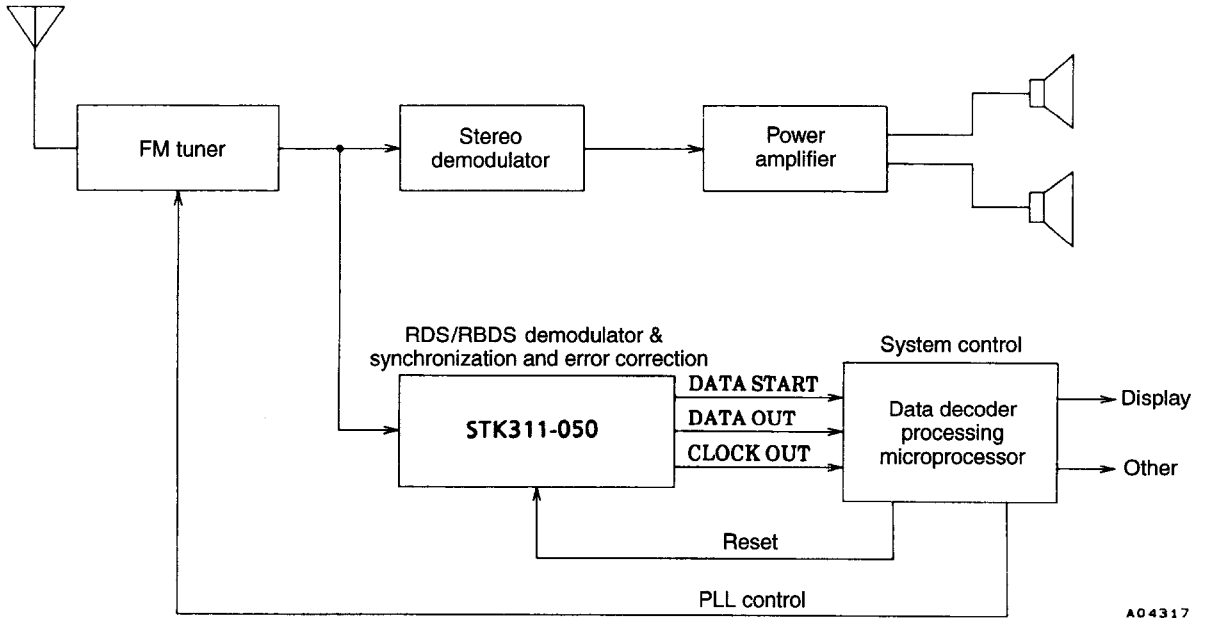

※ R11 is a function trimming resistor.
Pins 6, 7 and 8 are not used.

## Sample Application Circuit

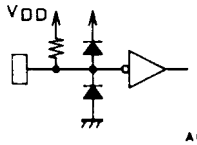
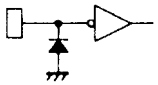
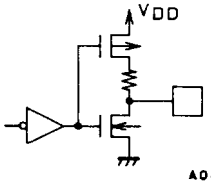
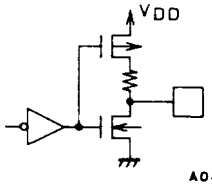
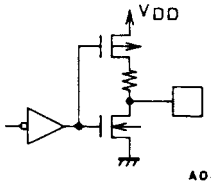



※ Pins 6, 7 and 8 are not used.

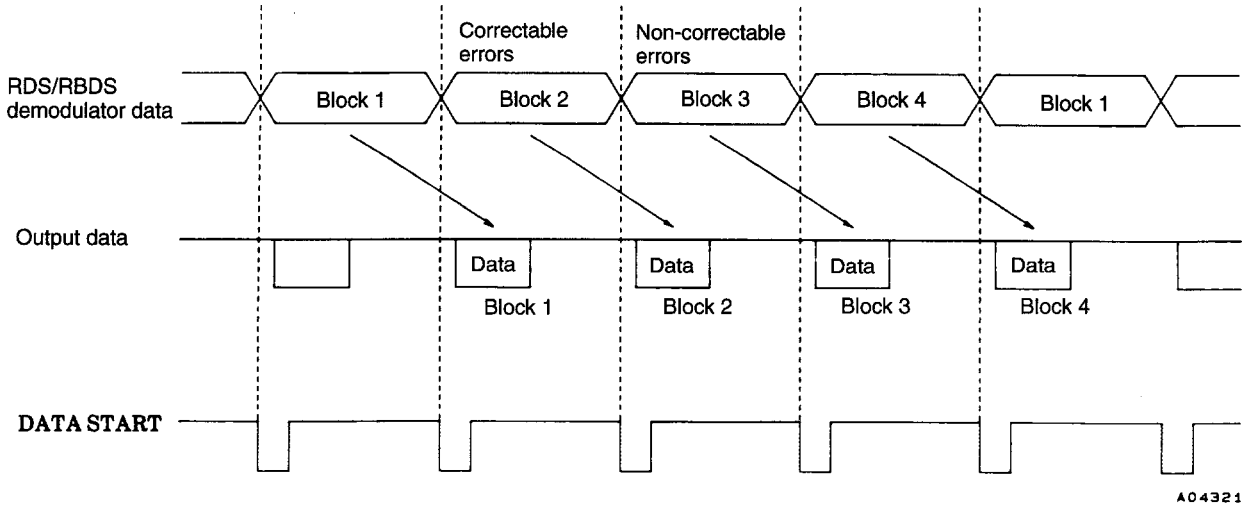
## Sample System Configuration



## Pin Functions

| Pin No. | Pin name | Function | |
|---|---|---|---|
| 1 | OSC | VCO ceramic oscillator pin (456kHz) | |
| 2 | $V_{CC}$ | Supply pin : LA2232 and LC7074 positive supply | |
| 3 | AG | Ground pin : LA2232 analog ground | |
| 4 | INPUT | Input pin | |
| 5 | MONI | BPF (for adjustment) monitor output | |
| 9 | ID-ADJ | SK detector sensitivity adjustment pin | |
| 10 | DK-ID | DK signal detector indicator output.<br>Low-level output when an DK signal is detected, and high-level when not detected. | |
| 11 | SK-ID | SK signal detector indicator output.<br>Low-level output when an SK signal is detected, and high-level when not detected. | |
| 12 | RDS/RBDS-ID | RDS/RBDS signal detector indicator output.<br>Low-level output when an RDS/RBDS signal is detected, and high-level when not detected. | |
| 13 | DG | Ground pin : LC7074 digital ground | |
| 14 | RESET |  | Reset input.<br>Reset restart occurs when held low for 4 cycles.<br>Schmitt-trigger input.<br>Pull-up resistor built-in. |
| 15 | CORR. SEL |  | Error correction selection input.<br>This pin selects whether the IC corrects errors in the RDS demodulated data.<br>Input = 0 : No correction performed.<br>Input = 1 : Error correction performed.<br>In modes where error correction is enabled, up to five error bits are corrected for distances of 5 bits or less. |
| 16 | DATA START |  | Serial data output block data start signal (D.S. CONTROL) input to control the output waveform.<br>Pull-up MOS transistor (CMOS) output. |
| 17 | DATA OUT |  | Serial data output.<br>Pull-up MOS transistor (CMOS) output. |
| 18 | CLK OUT |  | Clock output.<br>Pull-up MOS transistor (CMOS) output. |
| 19 | OSC CHK | OSC1 oscillation frequency check pin | |

## RDS/RBDS Demodulator Data (LA2232 Output) and LC7074 Output Data Relationship




The LC7074 serial data output is delayed by 1 block from the data received from the LA2232.

**Figure 3. Demodulator data and output data relationship**

## Serial Data Output Format and Timing

| Bit | Function | |
|---|---|---|
| S | Start bit (normally "0") | |
| E | Error flag | Parameter / E / F<br>No errors / 0 / 0<br>Errors corrected / 0 / 1<br>Non-correctable errors / 1 / 1<br>Note : When CORR. SEL is high. |
| F | Correction flag | |
| OE | Offset E | |
| OF | Offset F (normally "0", for future expansion) | |
| A/B | Group type version | 0 : Version A<br>1 : Version B |
| B1, B0 | Block number | 00 : Block 1<br>01 : Block 2<br>10 : Block 3<br>11 : Block 4 |
| D15 to D0 | RDS/RBDS data | |

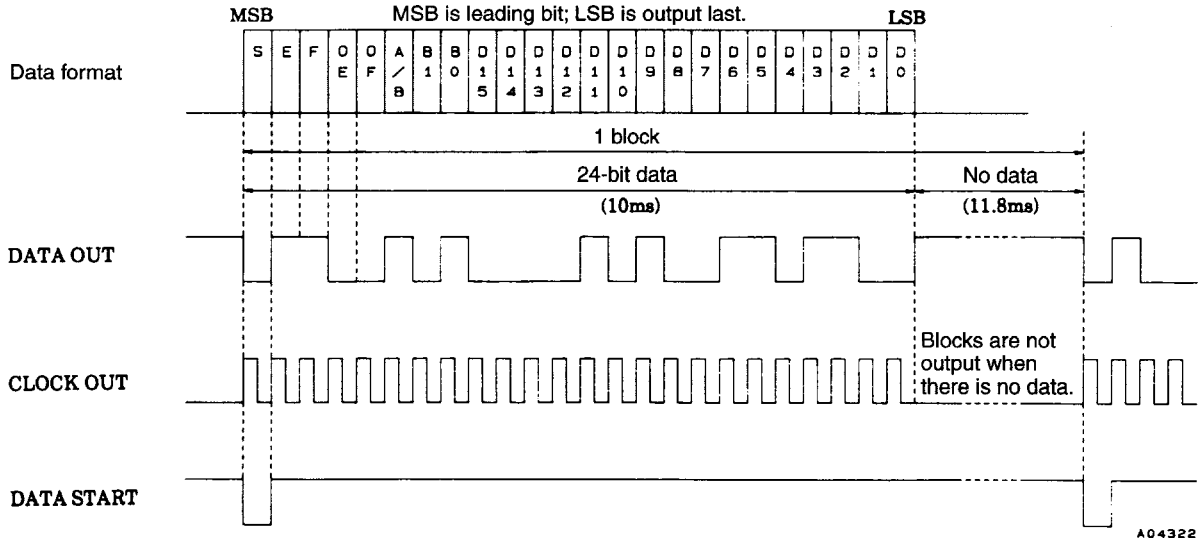



**Figure 4. Serial data output format and timing**

## Control Input CORR. SEL Read Timing

Normally, this pin is checked for its state. However, error correction can be enabled/disabled at any time.

### During Sync Detection

CORR. SEL is read for every bit of demodulator data from the RDS/RBDS demodulator IC (indiated by ↓), and is read into the LSI when 4 consecutive, matching states occur.

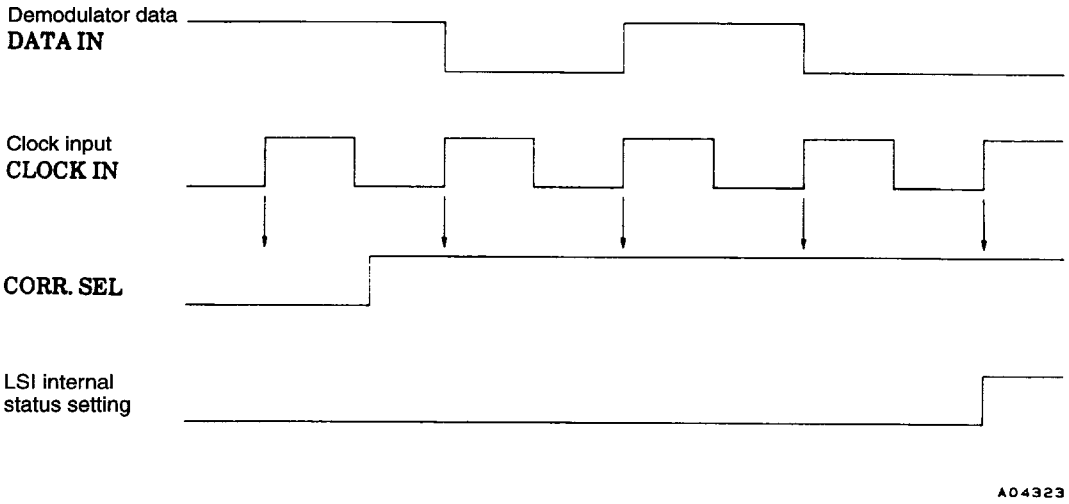



**Figure 5. CORR. SEL read timing during sync detection**

### After Sync Detection

CORR. SEL is read for the head of each block of demodulator data from the RDS/RDBS demodulator IC (indiated by ↓), and is read into the LSI when 4 consecutive, matching states occur.

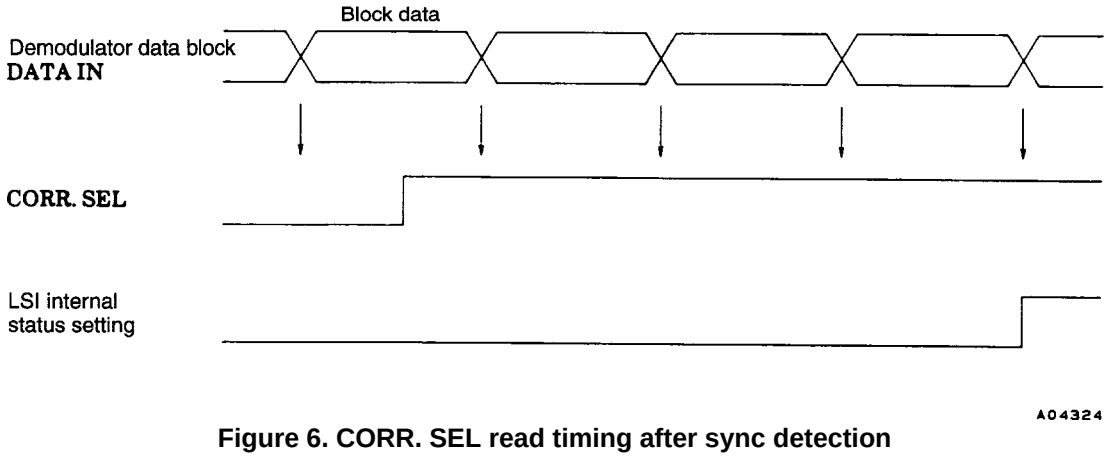



**Figure 6. CORR. SEL read timing after sync detection**

## Characteristics Data