

STK4044XI

AF Power Amplifier (Split Power Supply) (100 W min, THD = 0.008 %)

Features

- Compact packaging supports slimmer set designs
- Series designed from 50 up to 150 W and pincompatibility
- Simpler heat sink design facilitates thermal design of slim stereo sets
- Current mirror circuit, cascade circuit and purecomplimentary circuit application reduce distortion to 0.008 %
- Supports addition of electronic circuits for thermal shutdown and load-short protection circuit as well as pop noise muting which occurs when the power supply switch is turned on and off.

Specifications

Maximum Ratings at $Ta = 25^{\circ}C$

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Parameter	Symbol	Conditions /	Ratings	Unit
Maximum supply voltage	V _{CC} max		± 74	V
Thermal resistance	θј-с		1.2	°C/W
Junction temperature	Tj		150	°C
Operating substrate temperature	Tc		125	°C
Storage temperature	Tstg		−30 to +125	°C
Permissible load short time	t _s *1	$V_{CC} = \pm 51 \text{ V}, R_{L} = 8 \text{ G} = 50 \text{ Hz}, P_{O} = 100 \text{ W}$	1	s

Recommended Operating Conditions at Ta = 25 C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	Vcc		± 51	V
Load resistance	₹ ₹ R _L		8	Ω

Operating Characteristics

at Ta = 25°C, V_{CC} = ± 51 V, $R_f \neq 8 \Omega$, VG = 40 dB, $Rg \neq 600 \Omega$, 100 kHz LPF ON, R_L (noninductive)

Description of the state of the	4		Ratings			1.1
Parameter		Symbol		typ	max	Unit
Quiescent current	loco.	V _{CQ} = ≠ 61.5 V	15		120	mA
Output power	P _O	THD = 0.008 %, f = 20 Hz to 20 kHz	100			W
Total harmonic distortion	THD	Po = 1.0 W, f = 1 kHz			0.008	%
Frequency response	f∟, f _H ∕	$P_{O} = 1.0 \text{ W}, \frac{+0}{-3} \text{ dB}$		20 to 50k		Hz
Input resistance	1/	P _O = 1.0 W, f = 1 kHz		55		kΩ
Output noise voltage	¥ No *2	$V_{CC} = \pm 61.5 \text{ V}, \text{ Rg} = 10 \text{ k}\Omega$			1.2	mVrms
Neutral voltage	$I = V_N$	V _{CC} = ± 61.5 V	-70	0	+ 70	mV

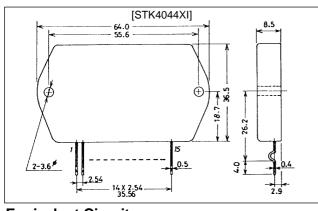
Note: Use rated power supply for test unless otherwise specified.

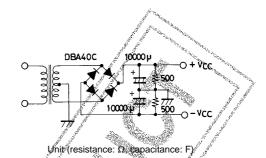
- *1. When measuring permissible load short time and output noise voltage use transformer power supply indicated next page.
- 2 Output noise voltage represents the peak value on the rms scale (VTVM). The noise voltage waveform does not include the pulse noise.
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Package Dimensions

unit: mm

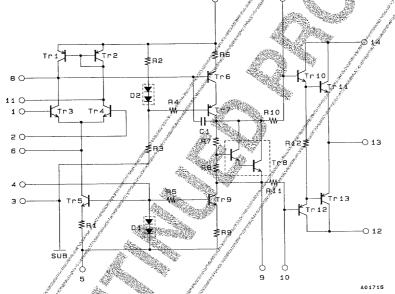
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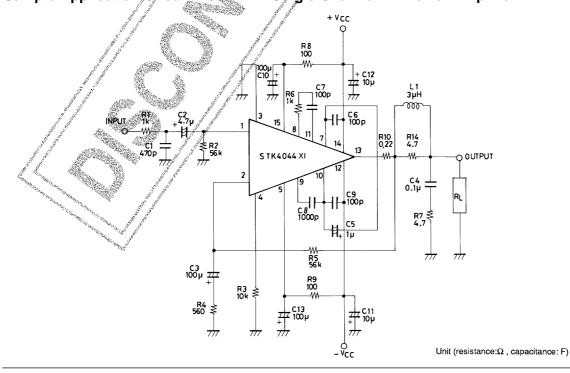


Specified Transformer Power Supply (MG-200 Equivalent)

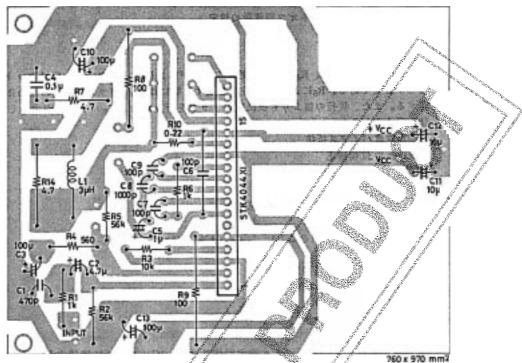




Sample Application Circuit: 100W min Single Channel AF Power Amplifier



Sample Printed Circuit Pattern for Application Circuit (Copper-foiled side)



Description of External Parts

Unit (resistance: Ω , capacitance: F)

 R_1, C_1 : Input filter circuit

• Reduces high-frequency noise.

C₂ : Input coupling capacitor

• DC current suppression. A reduction in reactance is effective because of increases in capacitor reactance at low frequencies and 1/f noise dependence on signal source resistance which result in output noise worsening.

R₂ : Input bias resistor

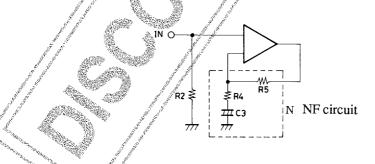
• Biases the input pin to zero.

ullet Effects V_N stability (refer to NF circuit).

• Due to differential input input resistance is more or less determined by this resistance value.

R₄, R₅ : NFB circuit (AC NF encurt). Use of resistor with 1% error is suggested.

 $C_3(R_2)$



 $\begin{array}{ll} C_3 & : \ AC \ NF \ capacitor \\ R_4, R_5 & : \ Used \ for \ VG \ setting. \end{array}$

• VG settings are obtained using R₄ and R₅ according to the following equation:

$$log 20 \cdot \frac{R_5}{R_4} \qquad \quad 40 \ dB \ is \ recommended.$$

• Low-frequency cutoff frequency settings are obtained using R4 and C3 according to the following

$$f_{L} = \frac{1}{2\pi \cdot R_4 \cdot C_3} \quad [Hz]$$

When changing the VG setting, you should change R4 which requires a recheck of the low cutoff frequency setting. When the VG setting is changed using R₅, the setting should ensure R₂ equals R₅ so that N_N balance stability is maintained. If the resistor value is increased more than the existing value, V_N balance may be disturbed and result in deterioration of V_N temperature characteristics

 R_3 : Differential constant-current bias resistor

 R_6, R_7 : For oscillation suppression and phase compensation applications

(For use with differential stage applications)

 R_7, C_4 : For oscillation suppression and phase compensation applications

(A Mylar capacitor is recommended for C₄ for use with output stage applications)

: For oscillation suppression and phase compensation applications

 C_6 : Positive (+) power Power stage (Must be connected near the pin) Negative (–) power

 C_8 : For oscillation suppression and phase compensation applications

(Oscillation suppression before power step clip)

 C_5 : For oscillation suppression and distortion improvement applications

 R_8, C_{10} : Ripple filter circuit on positive (+) side. : Ripple filter circuit on negative (-) side: R_9, C_{13}

 C_{11}, C_{12} : For oscillation suppression applications

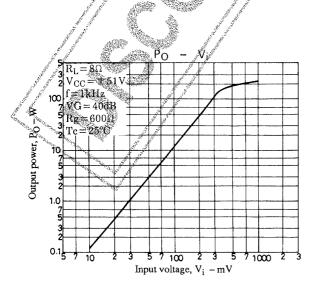
• Used for reducing power supply impedance to stable IC operation and should be connected near the IC pin. We recommend that you use an electrolytic capacitor.

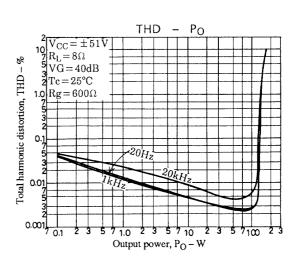
 R_{10} : Output resistor

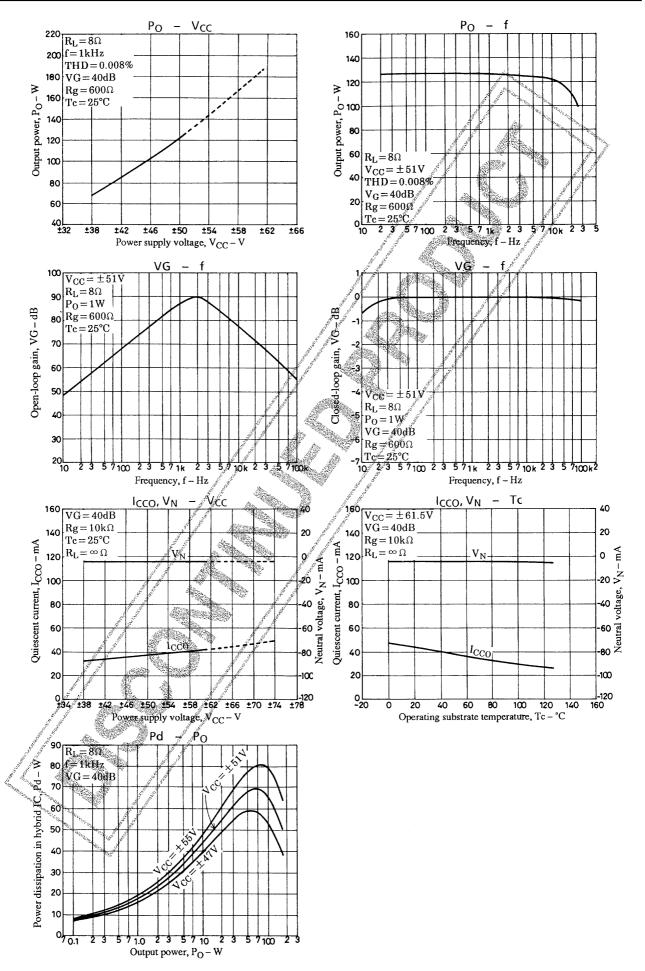
Increases load shorting endurance capacity during times of high output.

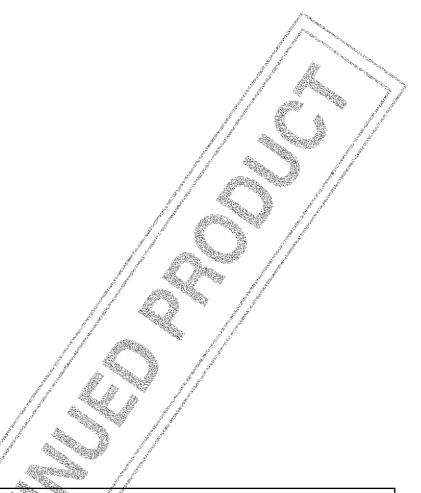
: For oscillation suppression applications R_{14}, L_1

Increases oscillation stability against capacitance loads.









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