Ordering number : ENA0754A

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

STK672-540 — Thick-Film Hybrid IC 2-phase Stepping Motor Driver

Overview

The STK672-540 is a hybrid IC for use as a unipolar, 2-phase stepping motor driver with PWM current control.

Applications

- Office photocopiers, printers, etc.

Features

- The motor speed can be controlled by the frequency of an external clock signal.
- 2-phase excitation or 1-2 phase excitation is selected according to switching the state of the MODE pin (low or high).
- The phase is maintained even if the excitation mode is switched in the middle of operation.
- The direction of rotation can be changed by applying a high or low signal to the CWB pin used to select the direction of rotation.
- Supports schmitt input for 2.5V high level input.
- Incorporating a current detection resistor (0.11Ω: resistor tolerance ±2%), motor current can be set using two external resistors.
- Equipped with an ENABLE pin that, during clock input, allows motor output to be cut-off and resumed later while maintaining the same excitation timing.

Specifications

Absolute Maximum Ratings at Tc = 25°C

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage 1	V_{CC} max	No signal	52	V
Maximum supply voltage 2	V_{DD} max	No signal	-0.3 to +7.0	V
Input voltage	V_{IN} max	Logic input pins	-0.3 to +7.0	V
Output current 1	I_{OP} max	10μA 1 pulse (resistance load)	10	A
Output current 2	I_{OH} max	V_{DD}=5V, CLOCK≥200Hz	4	A
Allowable power dissipation	Pd max	With an arbitrarily large heat sink. Per MOSFET	13.3	W
Operating substrate temperature	Tc max		105	°C
Junction temperature	Tj max		150	°C
Storage temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at Ta=25°C

Parameter	Symbol	Conditions	Ratings	unit
Operating supply voltage 1	V_{CC}	With signals applied	10 to 42	V
Operating supply voltage 2	V_{DD}	With signals applied	5±5%	V
Input high voltage	V_{IH}	Pins 8, 9, 10, 11, 12	2.5 to V_{DD}	V
Input low voltage	V_{IL}	Pins 8, 9, 10, 11, 12	0 to 0.6	V
Output current 1	$I_{OH}1$	Tc=105°C, CLOCK≥200Hz, Continuous operation, duty=100%	3.0	A
Output current 2	$I_{OH}2$	Tc=80°C, CLOCK≥200Hz, Continuous operation, duty=100%, See the motor current (I_{OH}) derating curve	3.3	A
CLOCK frequency	f_{CL}	Minimum pulse width: at least 10μs	0 to 50	kHz
Phase driver withstand voltage	V_{DSS}	I_D=1mA (Tc=25°C)	100min	V
Recommended operating substrate temperature	Tc	No condensation	0 to 105	°C
Recommended Vref range	Vref	Tc=105°C	0.14 to 1.62	V

Refer to the graph for each conduction-period tolerance range for the output current and brake current.

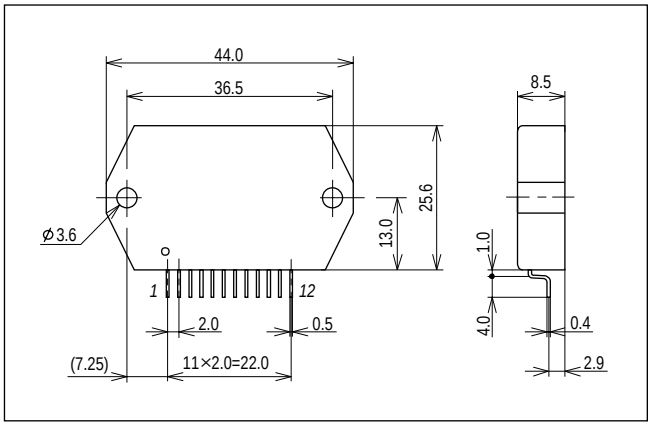
Electrical Characteristics at Tc=25°C, V_{CC}=24V, V_{DD}=5.0V

Parameter	Symbol	Conditions	min	typ	max	unit
V_{DD} supply current	I_{CCO}	Pin 6 current CLOCK=GND		3.1	7	mA
Output average current	Ioave	R/L=3Ω/3.8mH in each phase	0.52	0.58	0.64	A
FET diode forward voltage	Vdf	If=1A (R_L=23Ω)		1.0	1.6	V
Output saturation voltage	Vsat	R_L=23Ω		0.28	0.40	V
Input high voltage	V_{IH}	Pins 8, 9, 10, 11, 12	2.5			V
Input low voltage	V_{IL}	Pins 8, 9, 10, 11, 12			0.6	V
Input leak current	I_{IL}	Pins 8, 9, 10, 11, 12=GND and 5V			±10	μA
Vref input bias current	I_{IB}	Pin 7 =1.0V		204	216	μA
PWM frequency	fc		35	45	55	kHz

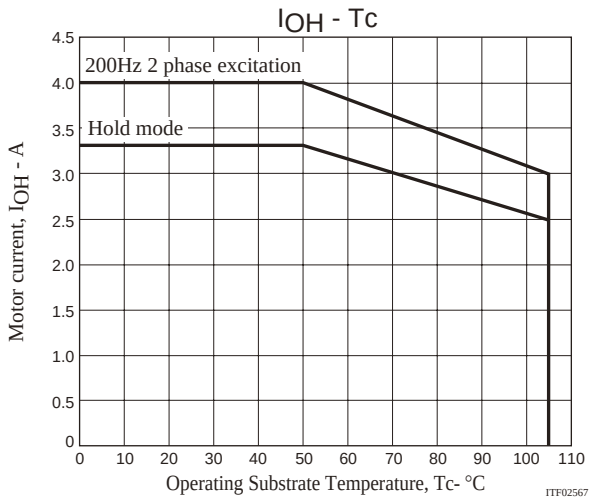
Notes: A fixed-voltage power supply must be used.

Package Dimensions

unit:mm (typ)



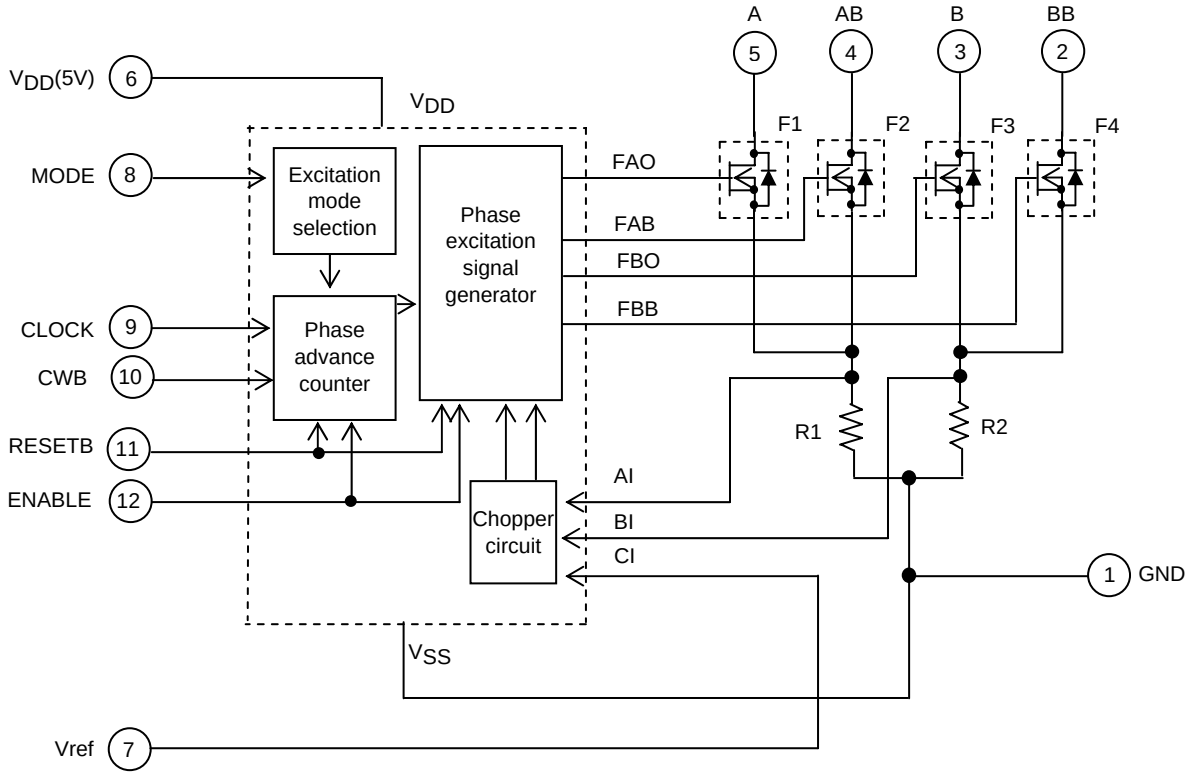
Derating Curve of Motor Current, I_{OH}, vs. STK672-540 Operating Substrate Temperature, Tc



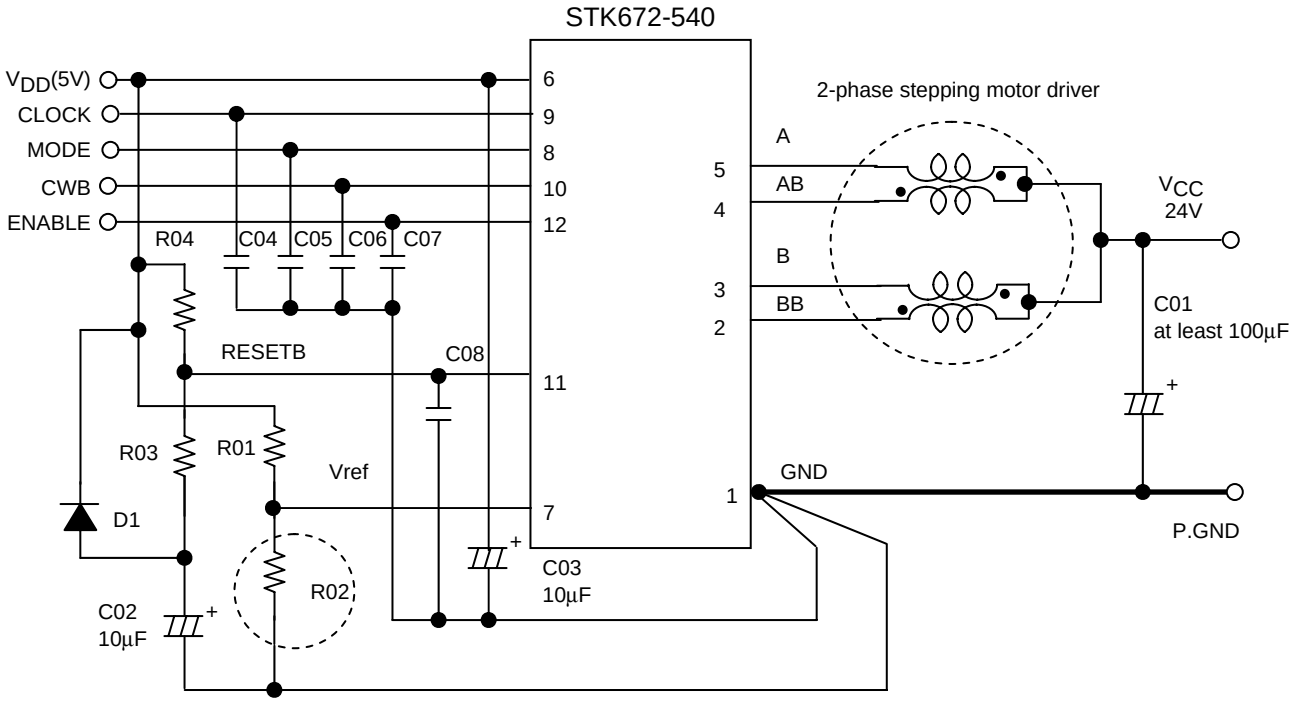
Notes

- The current range given above represents conditions when output voltage is not in the avalanche state.
- If the output voltage is in the avalanche state, see the allowable avalanche energy for STK672-5** series hybrid ICs given in a separate document.
- The operating substrate temperature, Tc, given above is measured while the motor is operating.
  Because Tc varies depending on the ambient temperature, Ta, the value of I_{OH}, and the continuous or intermittent operation of I_{OH}, always verify this value using an actual set.

Block Diagram



Sample Application Circuit



R02 is normally open.

Precautions

[GND wiring]

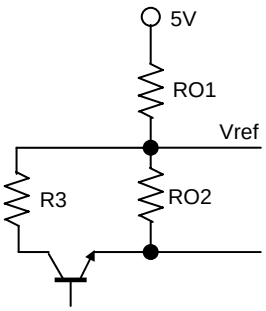
- To reduce noise on the 5V system, be sure to place the GND of C01 in the circuit given above as close as possible to Pin 1 of the hybrid IC. Also, the GND side of RO2 must be directly wired from P.GND terminal Pin 1 in order to accurately set the current.

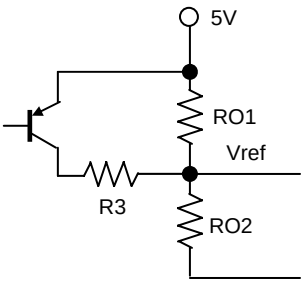
[Input pins]

- Insert resistor RO3 (47 to 100Ω) so that the discharge energy from capacitor CO2 is not directly applied to the CMOS IC in this hybrid device. If the diode D1 has Vf characteristics with Vf less than or equal to 0.6V (when If = 0.1A), this will be smaller than the CMOS IC input pin diode Vf. If this is the case RO3 may be replaced with a short without problem.
- Apply 2.5V High level input to pins 8, 9, 10, 11, and 12.
- If V_{DD} is being applied, use care that each input pin does not apply a negative voltage less than -0.3V to P.GND, Pin 1, and do not apply a voltage greater than or equal to V_{DD} voltage.
- Since the input pins do not have built-in pull-up resistors, when the open-collector type pins 8, 9, 10, 11, and 12 are used as inputs, a 10 to 47kΩ pull-up resistor (to V_{DD}) must be used.
  At this time, use a device for the open collector driver that has output current specifications that pull the voltage down to less than 0.6V at Low level.
- To prevent malfunction due to chopping noise, we recommend that you mount a 1000pF capacitor between Pin 1 and each of the input Pins 8, 9, 10, 11, and 12. Be sure to mount the capacitor as close as possible to the pins of hybrid IC.
  If input is fixed Low, directly connect to Pin 1.
  If input is fixed High, directly connect to the 5V power line.

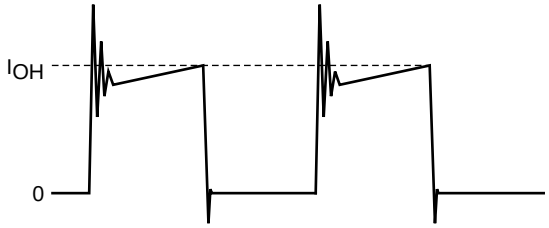
[Current setting Vref]

- In consideration of the specifications of the Vref input bias current, I_{IB}, a resistance from several kΩ to 100kΩ is recommended for RO1.
- If the motor current is temporarily reduced, the circuit given below (STK672-540: I_{OH}>0.25A) is recommended.
- Although the driver is equipped with a fixed current control function, it is not equipped with an overcurrent protection function to ensure that the current does not exceed the maximum output current, I_{OH} max. If Vref is mistakenly set to a voltage that exceeds I_{OH} max, the driver will be damaged by overcurrent.





• Motor current peak value I_{OH} setting



• When RO2 is open

I_{OH}= [Vref×1k/(1k+3.9k)] ÷Rs= (Vref÷4.9) ÷Rs

The values 1k and 3.9k represent internal driver resistance values, while Rs represents the internal driver current detection resistance.

Vref= (4.9k÷ (4.9k+RO1)) ×5V (or 3.3V) =I_{OH}×4.9×Rs

The value 4.9k represents the series resistance value of the internal driver values of 1k and 3.9k.

• If RO2 is connected

I_{OH}= [Vref×1k/ (1k+3.9k)] ÷Rs= (Vref÷4.9) ÷Rs

The values 1k and 3.9k represent the internal driver resistance values, while Rs represents the internal driver current detection resistance.

Vref= (R0x÷ (RO1+R0x)) ×5V (or 3.3V) =I_{OH}×4.9×Rs

= [(4.9k×RO2) ÷ ((4.9k×RO2) +RO1× (4.9k+RO2))] ×5V(or 3.3V)

R0x= (4.9k×RO2) ÷ (4.9k+RO2)

Rs represents the current detection resistance inside the HIC, while the value 4.9k in the formula above represents the internal resistance value of the Vref pin.

Rs=0.165Ω when using the STK672-530

Rs=0.11Ω when using the STK672-540

[Smoke Emission Precuations]

If any of the output pins 2, 3, 4, and 5 is held open, the electrical stress onto the driver due to the inductive energy accumulated in the motor could cause short-circuit followed by permanent damage to the internal MOSFET. As a result, the STK672-540 may give rise to emit smoke.

Input Pin Functions

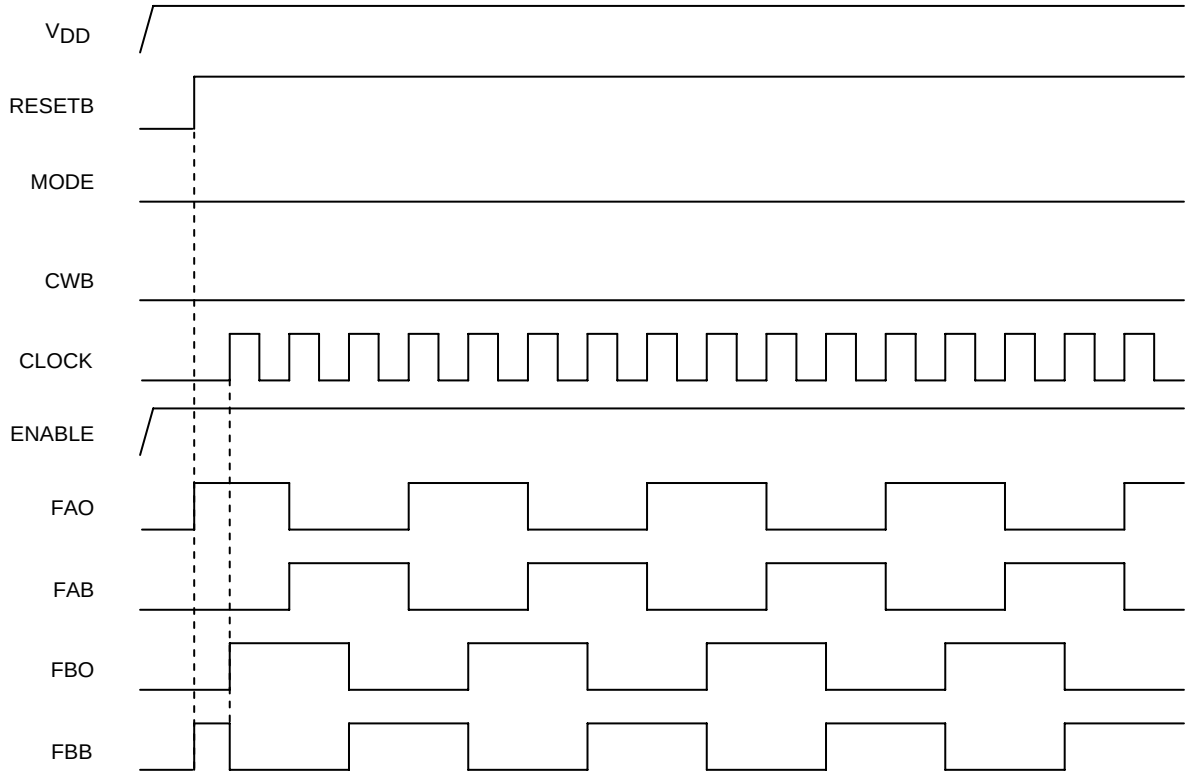
Pin Name	Pin No.	Function	Input Conditions When Operating
CLOCK	9	Reference clock for motor phase current switching	Operates on the rising edge of the signal
MODE	8	Excitation mode selection	Low: 2-phase excitation High: 1-2 phase excitation
CWB	10	Motor direction switching	Low: CW (forward) High: CCW (reverse)
RESETB	11	System reset and A, AB, B, and BB outputs cutoff. Applications must apply a reset signal for at least 10μs when V_{DD} is first applied.	A reset is applied by a low level
ENABLE	12	The A, AB, B, and BB outputs are turned off, and after operation is restored by returning the ENABLE pin to the high level, operation continues with the same excitation timing as before the low-level input.	The A, AB, B, and BB outputs are turned off by a low-level input.

(1) A simple reset function is formed from D1, CO2, RO3, and RO4 in this application circuit. With the CLOCK input held low, when the 5V supply voltage is brought up a reset is applied if the motor output phases A and BB are driven. If the 5V supply voltage rise time is slow (over 50ms), the motor output phases A and BB may not be driven. Increase the value of the capacitor CO2 and check circuit operation again.

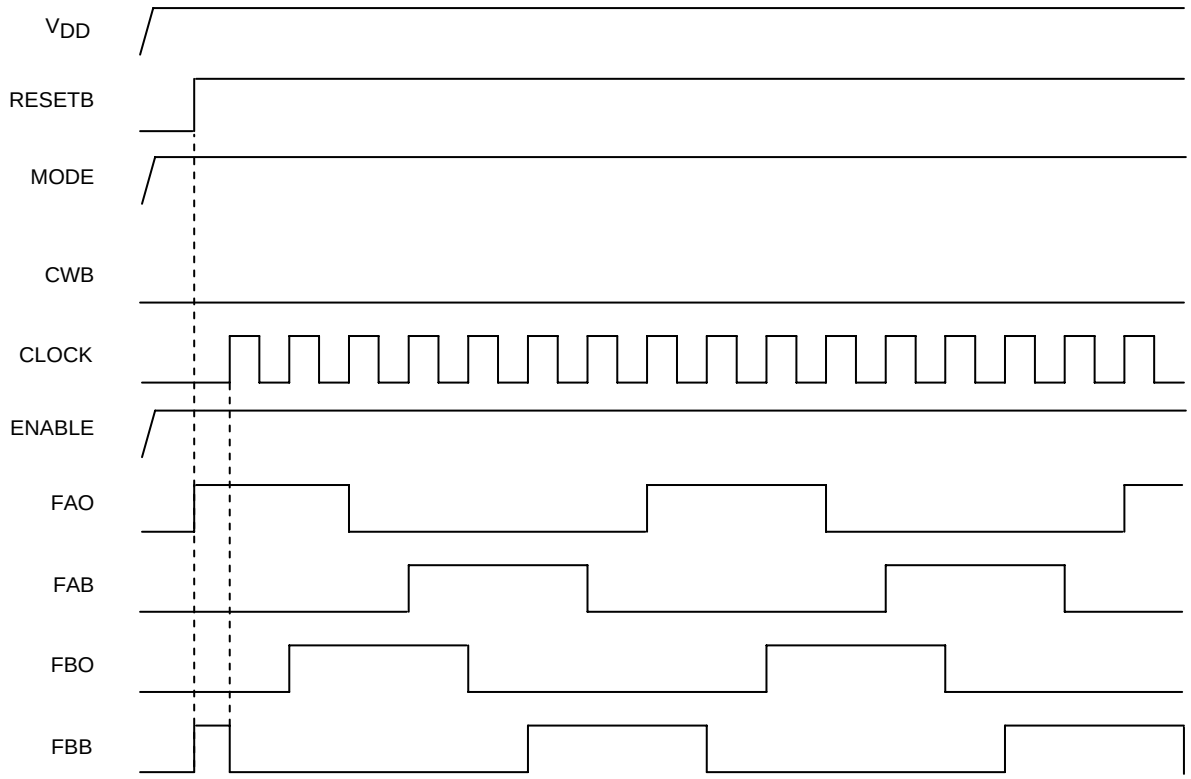
(2) See the timing chart for the concrete details on circuit operation.

Timing Charts

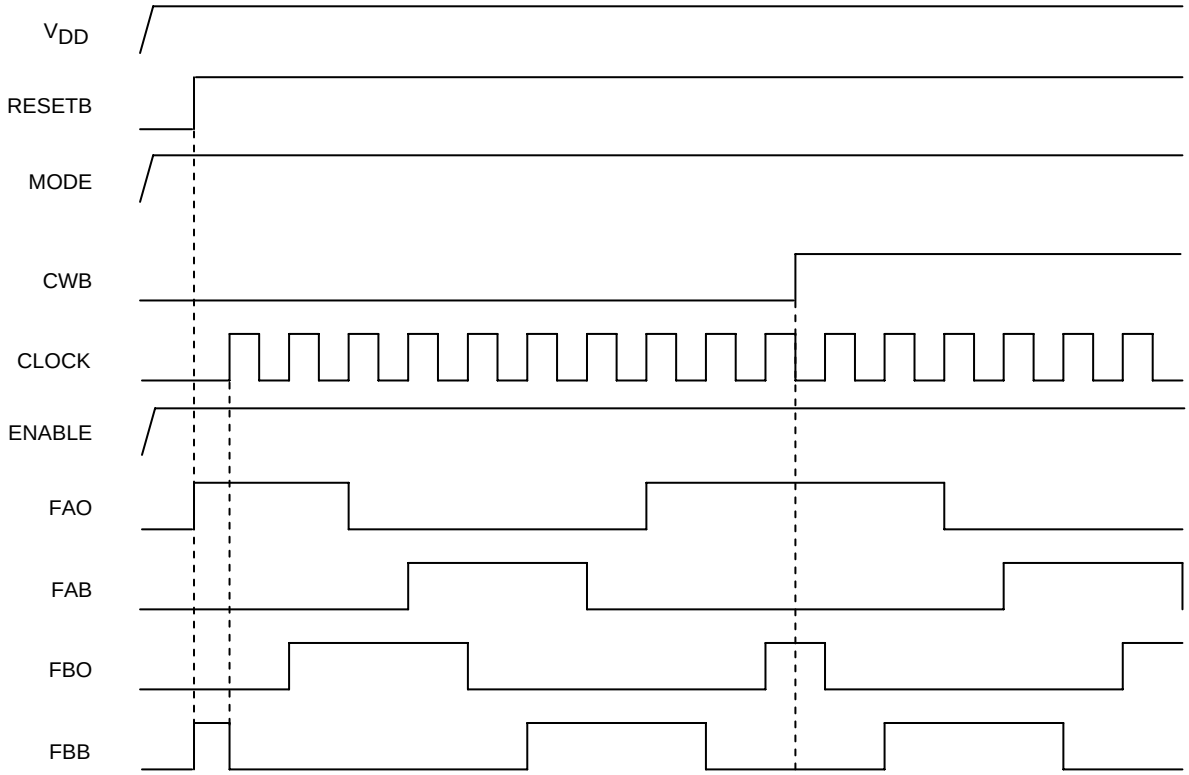
2-phase excitation



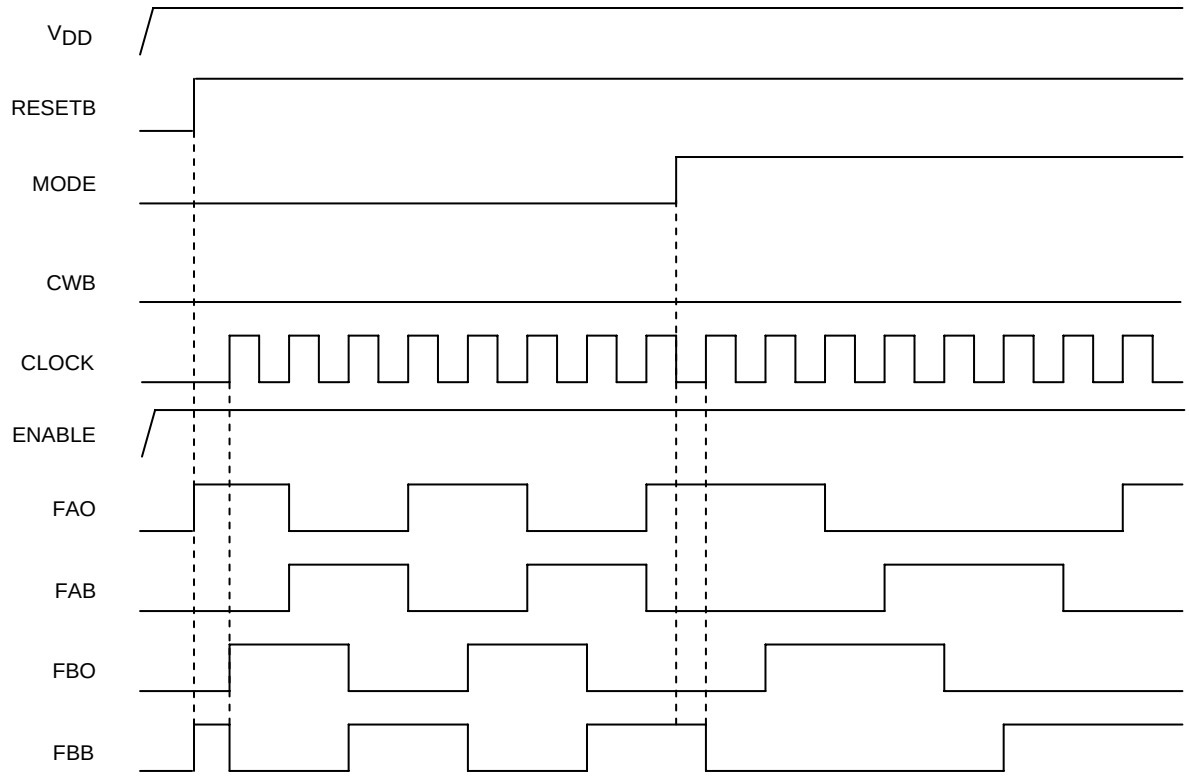
1-2 phase excitation



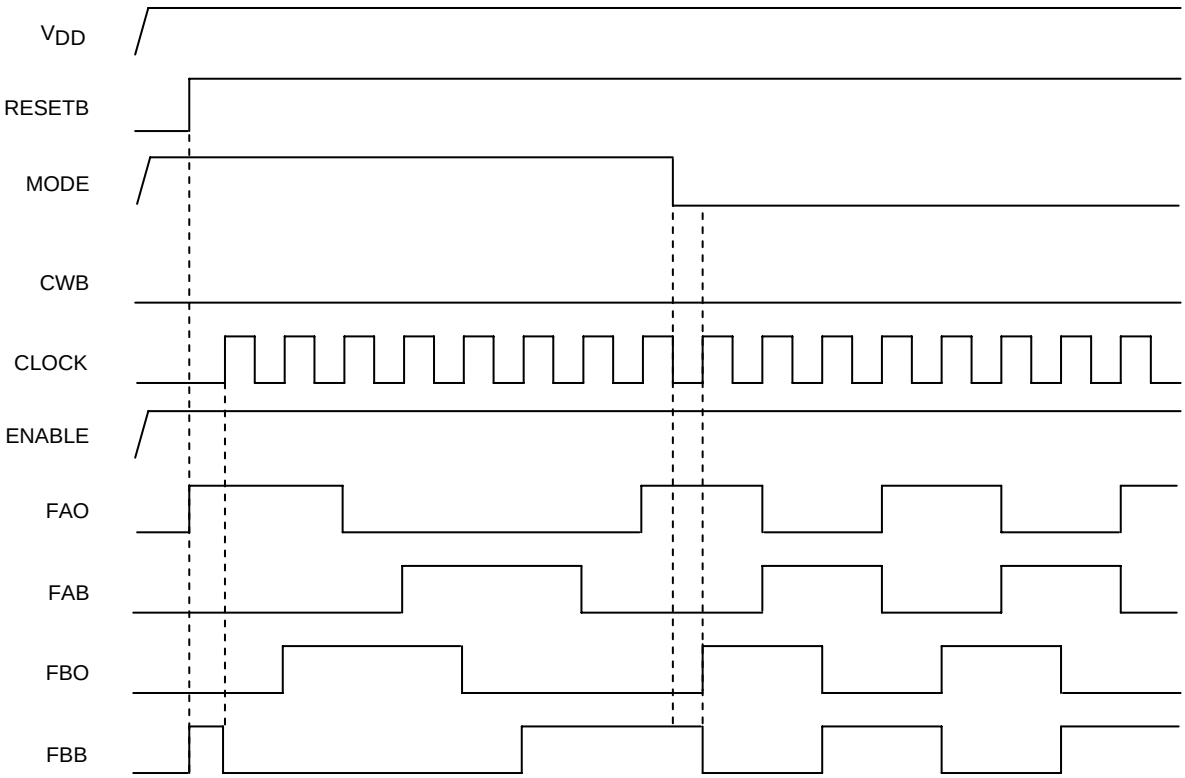
1-2 phase excitation



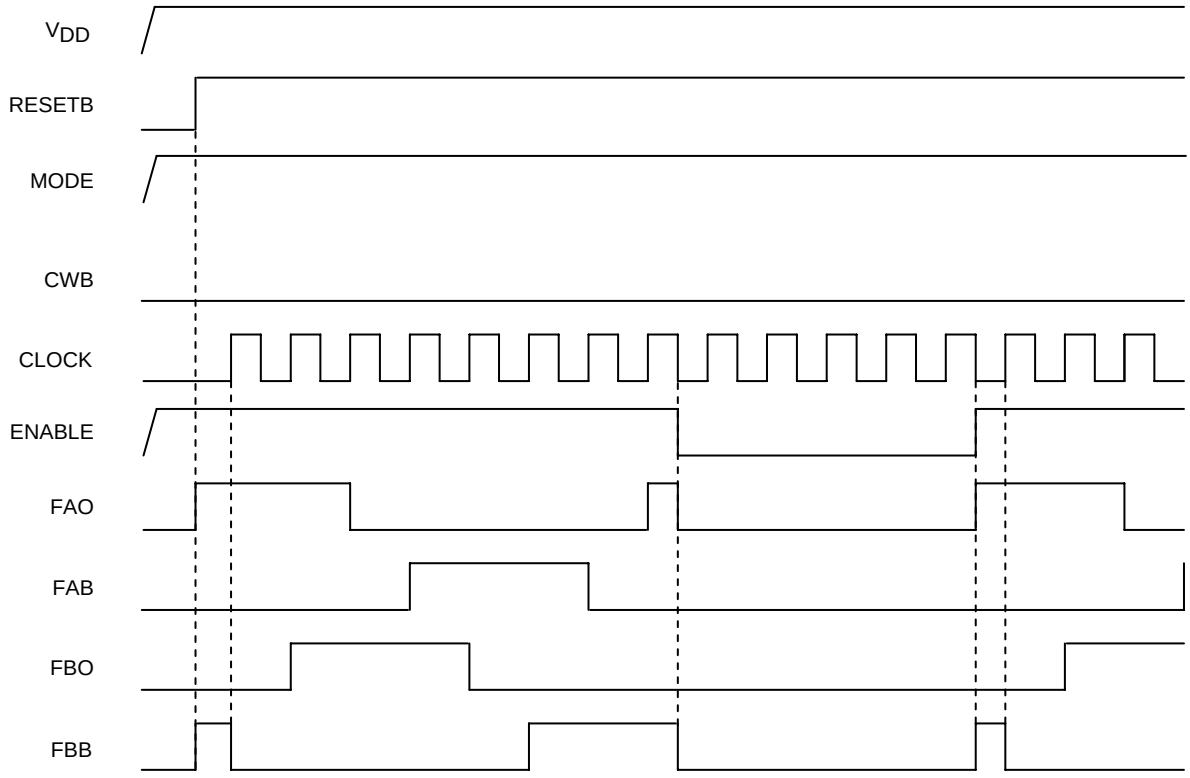
2-phase excitation→Switch to 1-2 phase excitation



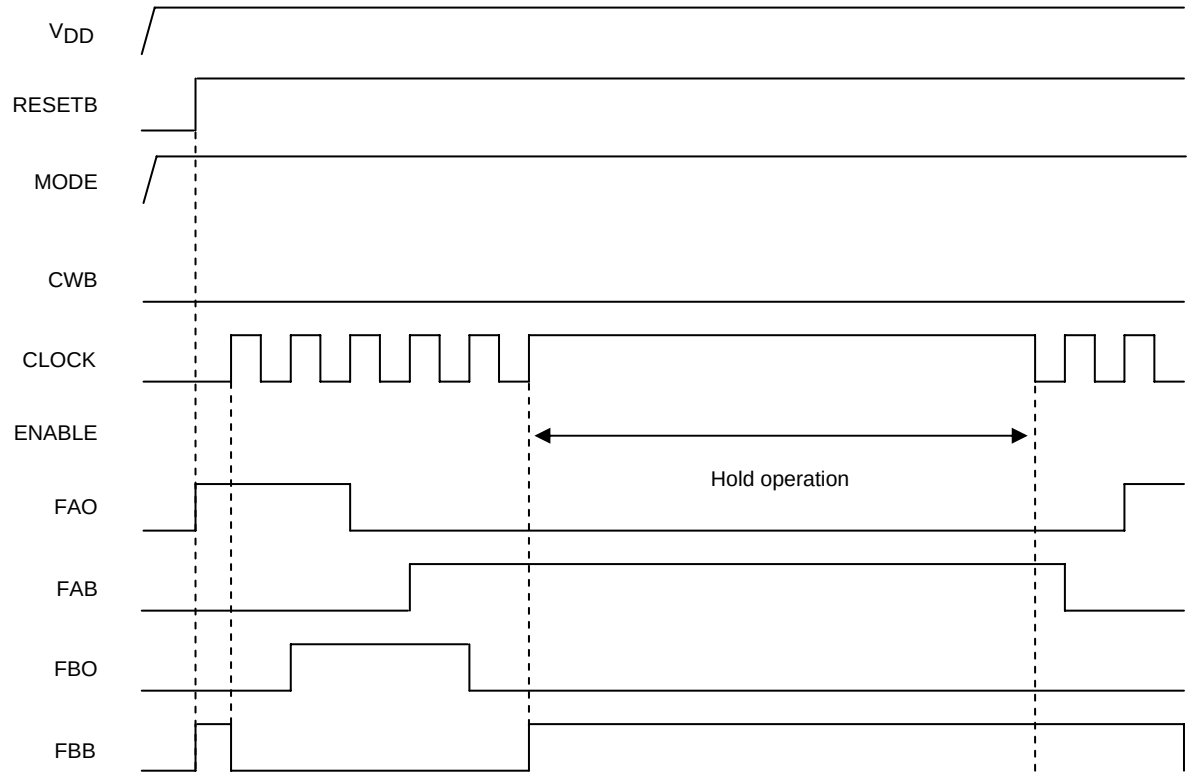
1-2-phase excitation→Switch to 2 phase excitation



1-2 phase excitation (ENABLE)



1-2 phase excitation (Hold operation results during fixed CLOCK)



Usage Notes

1. STK672-530 and STK672-540 input signal functions and timing
   (All inputs have no internal pull-up resistor.)

[RESETB and CLOCK (Input signal timing when power is first applied)]

As shown in the timing chart, a RESETB signal input is required by the driver to operate with the timing in which the F1 gate is turned on first. The RESETB signal timing must be set up to have a width of at least 10μs, as shown below. The capacitor CO2, and the resistors RO3 and RO4 in the application circuit form simple reset circuit that uses the RC time constant rising time. However, when designing the RESETB input based on V_{IH} levels, the application must have the timing shown in figure.

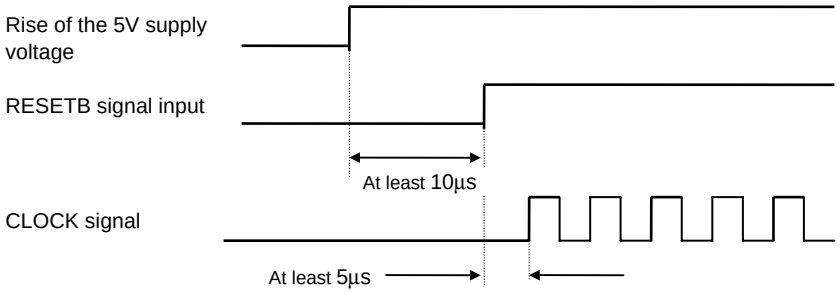


Figure 1 RESETB and CLOCK Signals Input Timing

[CLOCK (Phase switching clock)]

- Input frequency: DC to 50kHz
- Minimum pulse width: 10μs
- Signals are read on the rising edge.

[CWB (Motor direction setting)]

The direction of rotation is switched by setting CWB to 1 (high) or 0 (low).
See the timing charts for details on the operation of the outputs.
Note: The state of the CWB input must not be changed during the 6.25μs period before and after the rising edge of the CLOCK input.

[ENABLE (Controls forced OFF for A, AB, B, and selects BB and selects operation/hold mode of the hybrid IC)]

ENABLE=1: Normal operation
ENABLE=0: Outputs A, AB, B, and BB forced to the off state.
If, during the state where CLOCK signal input is provided, the ENABLE pin is set to 0 and then is later restored to the 1 state, the IC will resume operation with the excitation timing continued from before the point ENABLE was set to 0.
Enable must be initially set high for input as shown in the timing chart.

[MODE (Excitation mode selection)]

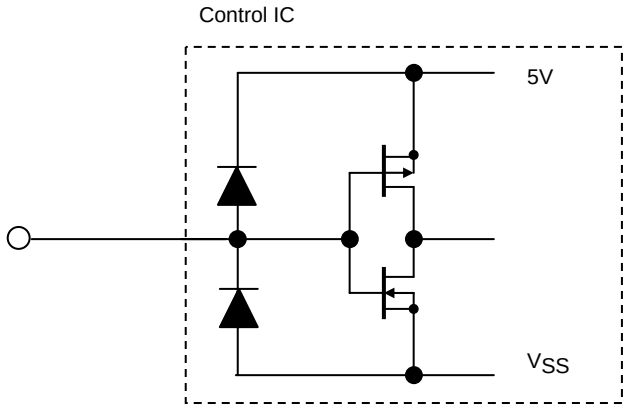
MODE=0: 2-phase excitation
MODE=1: 1-2 phase excitation
See the timing charts for details on output operation in these modes.

Note: The state of the MODE input must not be changed during the 5μs period before and after the rising edge of the CLOCK input.

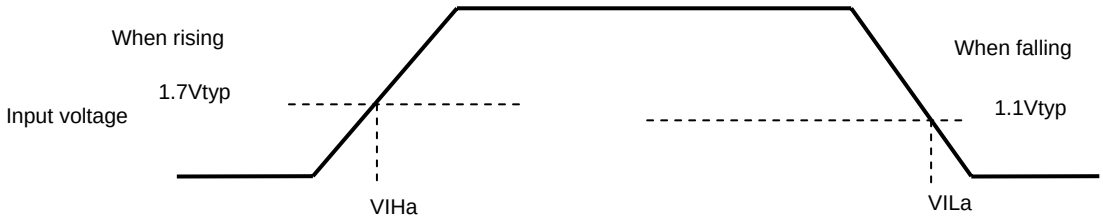
[Configuration of Each Input Pin]

<Configuration of the MODE, CLOCK, CWB, RESETB, and ENABLE input pins>

Input pins: Pin 8, 9, 10, 11, and 12



All input pins of this driver support schmitt input. Typ specifications at Tc = 25°C are given below. Hysteresis voltage is 0.6V (VIHa-VILa).



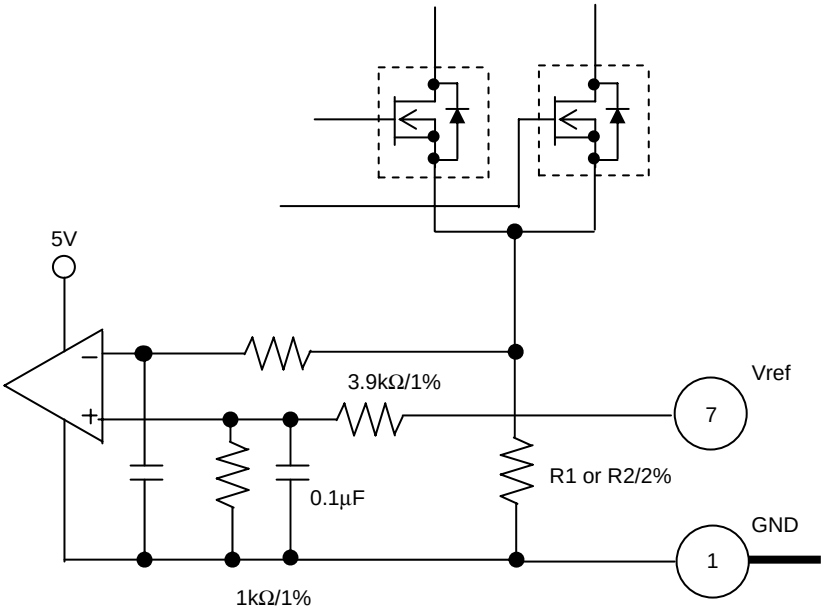
Input voltage specifications are as follows.

V_{IH}=2.5V min

V_{IL}=0.6V max

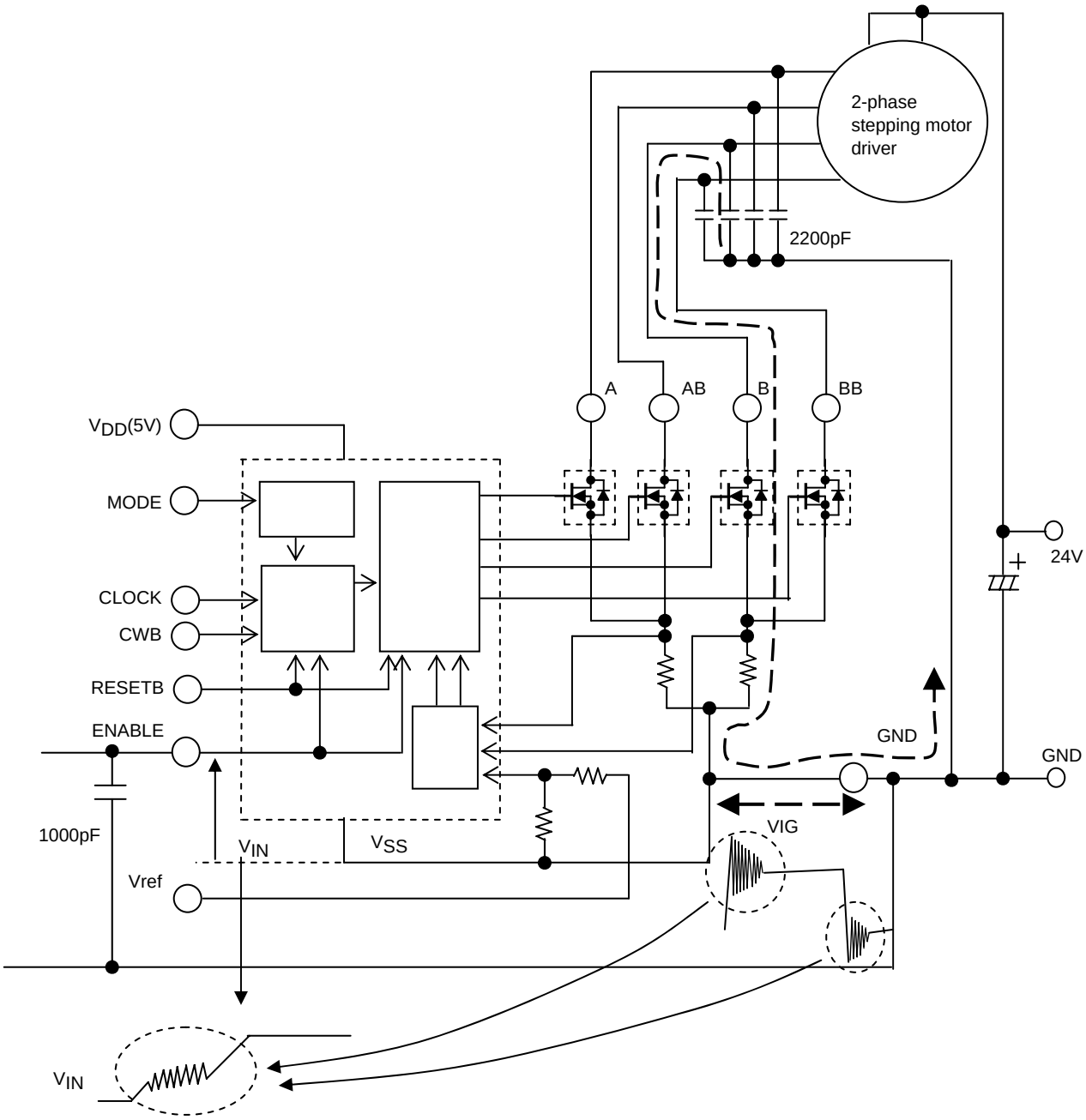
<Configuration of the Vref Input Pin>

Input pin: Pin 7



<Precautions for Input Signal>

Because the ringing voltage VIG of the GND line is added to the input signals inside the hybrid IC, the greater the through rate of input signals, the more opportunities there are to input a ringing signal at the rising or falling edge. Particularly in cases where a capacitor is added to output pins 2, 3, 4, and 5 as shown in the figure below to suppress electromagnetic noise, the ringing voltage increases even further due to charge/discharge of the capacitor. The ringing voltage amplitude of this type may exceed 0.6V input Hysteresis voltage. Because the ringing signal can cause a malfunction leading to failure due to over-current, be sure to apply input signals with the highest through rate possible. Direct input with HC type CMOS ICs is recommended.



2. Calculating STK672-540 HIC Internal Power Loss

The average internal power loss in each excitation mode of the STK672-540 can be calculated from the following formulas.

Each excitation mode
2-phase excitation mode
$2PdAVex = (Vsat+Vdf) \times 0.5 \times CLOCK \times I_{OH} \times t2 + 0.5 \times CLOCK \times I_{OH} \times (Vsat \times t1 + Vdf \times t3)$

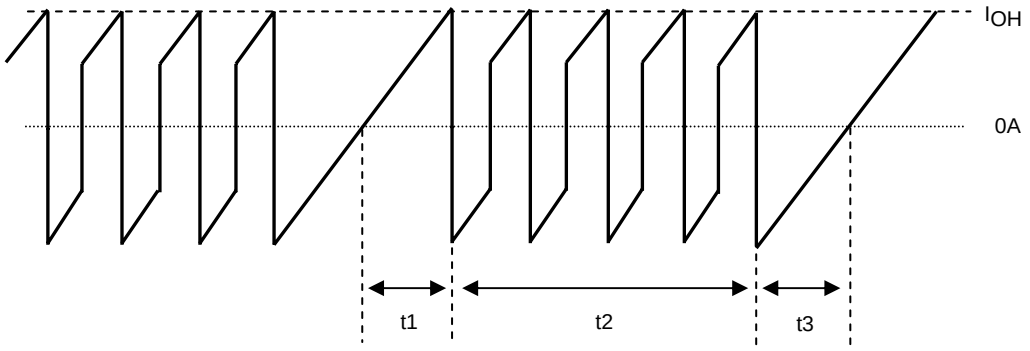
1-2 phase excitation mode
$1\text{-}2PdAVex = (Vsat+Vdf) \times 0.25 \times CLOCK \times I_{OH} \times t2 + 0.25 \times CLOCK \times I_{OH} \times (Vsat \times t1 + Vdf \times t3)$

Motor hold mode
$HoldPdAVex = (Vsat+Vdf) \times I_{OH}$

Vsat: Combined voltage represented by the Ron voltage drop+shunt resistor
Vdf: Combined voltage represented by the MOSFET body diode+shunt resistor
CLOCK: Input CLOCK (CLOCK pin signal frequency)

t1, t2, and t3 represent the waveforms shown in the figure below.

t1: Time required for the winding current to reach the set current (I_{OH})
t2: Time in the constant current control (PWM) region
t3: Time from end of phase input signal until inverse current regeneration is complete



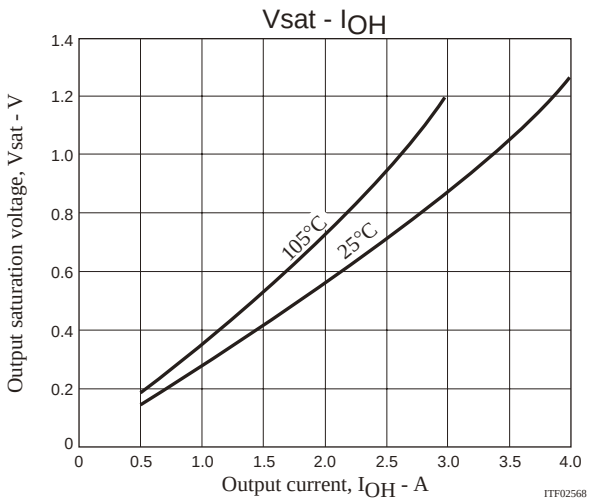
Motor COM Current Waveform Model

$t1 = (-L/(R+0.28)) \ln (1-((R+0.28)/V_{CC}) \times I_{OH})$
$t3 = (-L/R) \ln ((V_{CC}+0.28)/(I_{OH} \times R + V_{CC}+0.28))$
V_{CC}: Motor supply voltage (V)
L: Motor inductance (H)
R: Motor winding resistance (Ω)
I_{OH}: Motor set output current crest value (A)

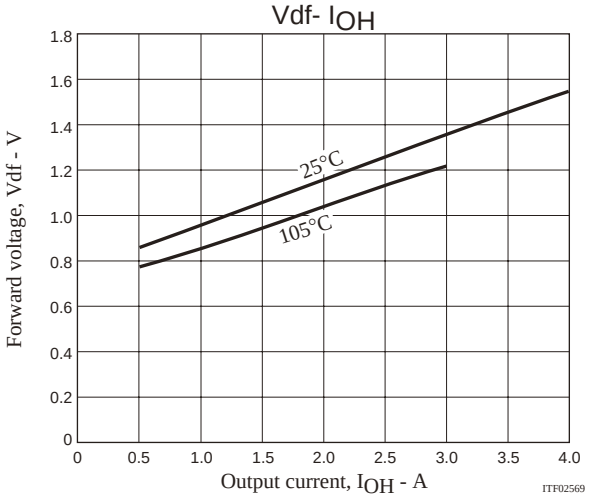
Relationship of CLOCK, t1, t2, and t3 in each excitation mode
2-phase excitation mode: t2= (2/CLOCK) - (t1+t3)
1-2 phase excitation mode: t2= (3/CLOCK) -t1

For Vsat and Vdf, be sure to substitute values from the graphs of Vsat vs. I_{OH} and Vdf vs. I_{OH} while the set current value is I_{OH}.
Then, determine whether a heat sink is required by comparing with the graph of ΔTc vs. Pd based on the average HIC power loss calculated.
When designing a heat sink, refer to the section “Thermal design” found on the next page. The average HIC power loss, PdAV, described above does not have the avalanche’s loss. To include the avalanche’s loss, be sure to add Equation (2), “STK672-5** Allowable Avalanche Energy Value” to PdAV above. When using this IC without a fin always check for temperature increases in the set, because the HIC substrate temperature, Tc, varies due to effects of convection around the HIC.

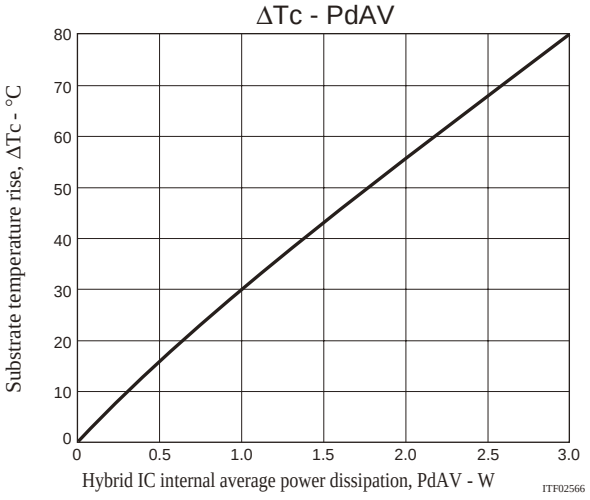
STK672-540 Output saturation voltage, Vsat - Output current, I_{OH}



STK672-540 Forward voltage, Vdf -Output current, I_{OH}



Substrate temperature rise , ΔTc (no heat sink) - Internal average power dissipation, PdAV



3. STK672-540 Allowable Avalanche Energy Value

(1) Allowable Range in Avalanche Mode

When driving a 2-phase stepping motor with constant current chopping using an STK672-5** Series hybrid IC, the waveforms shown in Figure 1 below result for the output current, I_D, and voltage, V_{DS}.

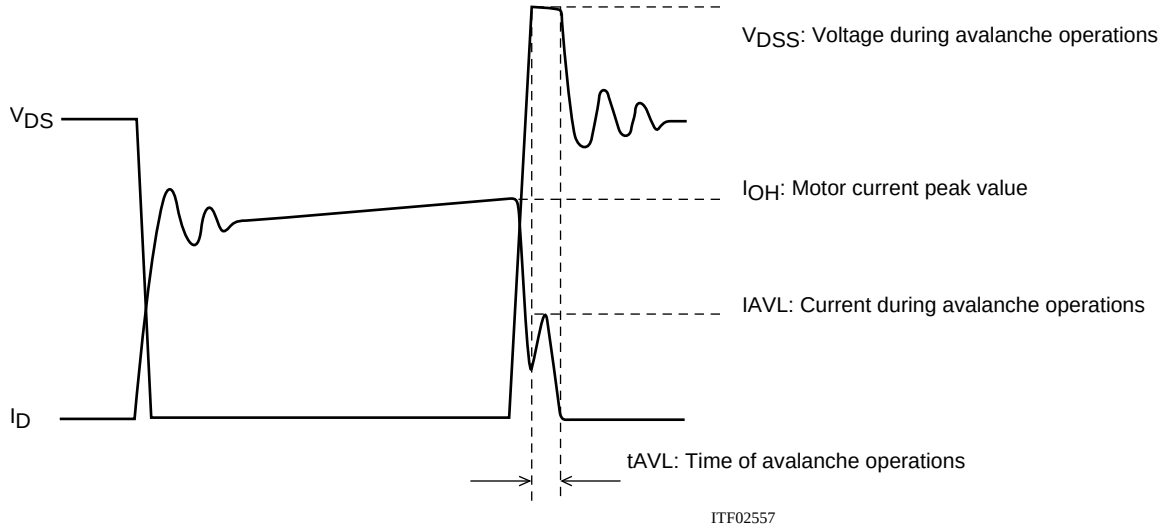


Figure 1 Output Current, I_D, and Voltage, V_{DS}, Waveforms 1 of the STK672-5** Series when Driving a 2-Phase Stepping Motor with Constant Current Chopping

When operations of the MOSFET built into STK672-5** Series ICs is turned off for constant current chopping, the I_D signal falls like the waveform shown in the figure above. At this time, the output voltage, V_{DS}, suddenly rises due to electromagnetic induction generated by the motor coil.

In the case of voltage that rises suddenly, voltage is restricted by the MOSFET V_{DSS}. Voltage restriction by V_{DSS} results in a MOSFET avalanche. During avalanche operations, I_D flows and the instantaneous energy at this time, EAVL1, is represented by Equation (1).

$$EAVL1=V_{DSS}\times IAVL\times 0.5\times tAVL \quad \text{---------- (1)}$$

V_{DSS}: V units, IAVL: A units, tAVL: sec units

The coefficient 0.5 in Equation (1) is a constant required to convert the IAVL triangle wave to a square wave.

During STK672-5** Series operations, the waveforms in the figure above repeat due to the constant current chopping operation. The allowable avalanche energy, EAVL, is therefore represented by Equation (2) used to find the average power loss, PAVL, during avalanche mode multiplied by the chopping frequency in Equation (1).

$$PAVL=V_{DSS}\times IAVL\times 0.5\times tAVL\times fc \quad \text{---------- (2)}$$

fc: Hz units (fc is set to the PWM frequency of 50kHz.)

For V_{DSS}, IAVL, and tAVL, be sure to actually operate the STK672-5** Series and substitute values when operations are observed using an oscilloscope.

Ex. If V_{DSS}=110V, IAVL=1A, tAVL=0.2μs when using a STK672-540 driver, the result is:

$PAVL=110\times 1\times 0.5\times 0.2\times 10^{-6}\times 50\times 10^{3}=0.55W$

V_{DSS}=110V is a value actually measured using an oscilloscope.

The allowable loss range for the allowable avalanche energy value, PAVL, is shown in the graph in Figure 3. When examining the avalanche energy, be sure to actually drive a motor and observe the I_D, V_{DSS}, and tAVL waveforms during operation, and then check that the result of calculating Equation (2) falls within the allowable range for avalanche operations.

(2) I_D and V_{DSS} Operating Waveforms in Non-avalanche Mode

Although the waveforms during avalanche mode are given in Figure 1, sometimes an avalanche does not result during actual operations.

Factors causing avalanche are listed below.

- Poor coupling of the motor's phase coils (electromagnetic coupling of A phase and AB phase, B phase and BB phase).
- Increase in the lead inductance of the harness caused by the circuit pattern of the P.C. board and motor.
- Increases in V_{DSS}, tAVL, and IAVL in Figure 1 due to an increase in the supply voltage from 24V to 36V.

If the factors above are negligible, the waveforms shown in Figure 1 become waveforms without avalanche as shown in Figure 2.

Under operations shown in Figure 2, avalanche does not occur and there is no need to consider the allowable loss range of PAVL shown in Figure 3.

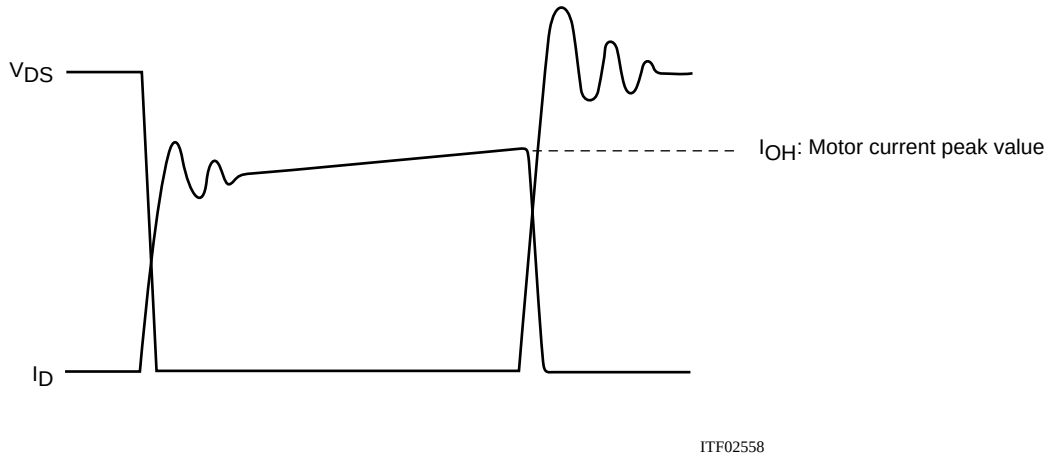
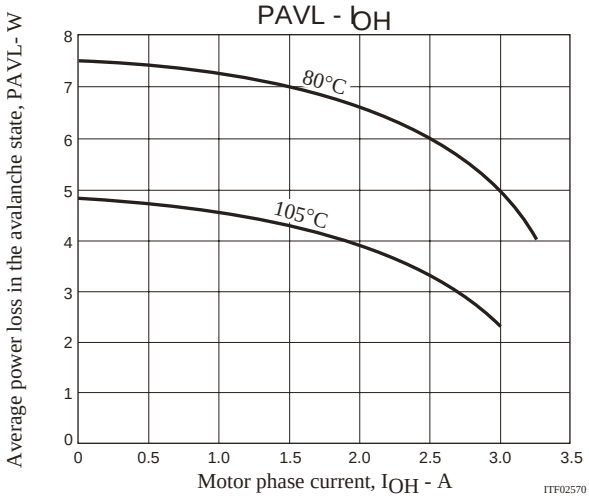


Figure 2 Output Current, I_D, and Voltage, V_{DS}, Waveforms 2 of the STK672-5** Series when Driving a 2-Phase Stepping Motor with Constant Current Chopping

Figure 3 Allowable Loss Range, PAVL-I_{OH} During STK672-540 Avalanche Operations



Note:

The operating conditions given above represent a loss when driving a 2-phase stepping motor with constant current chopping.

Because it is possible to apply 4.8W or more at I_{OH}=0A, be sure to avoid using the MOSFET body diode that is used to drive the motor as a zener diode.

4. Thermal design

[Operating range in which a heat sink is not used]

Use of a heat sink to lower the operating substrate temperature of the HIC (Hybrid IC) is effective in increasing the quality of the HIC.

The size of heat sink for the HIC varies depending on the magnitude of the average power loss, PdAV, within the HIC. The value of PdAV increases as the output current increases. To calculate PdAV, refer to "Calculating Internal HIC Loss for the STK672-540" in the specification document.

Calculate the internal HIC loss, PdAV, assuming repeat operation such as shown in Figure 1 below, since conduction during motor rotation and off time both exist during actual motor operations.

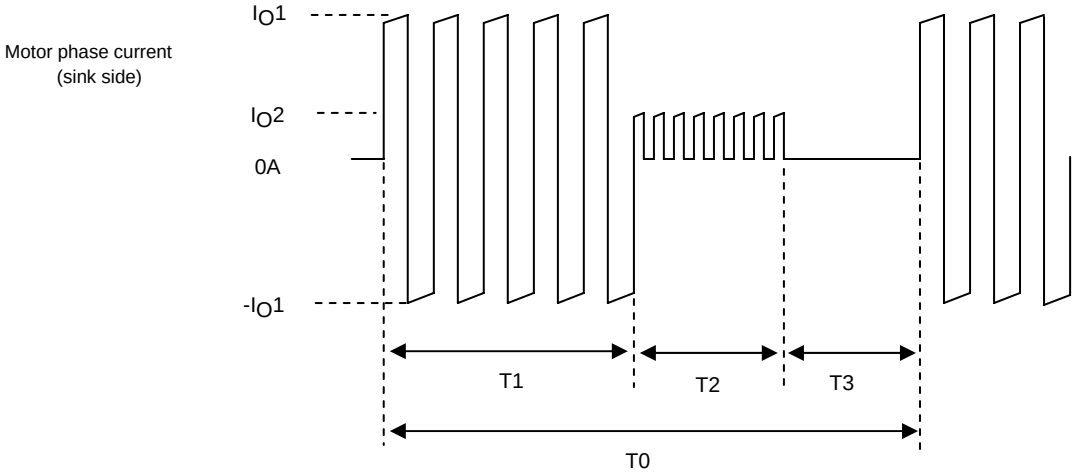


Figure 1 Motor Current Timing

T1: Motor rotation operation time
T2: Motor hold operation time
T3: Motor current off time
T2 may be reduced, depending on the application.
T0: Single repeated motor operating cycle
I_O1 and I_O2: Motor current peak values
Due to the structure of motor windings, the phase current is a positive and negative current with a pulse form.
Note that figure 1 presents the concepts here, and that the on/off duty of the actual signals will differ.
The hybrid IC internal average power dissipation PdAV can be calculated from the following formula.

PdAV= (T1×P1+T2×P2+T3×0) ÷T0 ---------- (I)

(Here, P1 is the PdAV for I_O1 and P2 is the PdAV for I_O2)

If the value calculated using Equation (I) is 1.5W or less, and the ambient temperature, Ta, is 60°C or less, there is no need to attach a heat sink. Refer to Figure 2 for operating substrate temperature data when no heat sink is used.

[Operating range in which a heat sink is used]

Although a heat sink is attached to lower Tc if PdAV increases, the resulting size can be found using the value of θc-a in Equation (II) below and the graph depicted in Figure 3.

θc-a= (Tc max-Ta) ÷PdAV ---------- (II)

Tc max: Maximum operating substrate temperature =105°C

Ta: HIC ambient temperature

Although a heat sink can be designed based on equations (I) and (II) above, be sure to mount the HIC in a set and confirm that the substrate temperature, Tc, is 105°C or less.

The average HIC power loss, PdAV, described above represents the power loss when there is no avalanche operation. To add the loss during avalanche operations, be sure to add Equation (2), "Allowable STK672-5** Avalanche Energy Value", to PdAV.

Figure 2 Substrate temperature rise, ΔTc - Internal average power dissipation, PdAV

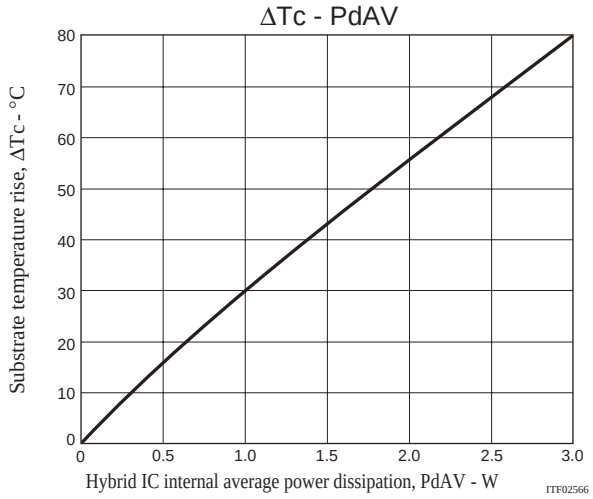
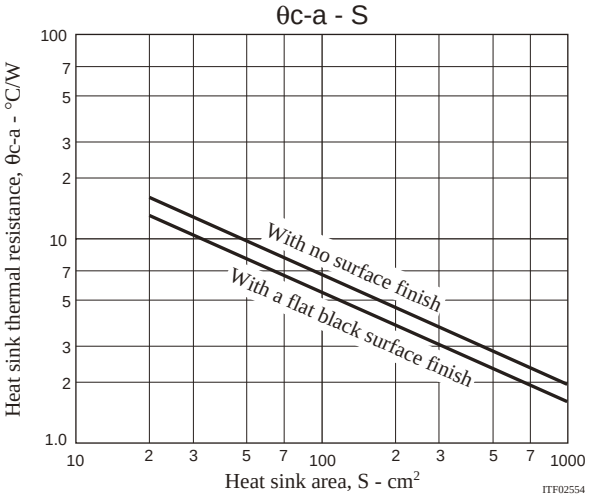
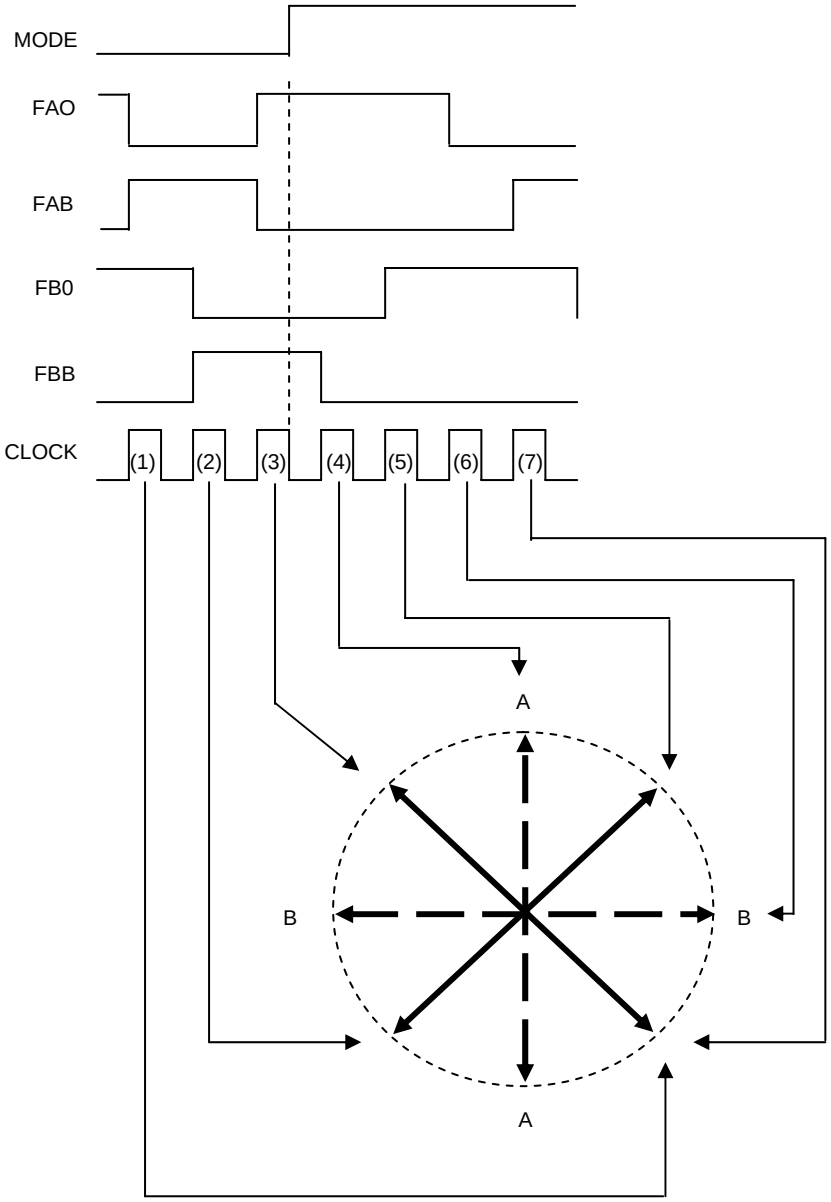


Figure 3 Heat sink area (Board thickness: 2mm) - θc-a



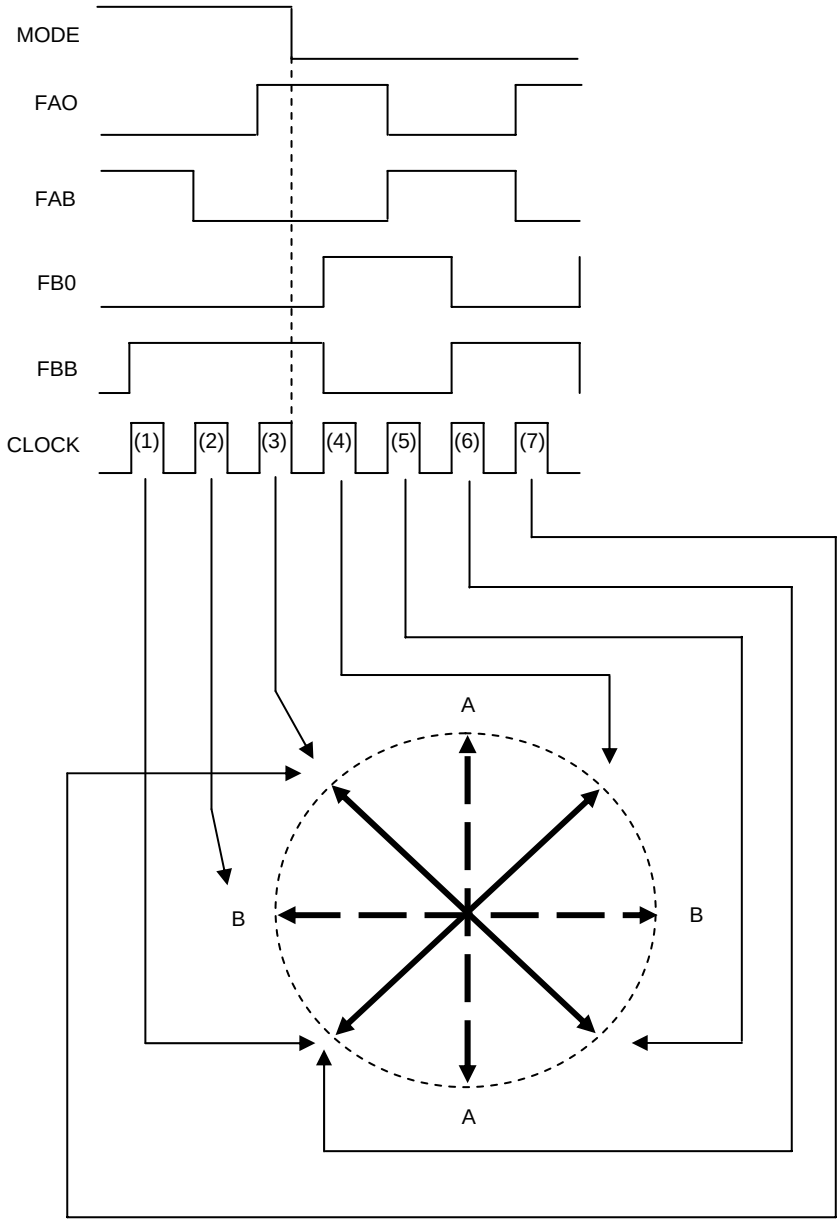
5. Changes in motor state when switching excitation with STK672-5** Series

Example 1: Switching from 2-phase to 1-2 phase excitation
Motor status is maintained when the excitation mode (MODE) is switched during motor rotation.
Because CLOCK cannot be detected when the interval between the rise in the MODE and CLOCK signals is 5μs or less, the mode may not change for one CLOCK cycle.



The solid arrows indicate 2-phase excitation, and dashed arrows indicate 1-phase excitation.

Example 2: Switching from 1-2 phase to 2-phase excitation
Motor status is maintained when the excitation mode (MODE) is switched during motor rotation.
Because CLOCK cannot be detected when the interval between the rise in the MODE signal and CLOCK signal is 5µs or less, the mode may not change for one CLOCK cycle.



The solid arrows indicate 2-phase excitation, and dashed arrows indicate 1-phase excitation.