

## Bluetooth EDR and RDS FM radio tuner

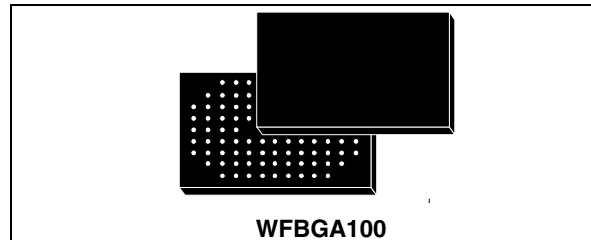
Data Brief

### Features

- WFBGA 5.0 x 7.5 x 0.8 mm lead-free/RoHS compliant 100 pins
- Only 1 external component required
- PCB footprint < 45 mm<sup>2</sup>

### Bluetooth features

- Based on Ericsson Technology Licensing Baseband Core (EBC)
- Bluetooth™ specification compliance: V2.1 (“Lisbon”) + EDR
- HW support for packet types ACL, SCO, eSCO
- Adaptive Frequency Hopping (AFH)
- Channel Quality Driven Data Rate (CQDDR)
- Power Class 2 and Power Class 1.5 (above 4 dBm) transmit power
- HCI H4 and enhanced H4 Transport Layer
- Implements Pitch-Period Error Concealment (PPEC)
- Fully flexible support for a wide range of WLAN and other co-existence scenarios
- Optimized Bluetooth and FM radio co-existence
- Low power consumption
- Ultra low power architecture with 3 different low-power levels
- Dual wake-up mechanism
- Communication interfaces: UART, SPI, PCM...
- ARM7TDMI™ CPU
- On-chip RAM, on-chip ROM
- Supports 1.65 V to 2.85 V I/O systems
- Auto calibration (VCO, Filters)



### FM radio features

- Worldwide FM band support (76-108 MHz)
- RDS/RBDS processor
- Line-level analog FM output
- 2-wire and 3-wire control interface
- 2.7 V to 5.5 V supply voltage
- 32.768 kHz reference clock
- Digital low-IF receiver
- Signal strength measurement
- Automatic Frequency Control (AFC)
- Automatic Gain Control (AGC)
- Excellent overload immunity and adaptive noise suppression

### Description

The STLC2593 combines Bluetooth and FM tuner functionality into one product and is fully optimized for mobile applications such as mobile phones, smart phones, PDAs and portable media players. The required board space has been minimized, only 1 external component is needed, power consumption levels are targeted for battery powered devices and the integration allows a cost-effective solution. The reduction of external components eases the integration of the STLC2593. Compared to its successful predecessor, the STLC2590, the STLC2593 supports the latest Bluetooth specification V2.1 (“Lisbon”) + EDR and further optimizes the RF performances and cost.

# 1 Overview

## 1.1 Bluetooth features

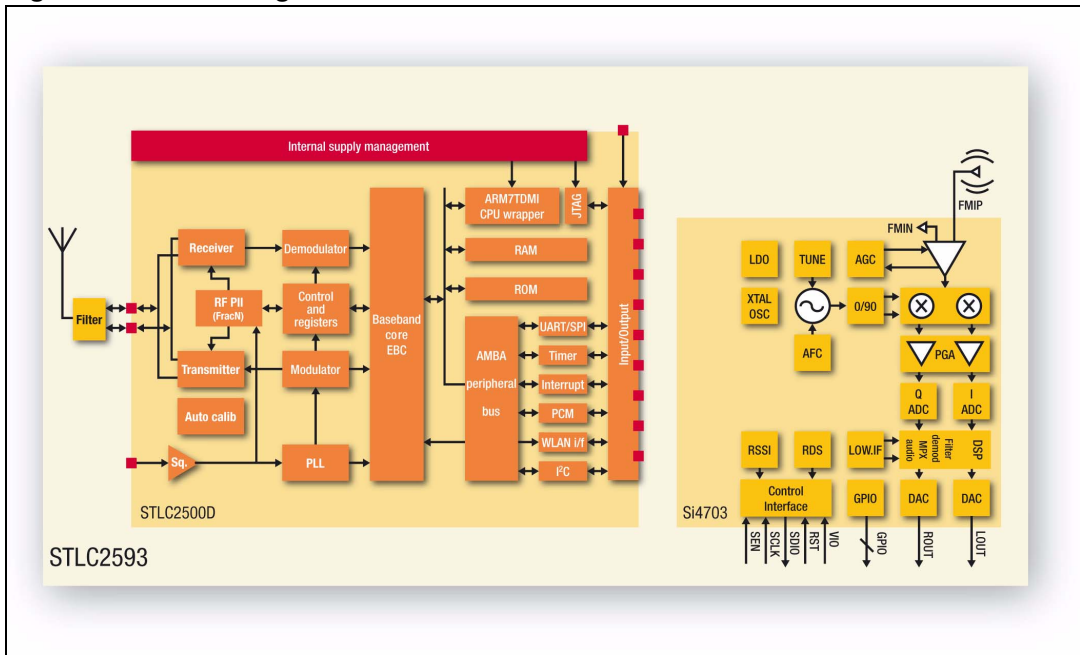
- Based on Ericsson Technology Licensing Baseband Core (EBC)
- Bluetooth™ specification compliance: V2.1 (“Lisbon”) + EDR
  - Point-to-point, point-to-multi-point (up to 7 slaves) and scatternet capability
  - Support ACL and SCO links
  - Extended SCO (eSCO) links
  - Faster connection
- “Lisbon” features
  - Encryption Pause/Resume (EPR)
  - Extended Inquiry Response (EIR)
  - Link Supervision Time Out (LSTO)
  - Secure simple pairing
  - Sniff subrating
  - Quality of Service (QoS)
    - Packet boundary flag
    - Erroneous data delivery
- HW support for packet types
  - ACL: DM1, DM3, DM5, DH1, DH3, DH5, 2-DH1, 2-DH3, 2-DH5, 3-DH1, 3-DH3, 3-DH5
  - SCO: HV1, HV3 and DV
  - eSCO: EV3, EV4, EV5, 2-EV3, 2-EV5, 3-EV3, 3-EV5
- Adaptive Frequency Hopping (AFH)
- Channel Quality Driven Data Rate (CQDDR)
- Transmit power
  - Power Class 2 and Power Class 1.5 (above 4 dBm)
  - Programmable output power
  - Power Class 1 compatible
- HCI
  - HCI H4 and enhanced H4 transport layer
  - HCI proprietary commands (e.g. peripherals control)
  - Single HCI command for patch/upgrade download
  - eSCO over HCI supported
- Implements Pitch-Period Error Concealment (PPEC)
- Fully flexible support for a wide range of WLAN and other co-existence scenarios
- Optimized Bluetooth and FM radio co-existence

- Low power consumption
  - Ultra low power architecture with 3 different low-power levels
  - Deep Sleep modes, including Host-power saving feature
  - Dual Wake-up mechanism: initiated by the Host or by the Bluetooth device
- Communication interfaces
  - Fast UART up to 4 MHz
  - Flexible SPI interface up to 13 MHz
  - PCM interface
  - Up to 10 additional flexibly programmable GPIOs
  - External interrupts possible through the GPIOs
  - Fast I<sup>2</sup>C interface as master
- Clock support
  - System clock input (digital or sine wave) at 9.6, 10, 13, 16, 16.8, 19.2, 26, 33.6 or 38.4 MHz
  - Low power clock input at 32.768 kHz
- ARM7TDMI™ CPU
- Memory organization
  - On chip RAM, including provision for patches
  - On chip ROM, preloaded with SW up to HCI
- Ciphering support up to 128 bits key
- Single power supply with internal regulators for core voltage generation
- Supports 1.65 V to 2.85 V I/O systems
- Auto calibration (VCO, Filters)

## 1.2 FM radio features

- Worldwide FM band support (76-108 MHz)
- RDS/RBDS processor
- Line-level analog FM output
- 2-wire and 3-wire control interface
- 2.7 V to 5.5 V supply voltage
  - Integrated LDO regulator allows direct connection to battery
- 32.768 kHz reference clock
  - Frequency synthesizer with integrated VCO
- Digital low-IF receiver
- Signal strength measurement
- Automatic Frequency Control (AFC)
- Automatic Gain Control (AGC)
- Excellent overload immunity
- Adaptive noise suppression

Figure 1. Block diagram



## 2 Ordering information

Table 1. Order codes

Part number	Package	Packing
E-STLC2593	WFBGA100	Tray
E-STLC2593TR	WFBGA100	Tape-on-reel

## 3 Revision history

Table 2. Document revision history

Date	Revision	Changes
22-Jan-2008	1	Initial release.

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