



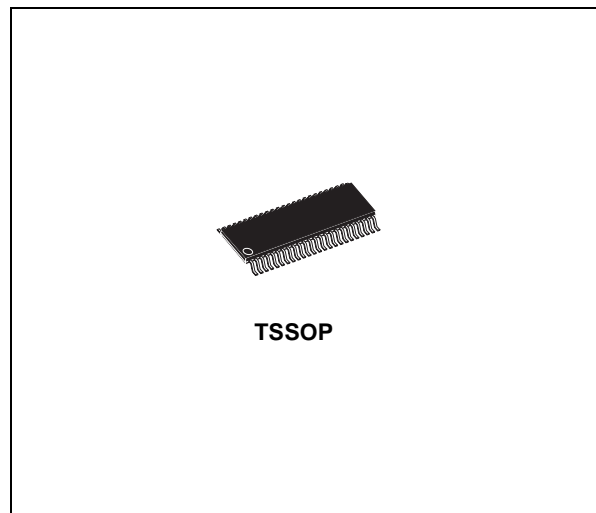
## HIGH SPEED PROTECTION SWITCH

- 24mA CMOS OUTPUT DRIVE CURRENT
- LVTTTL INPUT THRESHOLDS
- CONTROLLED SKEW BETWEEN DATA AND CLOCK SIGNALS
- LVDS INPUT-OUTPUT UP TO 155 MHZ
- IMPROVED LATCH-UP IMMUNITY UP TO 300mA

### DESCRIPTION

The STLVD112 is a low voltage differential to LVTTTL signal converter with enhanced loop-back and crosspoint features. The synchronous design allows a phase alignment between a clock and its data; this means a better BER (Bit Error Rate) performance.

The advanced 0.35µm technology makes the STLVD112 suitable for data rates up to 200Mbit. The main application field is SDH/SONET telecom infrastructure. The STLVD112 flexible switch architecture makes it easy to implement multiple protection schemes in STM1 access systems. Thanks to the flexible multiplexing allowed, it becomes simple to redirect the data/clock signal coming from the faulty access card to the spare card. In normal mode the STLVD112 converts the differential data levels of the LVDS and related

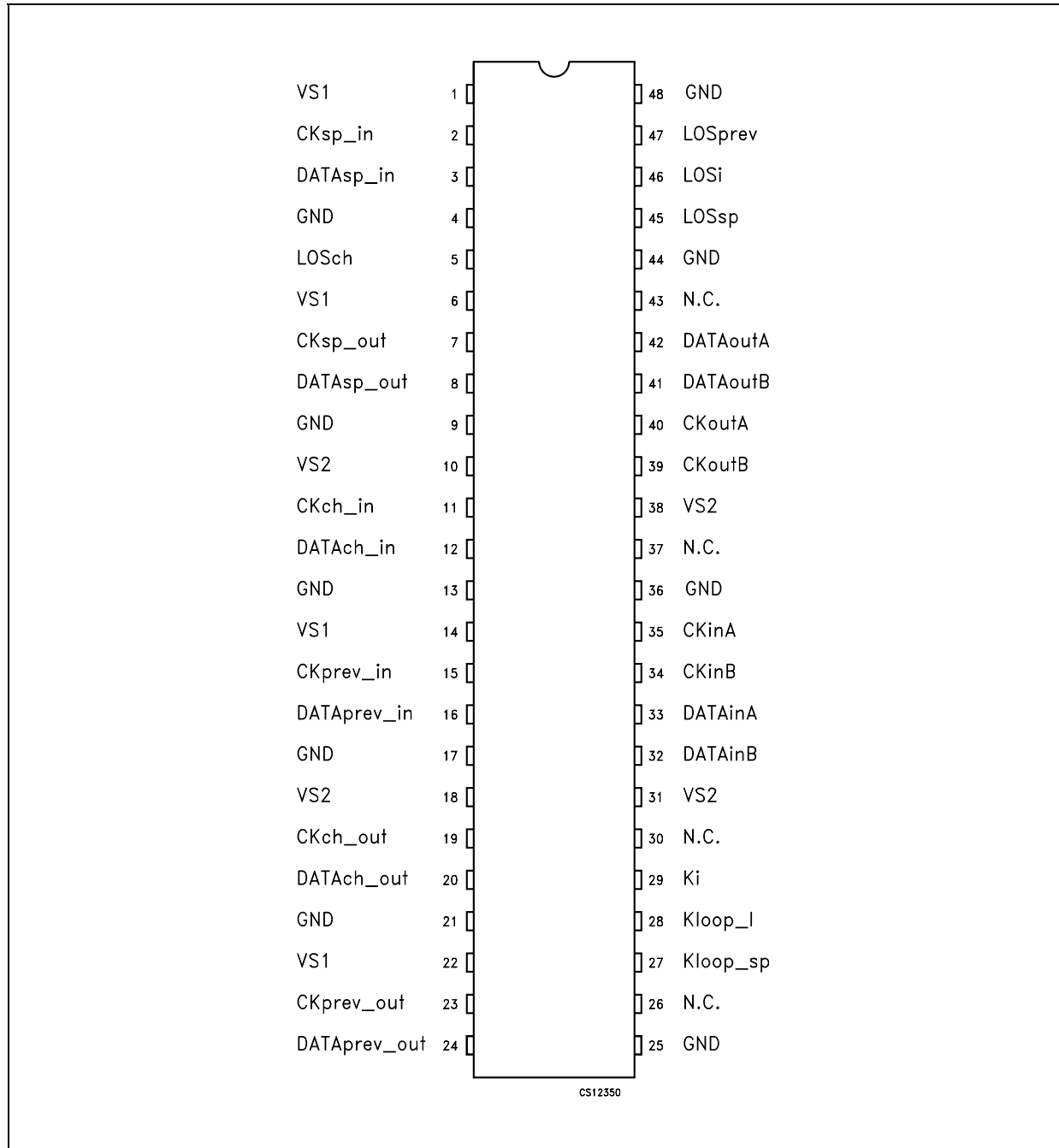


clock signal from (to) the line interface in LVTTTL level signals to (from) the backpanel. In addition the switch functions prevent the equipment from line interface faults. In fact, it is possible to switch the signals coming from a different line interface to the local line interface or the signals from the local line interface to a different line interface.

### ORDERING CODES

| Type        | Temperature Range | Package               | Comments            |
|-------------|-------------------|-----------------------|---------------------|
| STLVD112BTR | -40 to 85 °C      | TSSOP48 (Tape & Reel) | 1000 parts per reel |
| STLVD112CTR | 0 to 70 °C        | TSSOP48 (Tape & Reel) | 1000 parts per reel |

PIN CONFIGURATION



## PIN DESCRIPTION

| PIN N°                              | SYMBOL       | NAME AND FUNCTION   |
|-------------------------------------|--------------|---------------------|
| 1, 6, 14, 22                        | VS1          | Main Power Supply   |
| 2                                   | CKsp_in      | LVTTTL Clock Input  |
| 3                                   | DATAsp_in    | LVTTTL Data Input   |
| 4, 9, 13, 17, 21,<br>25, 36, 44, 48 | GND          | Ground              |
| 5                                   | LOSch        | Control Output      |
| 7                                   | CKsp_out     | LVTTTL Clock Output |
| 8                                   | DATAsp_out   | LVTTTL Data Output  |
| 10, 18, 31, 38                      | VS2          | Second Power Supply |
| 11                                  | CKch_in      | LVTTTL Clock Input  |
| 12                                  | DATAch_in    | LVTTTL Data Input   |
| 15                                  | CKprev_in    | LVTTTL Clock Input  |
| 16                                  | DATAprev_in  | LVTTTL Data Input   |
| 19                                  | CKch_out     | LVTTTL Clock Output |
| 20                                  | DATAch_out   | LVTTTL Data Output  |
| 23                                  | CKprev_out   | LVTTTL Clock Output |
| 24                                  | DATAprev_out | LVTTTL Data Output  |
| 26, 30, 37, 43                      | N.C.         | Not Connected       |
| 27                                  | Kloop_sp     | Control Input       |
| 28                                  | Kloop_l      | Control Input       |
| 29                                  | Ki           | Control Input       |
| 32                                  | DATAinB      | LVDS Data Input -   |
| 33                                  | DATAinA      | LVDS Data Input +   |
| 34                                  | CKinB        | LVDS Clock Input -  |
| 35                                  | CKinA        | LVDS Clock Input +  |
| 39                                  | CKoutB       | LVDS Clock Output - |
| 40                                  | CKoutA       | LVDS Clock Output + |
| 41                                  | DATAoutB     | LVDS Data Output -  |
| 42                                  | DATAoutA     | LVDS Data Output +  |
| 45                                  | LOSp         | Control Output      |
| 46                                  | LOSi         | Control Input       |
| 47                                  | LOSprev      | Control Input       |

## TRUTH TABLES FOR THE FIVE MUX

| INPUTS |          |         | OUTPUT    |
|--------|----------|---------|-----------|
| Ki     | Kloop_sp | Kloop_i | DATA_out  |
| LOW    | X        | X       | DATAch_in |
| HIGH   | X        | X       | DATAsp_in |

| INPUTS |          |         | OUTPUT     |
|--------|----------|---------|------------|
| Ki     | Kloop_sp | Kloop_i | DATAch_out |
| X      | X        | LOW     | DATAin     |
| X      | X        | HIGH    | DATAch-in  |

## STLVD112

| INPUTS |          |         | OUTPUT                   |
|--------|----------|---------|--------------------------|
| Ki     | Kloop_sp | Kloop_i | DATA <sub>sp</sub> _out  |
| LOW    | LOW      | X       | DATA <sub>prev</sub> _in |
| HIGH   | LOW      | X       | DATA_in                  |
| X      | HIGH     | X       | DATA <sub>sp</sub> _in   |

| INPUTS |          |         | OUTPUT            |
|--------|----------|---------|-------------------|
| Ki     | Kloop_sp | Kloop_i | LOS <sub>ch</sub> |
| X      | X        | LOW     | LOS <sub>i</sub>  |
| X      | X        | HIGH    | LOW               |

| INPUTS |          |         | OUTPUT              |
|--------|----------|---------|---------------------|
| Ki     | Kloop_sp | Kloop_i | LOS <sub>sp</sub>   |
| LOW    | LOW      | X       | LOS <sub>prev</sub> |
| HIGH   | LOW      | X       | LOS <sub>i</sub>    |
| X      | HIGH     | X       | LOW                 |

### ABSOLUTE MAXIMUM RATINGS

| Symbol           | Parameter                     | Value               | Unit |
|------------------|-------------------------------|---------------------|------|
| VS1, VS2         | Supply Voltage                | -0.3 to 4.6         | V    |
| VS2              | Supply Voltage                | -0.3 to (VS1 + 0.3) | V    |
| V <sub>I</sub>   | DC Input Voltage              | -0.3 to (VS1 + 0.3) | V    |
| V <sub>O</sub>   | DC Output Voltage             | -0.3 to (VS1 + 0.3) | V    |
| I <sub>lik</sub> | DC Input Diode Clamp Current  | ±20                 | mA   |
| I <sub>lok</sub> | DC Output Diode Clamp Current | ±20                 | mA   |
| I <sub>O</sub>   | DC Output Current             | ±50                 | mA   |
| T <sub>L</sub>   | Lead Temperature (10sec)      | 300                 | °C   |
| T <sub>stg</sub> | Storage Temperature Range     | -65 to 150          | °C   |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

### RECOMMENDED OPERATING CONDITIONS

| Symbol         | Parameter                        | Value            | Unit |
|----------------|----------------------------------|------------------|------|
| VS1, VS2       | Supply Voltage                   | 3 to 3.6         | V    |
| VS2            | Supply Voltage                   | 3 to (VS1 + 0.3) | V    |
| V <sub>I</sub> | DC Input Voltage                 | 0 to VS1         | V    |
| V <sub>O</sub> | DC Output Voltage                | 0 to VS1         | V    |
| Top            | Operating Temperature            | -45 to 85        | °C   |
| dt/dv          | Maximum Input Rise and Fall Time | 10               | ns/V |

**ELECTRICAL CHARACTERISTICS** (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A=25^\circ\text{C}$  and  $V_{S1}, V_{S2} = 3.3\text{V}$ )

| Symbol   | Parameter                   | Test Conditions                           | Value        |              |          | Unit          |
|----------|-----------------------------|---|--------------|--------------|----------|---------------|
|          |                             |   | Min.         | Typ.         | Max.     |               |
| $V_{OL}$ | Low Level Output Voltage    | $I_{OUT} = 24\text{ mA}$                  |              | 0.2          | 0.4      | V             |
| $V_{OH}$ | High Level Output Voltage   | $I_{OUT} = 24\text{ mA}$                  | $V_{S1}-0.5$ | $V_{S1}-0.3$ |          | V             |
| $V_{IL}$ | Low Level Input Thresholds  | $V_{OUT} = 0.1\text{V}$ or $V_{S1} - 0.1$ | 0            |              | 0.8      | V             |
| $V_{IH}$ | High Level Input Thresholds | $V_{OUT} = 0.1\text{V}$ or $V_{S1} - 0.1$ | 2            |              | $V_{S1}$ | V             |
| $I_{IN}$ | Input Leakage Current       | $V_{IN} = \text{GND}$ or $V_{CC}$         | -1           |              | 1        | $\mu\text{A}$ |
| $I_{CC}$ | Quiescent Supply Current    | $V_{IN} = \text{GND}$ or $V_{CC}$         |              | 15           |          | mA            |
|          |                             | $f_{CLOCK} = 155\text{MHz}$               |              | 110          |          |               |

**LVDS DRIVER ELECTRICAL CHARACTERISTICS** (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A=25^\circ\text{C}$  and  $V_{S1}, V_{S2} = 3.3\text{V}$ )

| Symbol              | Parameter   | Test Conditions                 | Value |      |          | Unit          |
|---------------------|---|---------------------------------|-------|------|----------|---------------|
|                     |   |                                 | Min.  | Typ. | Max.     |               |
| $V_{OD}$            | Differential Output Voltage   | $R_L = 100\ \Omega$             | 247   | 364  | 454      | mV            |
| $\Delta V_{OD}$     | Change in differential output voltage between logic states            |                                 | -50   |      | 50       | mV            |
| $V_{OC(SS)}$        | Steady-state common-mode output voltage                               |                                 | 1     | 1.15 | 1.30     | V             |
| $\Delta V_{OC(SS)}$ | Change in steady-state common-mode output voltage between logic State |                                 | -50   |      | 50       | mV            |
| $\Delta V_{OC(PP)}$ | Peak-to-Peack common-mode output voltage                              |                                 |       | 100  | 150      | mV            |
| $I_{SC}$            | Short Circuit Output Current  | $V_{O(Y)}$ or $V_{O(Z)} = 0$    | -24   | -4   |          | mA            |
|                     |   | $V_{OD} = 0$                    |       |      | $\pm 12$ |               |
| $I_{OFF}$           | Power Off Output Current  | $V_{CC} = 0, V_O = 2.4\text{V}$ | -1    |      | 1        | $\mu\text{A}$ |

**LVDS RECEIVER ELECTRICAL CHARACTERISTICS** (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A=25^\circ\text{C}$  and  $V_{S1}, V_{S2} = 3.3\text{V}$ )

| Symbol     | Parameter   | Test Conditions | Value      |      |            | Unit |
|------------|---|-----------------|------------|------|------------|------|
|            |   |                 | Min.       | Typ. | Max.       |      |
| $V_{ITH+}$ | Positive-going Differential Input Voltage Threshold |                 |            |      | 100        | mV   |
| $V_{ITH-}$ | Negative-going Differential Input Voltage Threshold |                 | -100       |      |            | mV   |
| $ V_{ID} $ | Magnitude of Differential Input Voltage             |                 | 0.1        |      | 0.6        | V    |
| $V_{IC}$   | Common-mode Input Voltage                           |                 | 0.5        |      | 2.4-0.5    | V    |
|            |   |                 | $ V_{ID} $ |      | $ V_{ID} $ |      |
|            |   |                 |            |      | $V_{CC}-1$ |      |

**LVDS SWITCHING TIMING CHARACTERISTICS** (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A=25^\circ\text{C}$  and  $V_{S1}, V_{S2} = 3.3\text{V}$ )

| Symbol | Parameter           | Test Conditions | Value |      |      | Unit |
|--------|---------------------|-----------------|-------|------|------|------|
|        |                     |                 | Min.  | Typ. | Max. |      |
| $t_W$  | Minimum Pulse Width |                 | <1    |      |      | ns   |

**AC LVTTTL IN LVTTTL OUT** (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A=25^\circ\text{C}$  and  $V_{S1}, V_{S2} = 3.3\text{V}$ )

| Symbol    | Parameter   | Test Conditions   | Value |      |      | Unit |
|-----------|---|---|-------|------|------|------|
|           |   |   | Min.  | Typ. | Max. |      |
| $t_{PLH}$ | Propagation Delay Time, low-to-high-level output (50% to 50%) | Measured with $V_{IN}=0$ to 2.5V, $f_{CLOCK} = 1\text{MHz}$ , $f_{DATA} = 0.5\text{MHz}$<br>$t_r = t_f = 0.4\text{ns}$ , +Duty Cycle=50%<br>$t_{PHL}$ , $t_{PLH}$ are referred to output clock transitions. | 2.4   | 3.9  | 5.6  | ns   |
| $t_{PHL}$ | Propagation Delay Time, high-to-low-level output (50% to 50%) |   | 2.5   | 4.2  | 5.3  | ns   |
| $t_{TLH}$ | Transition Time, low-to-high-level output (10% to 90%)        |   | 0.7   | 1.3  | 1.6  | ns   |
| $t_{THL}$ | Transition Time, high-to-low-level output (90% to 10%)        |   | 0.7   | 1.1  | 1.3  | ns   |
| $f_{opr}$ | Operative frequency   |   | 100   | 155  | 200  | MHz  |

**AC CONTROL OUTPUT (LOSsp, LOSch)** (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A=25^\circ\text{C}$  and  $V_{S1}, V_{S2} = 3.3\text{V}$ )

| Symbol    | Parameter   | Test Conditions   | Value |      |      | Unit |
|-----------|---|---|-------|------|------|------|
|           |   |   | Min.  | Typ. | Max. |      |
| $t_{PLH}$ | Propagation Delay Time, low-to-high-level output (50% to 50%) | Measured with $V_{IN}=0$ to 2.5V, $f_{CLOCK} = 1\text{MHz}$ , $f_{DATA} = 0.5\text{MHz}$<br>$t_r = t_f = 0.4\text{ns}$ , +Duty Cycle=50%<br>$t_{PHL}$ , $t_{PLH}$ are referred to output clock transitions. | 2.4   | 3.6  | 4.4  | ns   |
| $t_{PHL}$ | Propagation Delay Time, high-to-low-level output (50% to 50%) |   | 2.4   | 3.4  | 4.2  | ns   |
| $t_{TLH}$ | Transition Time, low-to-high-level output (10% to 90%)        |   | 0.9   | 1.9  | 2.3  | ns   |
| $t_{THL}$ | Transition Time, high-to-low-level output (90% to 10%)        |   | 0.7   | 1.0  | 1.2  | ns   |

**AC LVTTTL IN LVDS OUT** (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A=25^\circ\text{C}$  and  $V_{S1}, V_{S2} = 3.3\text{V}$ )

| Symbol    | Parameter   | Test Conditions   | Value |      |      | Unit |
|-----------|---|---|-------|------|------|------|
|           |   |   | Min.  | Typ. | Max. |      |
| $t_{PLH}$ | Propagation Delay Time, low-to-high-level output (50% to 50%) | Measured with $V_{IN}=0$ to 2.5V, $f_{CLOCK} = 1\text{MHz}$ , $f_{DATA} = 0.5\text{MHz}$<br>$t_r = t_f = 0.4\text{ns}$ , +Duty Cycle=50%<br>$t_{PHL}$ , $t_{PLH}$ are referred to output clock transitions. | 2.8   | 3.8  | 4.7  | ns   |
| $t_{PHL}$ | Propagation Delay Time, high-to-low-level output (50% to 50%) |   | 2.6   | 3.4  | 4.1  | ns   |
| $t_{TLH}$ | Transition Time, low-to-high-level output (20% to 80%)        |   | 0.4   | 0.5  | 0.6  | ns   |
| $t_{THL}$ | Transition Time, high-to-low-level output (80% to 20%)        |   | 0.4   | 0.6  | 0.7  | ns   |
| $f_{opr}$ | Operative frequency   |   | 100   | 155  | 200  | MHz  |

**AC LVDS IN LVTTTL OUT** (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A=25^\circ\text{C}$  and  $V_{S1}, V_{S2} = 3.3\text{V}$ )

| Symbol    | Parameter   | Test Conditions  | Value |      |      | Unit |
|-----------|---|--|-------|------|------|------|
|           |   |  | Min.  | Typ. | Max. |      |
| $t_{PLH}$ | Propagation Delay Time, low-to-high-level output (50% to 50%) | $V_{DIFF} = 400\text{mV}$<br>Measured with $V_{ICM} = 1.2\text{V}$ ,<br>$f_{CLOCK} = 1\text{MHz}$ , $f_{DATA} = 0.5\text{MHz}$<br>$t_r = t_f = 0.4\text{ns}$ , +Duty Cycle=50%<br>$t_{PHL}$ , $t_{PLH}$ are referred to output clock transitions | 4.3   | 5.6  | 6.9  | ns   |
| $t_{PHL}$ | Propagation Delay Time, high-to-low-level output (50% to 50%) |  | 4.1   | 5.4  | 6.7  | ns   |
| $t_{TLH}$ | Transition Time, low-to-high-level output (10% to 90%)        |  | 0.7   | 0.9  | 1.1  | ns   |
| $t_{THL}$ | Transition Time, high-to-low-level output (90% to 10%)        |  | 0.8   | 1.0  | 1.3  | ns   |
| $f_{opr}$ | Operative frequency   |  | 100   | 155  | 200  | MHz  |

**LVTTTL IN LVTTTL OUT** ( $V_{CC} = 3$  to  $3.6\text{V}$   $T_A = -45$  to  $80^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = 25^\circ\text{C}$ )

| Symbol | Parameter  | Test Conditions   | Value |      |      | Unit |
|--------|------------|---|-------|------|------|------|
|        |            |   | Min.  | Typ. | Max. |      |
| $t_s$  | Setup Time | $f = 10\text{MHz}$ , $V_{ICM} = 1.2\text{V}$                    | 1     |      |      | ns   |
| $t_H$  | Hold Time  | $V_{DIFF} = 400\text{mV}$ ,<br>$V_{INTTL} = 0$ to $2.5\text{V}$ | 1     |      |      | ns   |

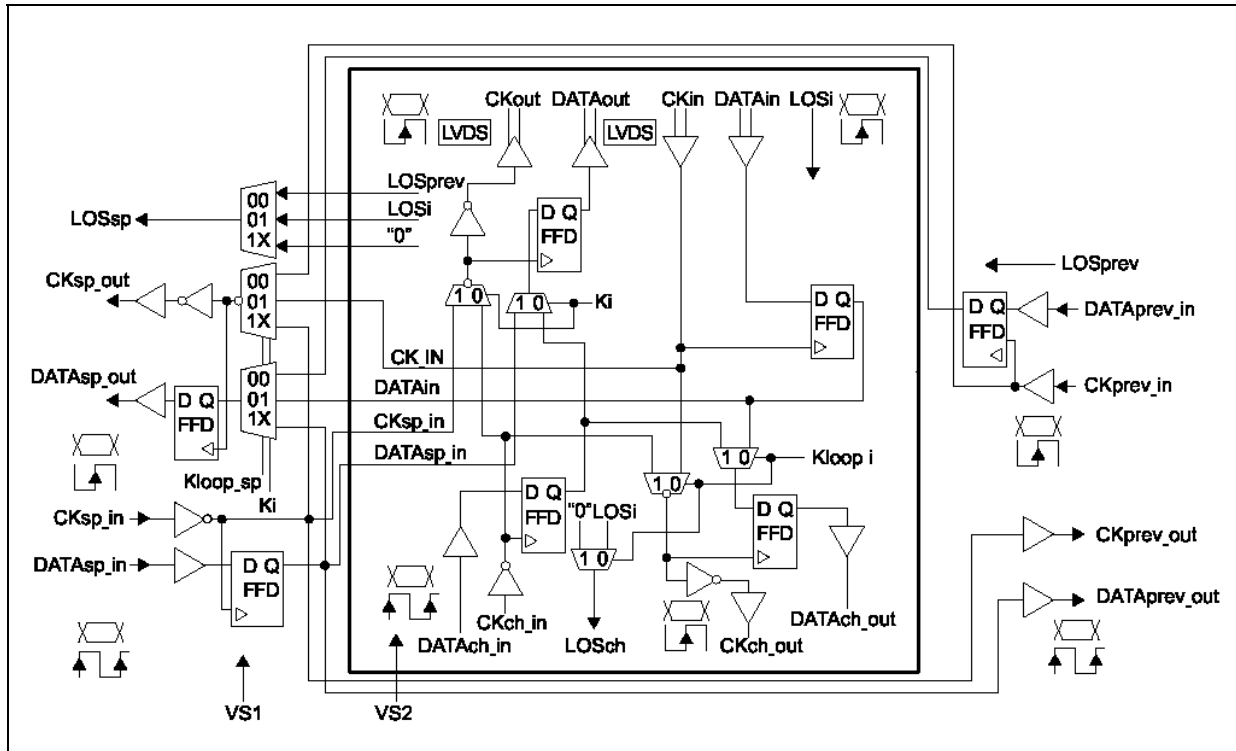
**LVTTTL IN LVDS OUT** (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A=25^\circ\text{C}$  and  $V_{S1}, V_{S2} = 3.3\text{V}$ )

| Symbol | Parameter  | Test Conditions   | Value |      |      | Unit |
|--------|------------|---|-------|------|------|------|
|        |            |   | Min.  | Typ. | Max. |      |
| $t_s$  | Setup Time | $f = 10\text{MHz}$ , $V_{ICM} = 1.2\text{V}$                    | 1     |      |      | ns   |
| $t_H$  | Hold Time  | $V_{DIFF} = 400\text{mV}$ ,<br>$V_{INTTL} = 0$ to $2.5\text{V}$ | 1     |      |      | ns   |

**LVDS IN LVTTTL OUT** (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A=25^\circ\text{C}$  and  $V_{S1}, V_{S2} = 3.3\text{V}$ )

| Symbol | Parameter  | Test Conditions   | Value |      |      | Unit |
|--------|------------|---|-------|------|------|------|
|        |            |   | Min.  | Typ. | Max. |      |
| $t_s$  | Setup Time | $f = 10\text{MHz}$ , $V_{ICM} = 1.2\text{V}$                    | 1.5   |      |      | ns   |
| $t_H$  | Hold Time  | $V_{DIFF} = 400\text{mV}$ ,<br>$V_{INTTL} = 0$ to $2.5\text{V}$ | 1     |      |      | ns   |

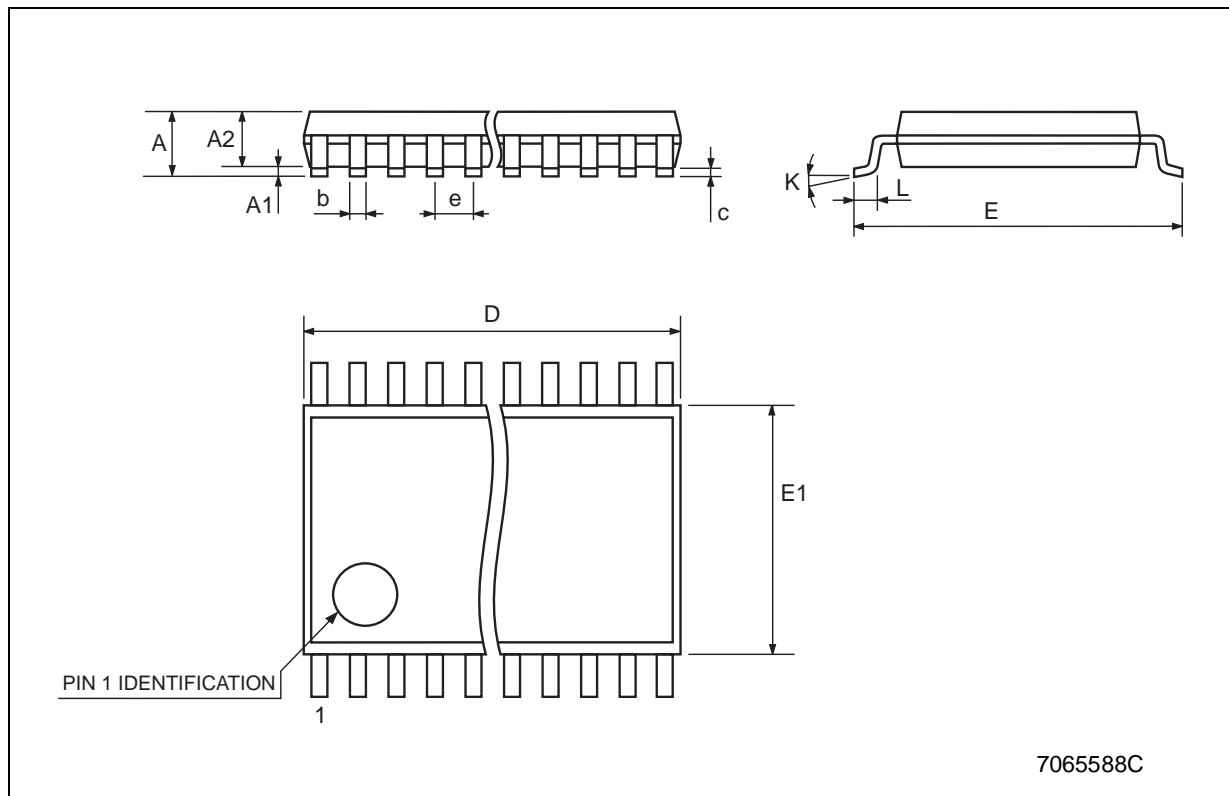
LOGIC DIAGRAM





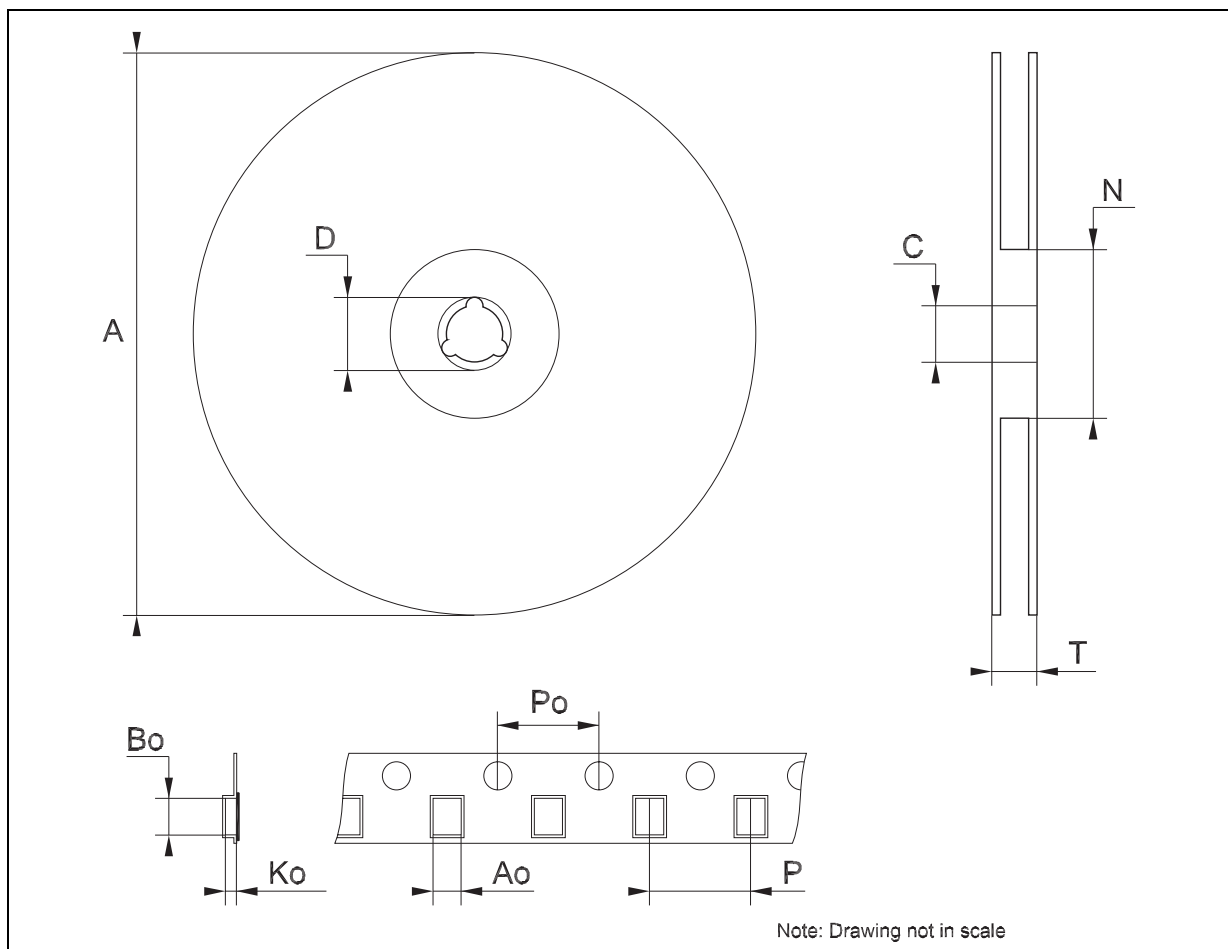
## TSSOP48 MECHANICAL DATA

| DIM. | mm.  |         |      | inch   |            |        |
|------|------|---------|------|--------|------------|--------|
|      | MIN. | TYP.    | MAX. | MIN.   | TYP.       | MAX.   |
| A    |      |         | 1.2  |        |            | 0.047  |
| A1   | 0.05 |         | 0.15 | 0.002  |            | 0.006  |
| A2   |      | 0.9     |      |        | 0.035      |        |
| b    | 0.17 |         | 0.27 | 0.0067 |            | 0.011  |
| c    | 0.09 |         | 0.20 | 0.0035 |            | 0.0079 |
| D    | 12.4 |         | 12.6 | 0.488  |            | 0.496  |
| E    |      | 8.1 BSC |      |        | 0.318 BSC  |        |
| E1   | 6.0  |         | 6.2  | 0.236  |            | 0.244  |
| e    |      | 0.5 BSC |      |        | 0.0197 BSC |        |
| K    | 0°   |         | 8°   | 0°     |            | 8°     |
| L    | 0.50 |         | 0.75 | 0.020  |            | 0.030  |



**Tape & Reel TSSOP48 MECHANICAL DATA**

| DIM. | mm.  |     |      | inch  |      |        |
|------|------|-----|------|-------|------|--------|
|      | MIN. | TYP | MAX. | MIN.  | TYP. | MAX.   |
| A    |      |     | 330  |       |      | 12.992 |
| C    | 12.8 |     | 13.2 | 0.504 |      | 0.519  |
| D    | 20.2 |     |      | 0.795 |      |        |
| N    | 60   |     |      | 2.362 |      |        |
| T    |      |     | 30.4 |       |      | 1.197  |
| Ao   | 8.7  |     | 8.9  | 0.343 |      | 0.350  |
| Bo   | 13.1 |     | 13.3 | 0.516 |      | 0.524  |
| Ko   | 1.5  |     | 1.7  | 0.059 |      | 0.067  |
| Po   | 3.9  |     | 4.1  | 0.153 |      | 0.161  |
| P    | 11.9 |     | 12.1 | 0.468 |      | 0.476  |



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